Process Issues in Micro Via Fabrication and their Impact on CMP

Anke Hanisch[1] Jens Bonitz[1] Jinji Luo-Hofmann[1] Lutz Hofmann[1] Romy Junghans[1] Imme Ellebrecht[2] Knut Gottfried[1,2]

1) Fraunhofer ENAS, Technology Campus 3, 09126 Chemnitz, Germany

2) ErzM-Technologies UG, Technology Campus 1, 09126 Chemnitz, Germany

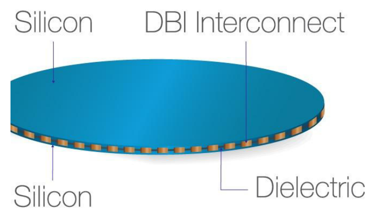
Outline

- Background / general remarks to hybrid bonding
- Hybrid bond layer process flow
- Conclusions
- Next European CMP and WET UGM

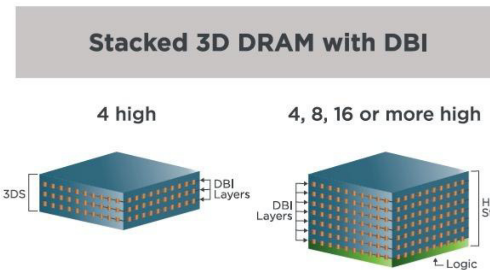
Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

Background – wafer level / hybrid integration by hybrid bonding (W2W or D2W)

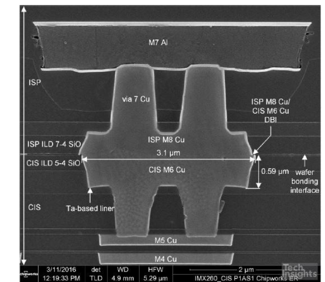
- 1st wave: Sensors, displays, edge devices
- 2nd wave: NAND
- 3rd wave: Computing devices
- ???



© Adeia / Experi

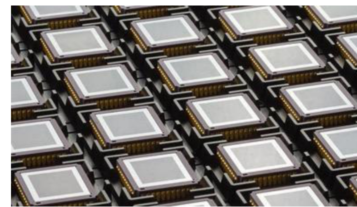


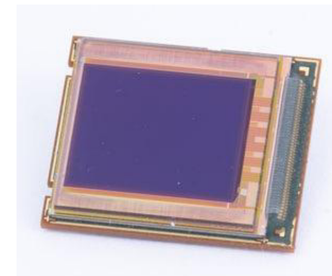
© Adeia / Experi

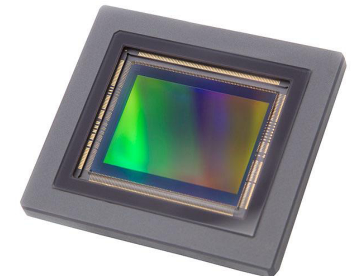


© TechInsights

© EV Group Austria

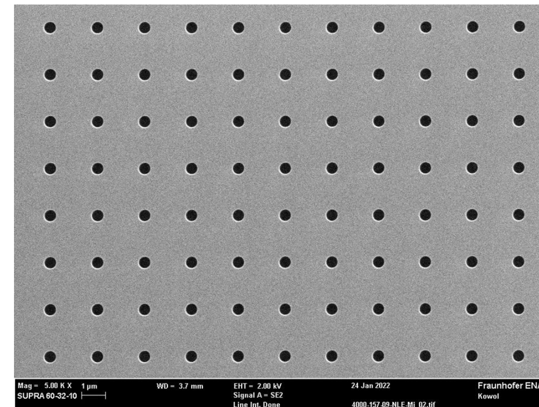

Micro Bolometer © Teledyne DALSA

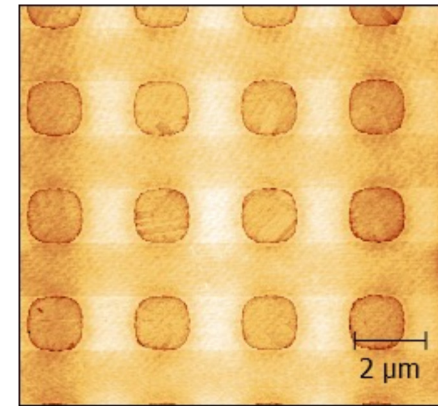

Micro OLED Display © VECTED GmbH

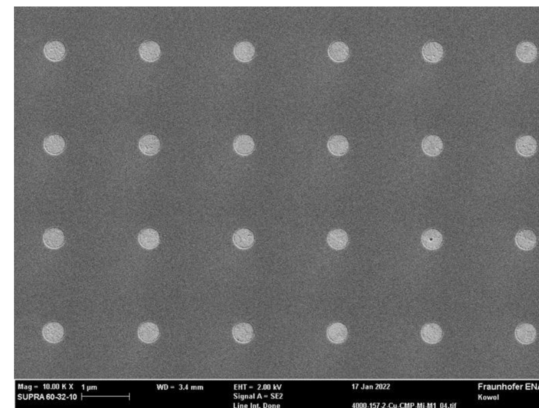

Canon CMOS Image Sensor
13272H x 9176V © Canon

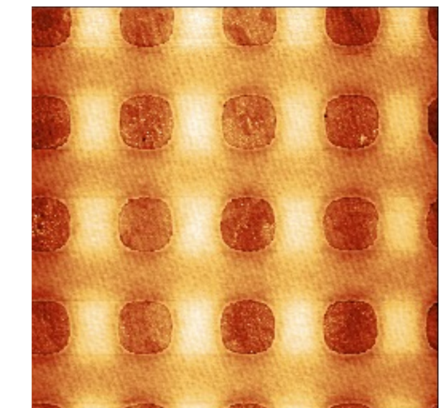
Hybrid bonding

- Achieving electrical and mechanical connection in on single step
  - Spontaneous direct bond in dielectric area
  - Subsequent annealing
    - Transforms physical bonds to chemical bonds (dielectric)
    - Cu to Cu bond in electrical contacts (vias)
- Very high number of electrical connections
  - Example 4k micro display with 3840 x 3840 resolution
  - 14,745,600 pixels = contacts = vias per die!
- Micro vias
  - Main building blocks for hybrid bonding
  - Diameter from below 1µm up to a few µm
  - Thickness in µm range







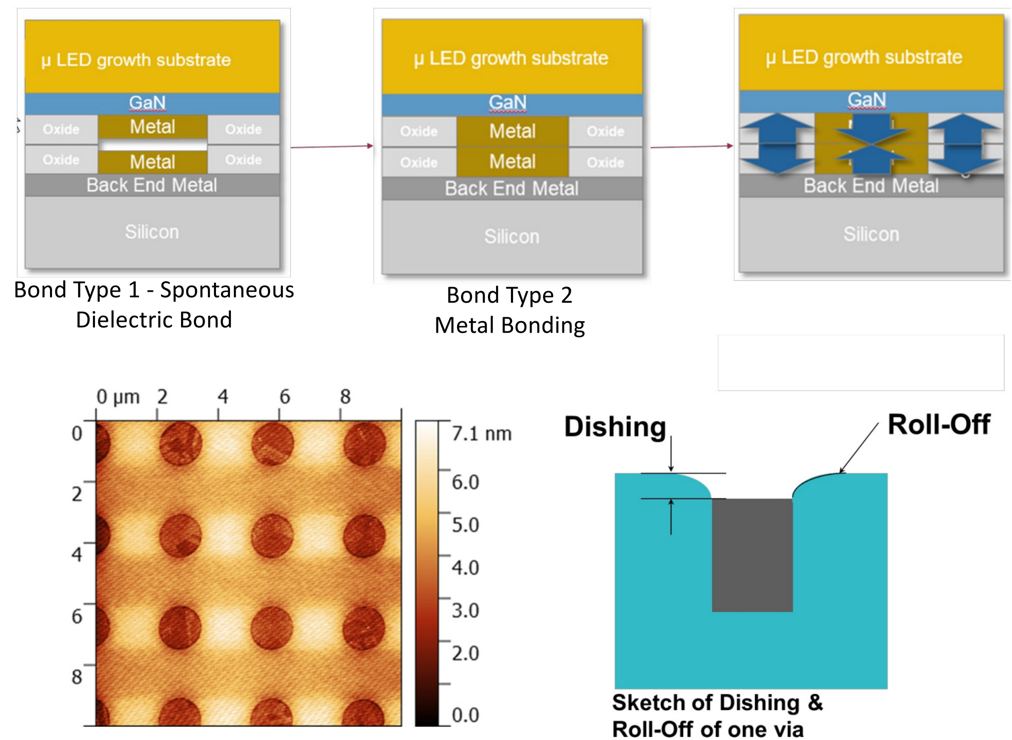


Hybrid bonding – process requirements

- Good uniformity: within die, within wafer, wtw
- Low remaining topography
- Low roughness

Specific to hybrid bonding applications

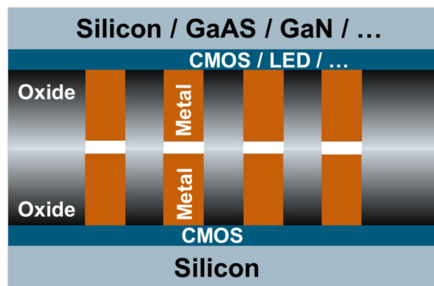
- Oxide roughness: same as direct bonding < 0.5 nm
- Oxide rounding: < 1 nm / µm
- Cu roughness in lower nm range
- Dishing: no rule of thumb, depends on via size (Cu-volume) and temperature budget (typ. 1 nm … 10 nm)
- Low remaining long-range topography (typ. less than 10 nm)
- Trenching: as low as possible (undesired effect)



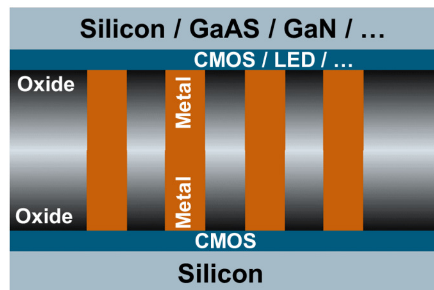
Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

Hybrid bonding – failure modes

Oxide to Oxide bond at room temperature



Heat closes dishing gap (metal CTE > Oxide CTE)

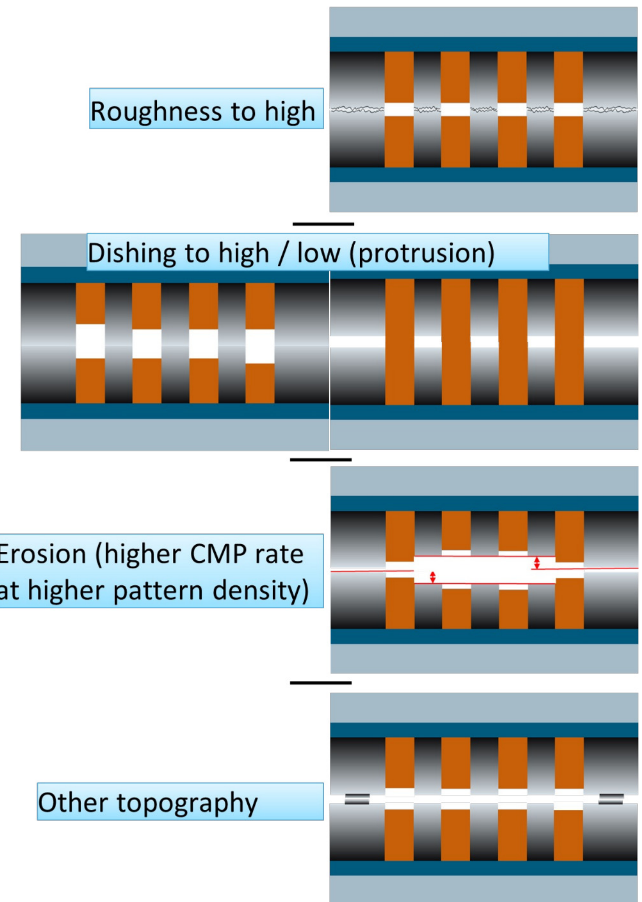


Critical parameters for bonding

- Roughness Oxide
- Dishing
- Erosion
- Topography (from underlying layers)

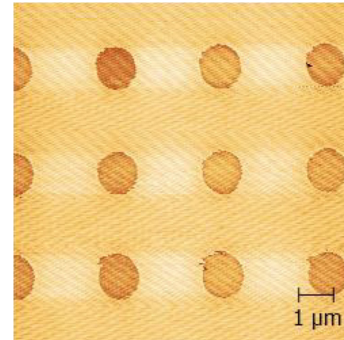
These parameters have to be measured during processing in an adequate way to increase homogeneity, quality, yield, …

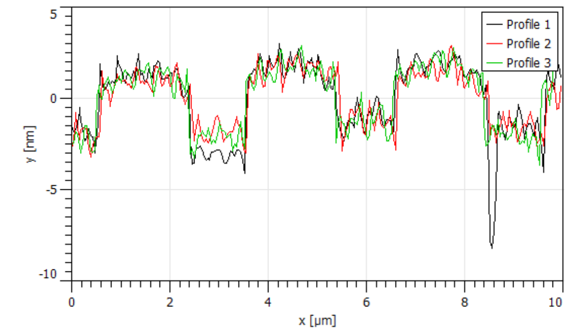
Failure modes, which prevent bonding

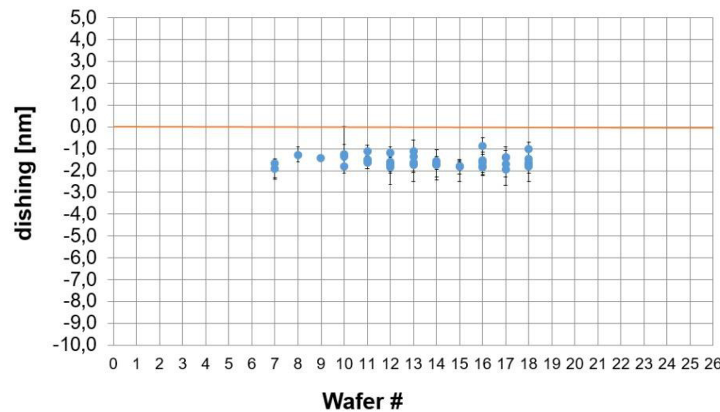


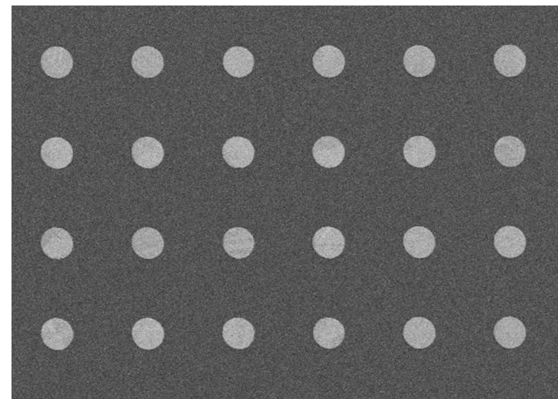
Hybrid bonding – challenge for CMP, but doable

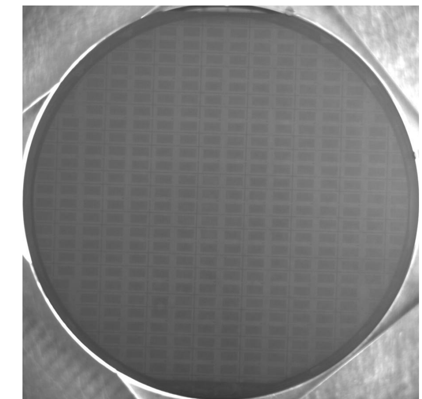
- Precise process control
- Good process monitoring
- Appropriate consumables
- Deep process understanding (e.g. interaction between CMP and post CMP cleaning)



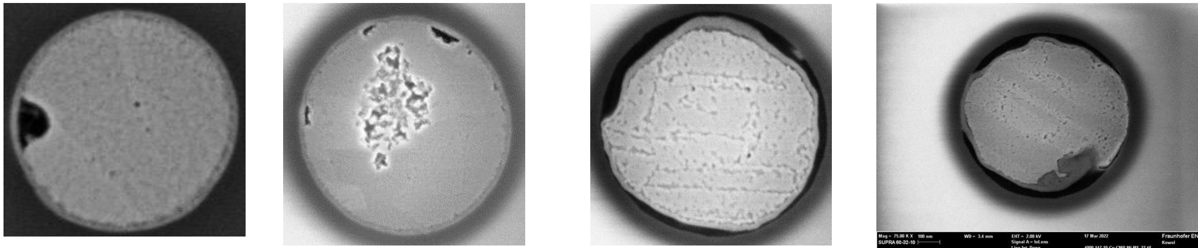


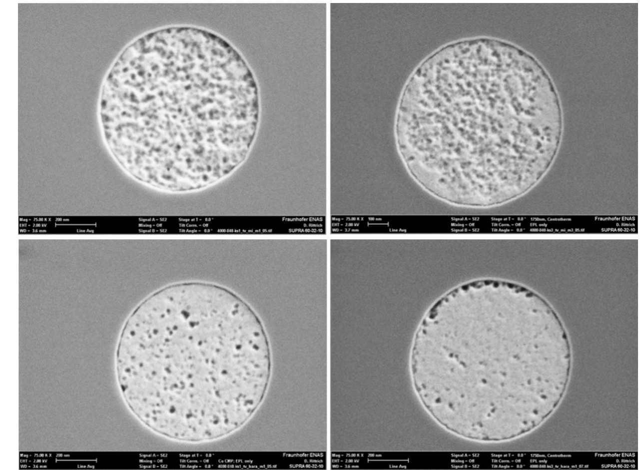






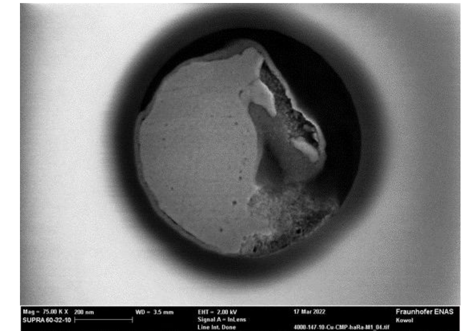
What’s that?





That can only be caused by ECD or CMP – but most likely it is CMP!

- Your slurry is too aggressive!
- You have the wrong parameters!
- That’s light induced corrosion!
- That’s galvanic corrosion!
- That’s …



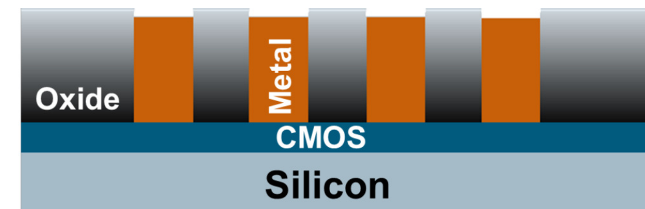
Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

Hybrid bond layer processing – process flow

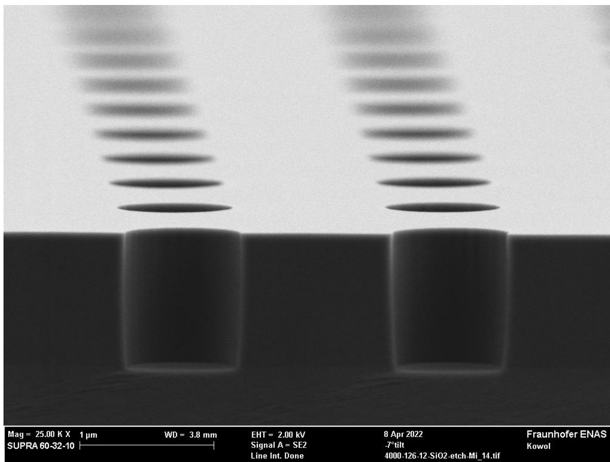
Hybrid bond layer processing is not only CMP – it is an integration scheme! CMP is only that process that reveals everything, also from process steps before!

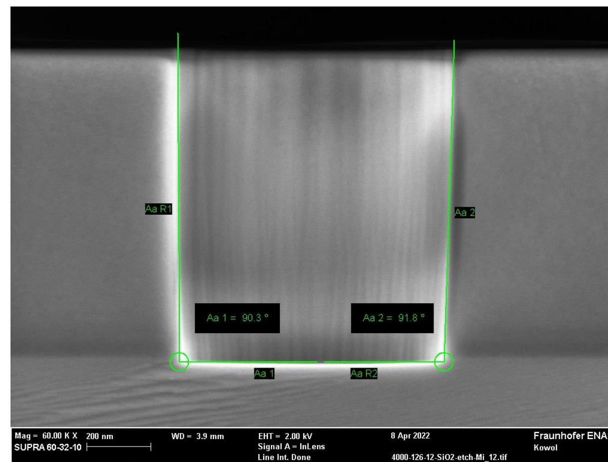
- Dielectric deposition (Si_aO_b, $Si_aO_bN_c$, $Si_aC_bN_c$)
- Dielectric planarization
- Via lithography (type of resist, thickness)
- Via etch
- Resist strip / post etch resist removal
- Barrier / seed deposition
- ECD including pre and post treatment
- Cu/Barrier CMP

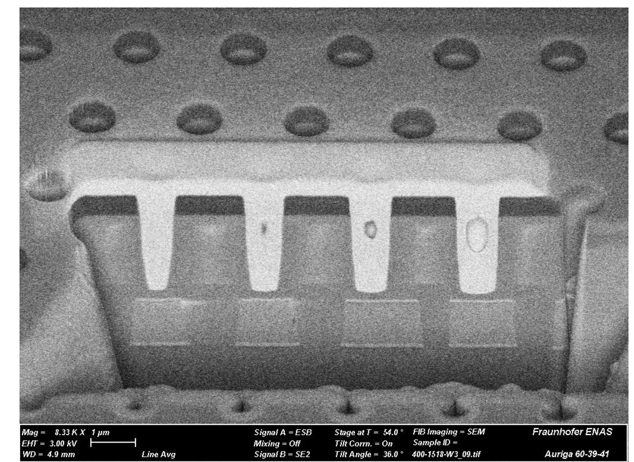
Hybrid bond layer



Hybrid bond layer processing – Via etch



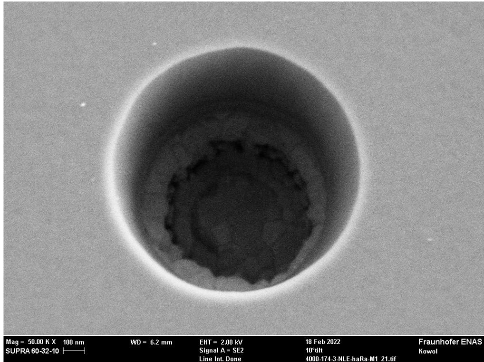


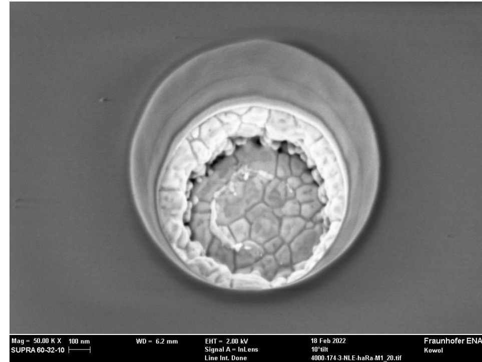


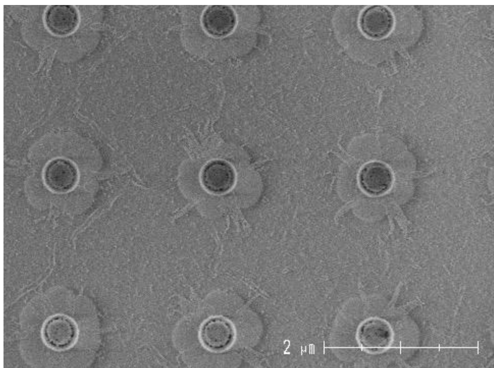
- Sidewall roughness
- Profile / taper
- Endpoint
- Over etch
- No attack of underlying material

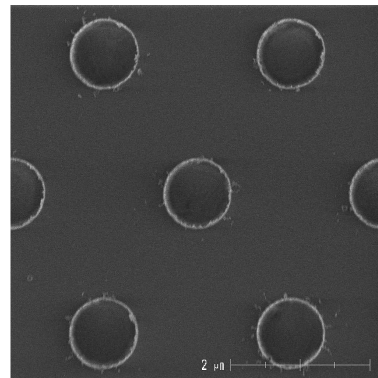
Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

Hybrid bond layer processing – Resist strip & PER

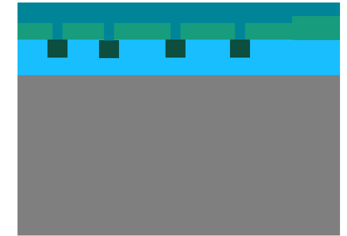






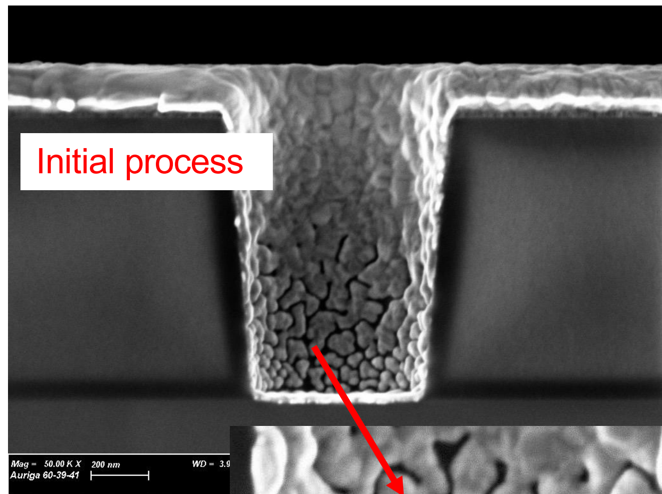


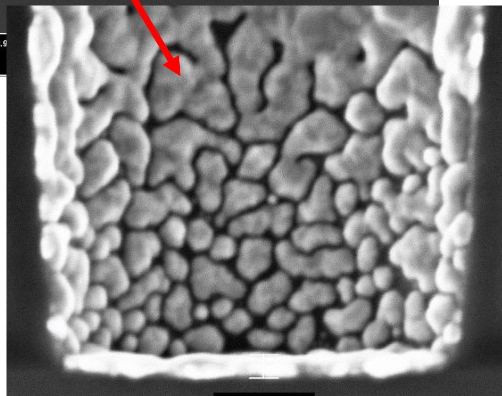
- General approach
  - Wet
  - Dry
  - Wet + dry // dry + wet
- Underlying metal (Al, Cu, …)
- Removal efficiency
- Selection of suitable strip chemistries



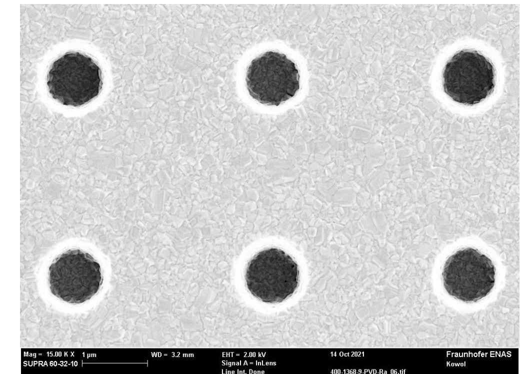
➢ Resist strip and PER is probably the most critical process in processing hybrid bond layers

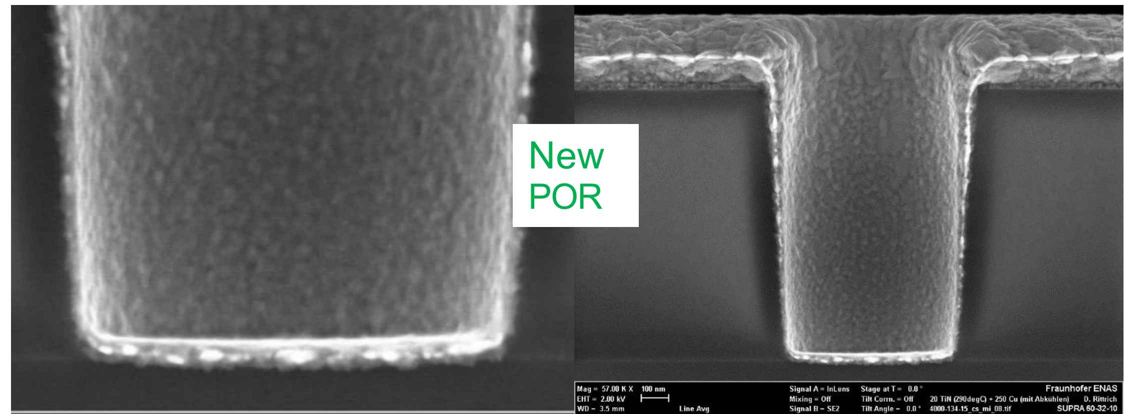
Hybrid bond layer processing – barrier seed deposition





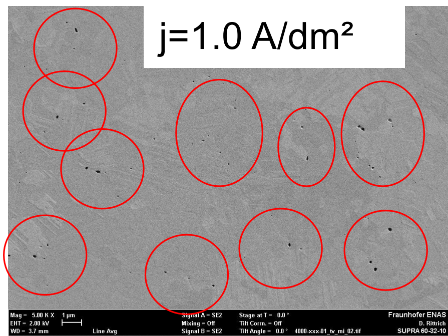
- Barrier material (Ti/TiN, Ta/TaN, …)
- Cu-seed
  - Process (PVD, i-PVD, MoCVD, …)
  - Thickness
- Other parameters (e.g. temperature, …)

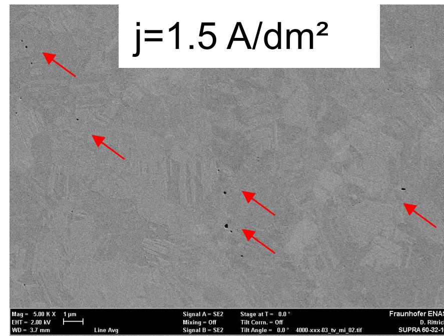


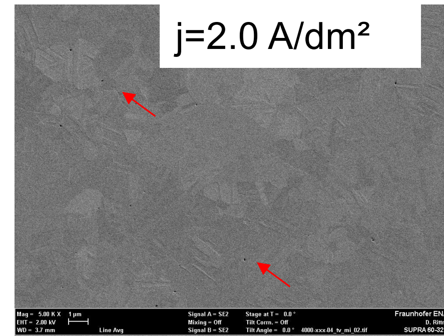


Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

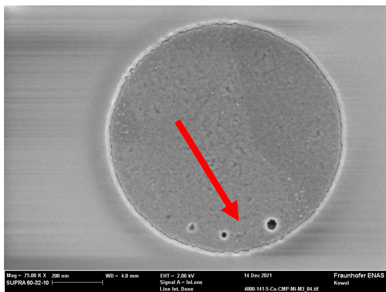
Hybrid bond layer processing – ECD including pre and post treatments

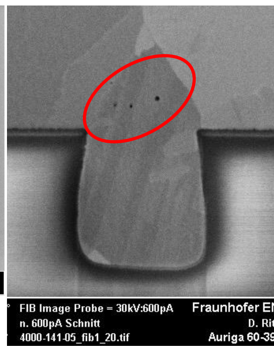


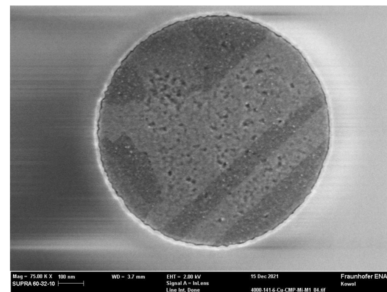


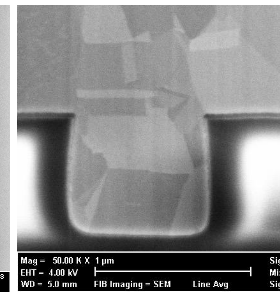


- Electrolyte
- Descum
- Pre-treatment (vacuum)
- Process parameters
- Post ECD-anneal
  - Temperature
  - Ramping







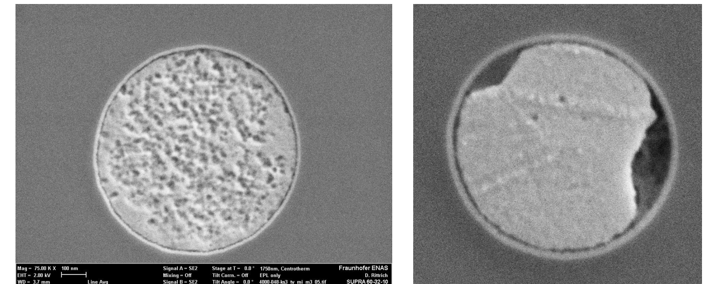


Fraunhofer ENAS
TECHNISCHE UNIVERSITÄT CHEMNITZ
ZfM
Erz

Conclusion

- Hybrid bond layer processing is a very sensitive integration scheme and not only a sequence of processes
- Requires a well aligned process regime
- The sequence litho – etch – strip – barrier/seed – ECD is time critical - rule of thumb 3 days!
- Problems become visible after CMP but in many cases are not caused by CMP only
  - ➢Most failures in the via fabrication flow result in porous or partially filled vias, visible after CMP only
  - ➢Look into the entire integration scheme first!

Problems remain? – We are happy to help you ☺



Thank you for your attention!

Imme Ellebrecht
+49 176 46651838
imme.ellebrecht@erzm-tech.com

Dr. Knut Gottfried
+49 179 2042873
knut.gottfried@erzm-tech.com

Next European CMP & WET Users Meeting …

…Spring Meeting 2025, April 10 & 11, IMEC, Leuven, Belgium