The Inception of Chemical Mechanical Polishing for Device Applications

By

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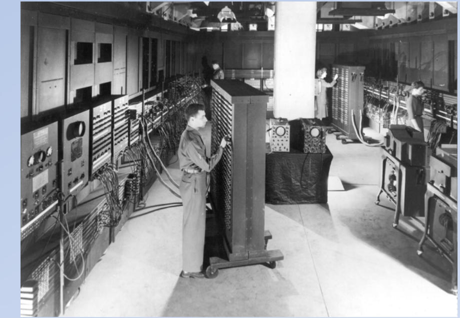
with

Bob Roberts, X-trinsic Inc. and Chair, North America CMP User Group PC

The Inception of Chemical Mechanical Polishing
for
Device Applications

The initial few slides of this presentation are intended to give the reader a sense of how the pent-up demand for a viable, workable, efficient, and cost effective planarization solution came about once multi-layer circuit design became imperative. There should be no doubt that without Chemical Mechanical Polishing for the planarization of thin films on semiconductor wafers and MEMS devices and other nanotechnology applications, the digital age would be stalled in the 1980's timeframe. It is true that someone, sometime would have probably determined that the roadblocks and pothole hazards of the CMP polishing process could be overcome. However, it was Dr. Klaus Beyer who took the reigns, saw the great advantages, and broke through the barriers of fear and hesitation, to champion the technology we know of today as "CMP," the mainstream enabling technology that makes possible all things digital.

The Inception of CMP

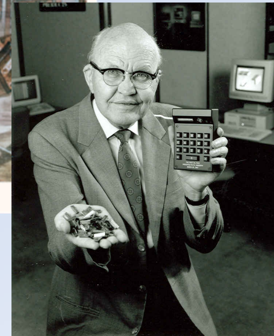


A Quick Walk Through History

1895 Guglielmo Marconi invents a practical radio-based wireless telegraph system and transmits signals through the air from one end of his house to the other.

1946 **ENIAC –** first general-purpose computer is announced. Features 18,000 vacuum tubes, weighs 30 tons, takes up a 160 square meter room.

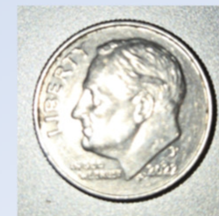
1947 December 16th, Walter Brattain and John Bardeen, working under William Shockley at AT&T Bell Labs make the first transistor.



1958 Jack Kilby invents first hybrid IC (Germanium)

1959 Robert Noyce invents the monolithic IC (silicon)

1959 Monsanto (manufacturing the artificial sweetener saccharin) starts new division to produce ultra-pure silicon wafers (their first silicon wafer was 19 millimeters in diameter!).



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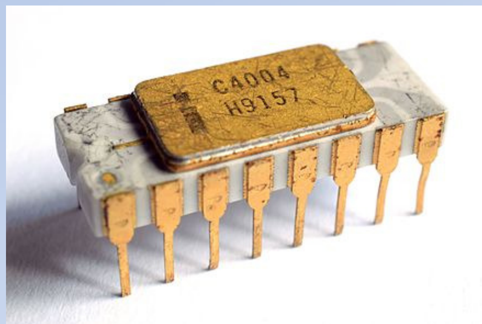
A Quick Walk Through History

1962 MEMC introduced into manufacturing:

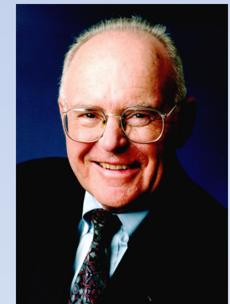
- the automated CMP process for Si wafers which established a new flatness standard
- the Czochralski crystal growing process.

1965 Gordon Moore (INTEL) proclaimed that the number of transistors that can fit on an integrated circuit will double every two years. This becomes “Moore’s Law.”

1971 Intel’s first microprocessor the 4004, was released and contained 2300 transistors. Cost = $60 (=$500 in 2024)



Raytheon, 1956



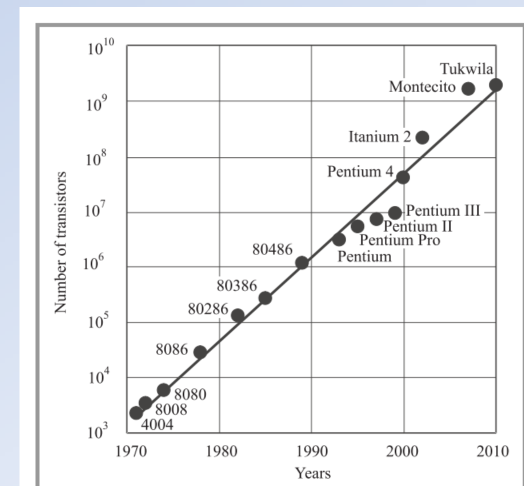


Fig. 7. Number of transistors in successive Intel processors as a function of time (data after [44]).

Semanticscholar.org: History of Semiconductors

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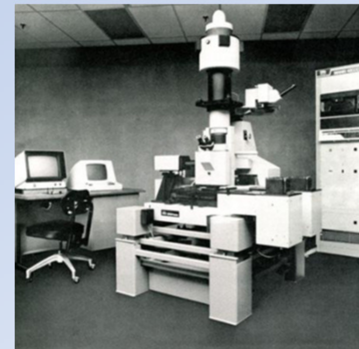
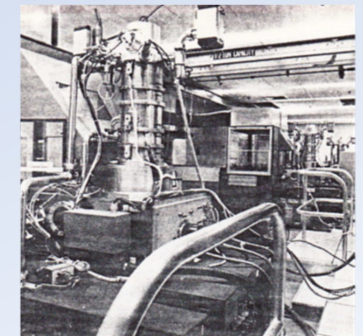
A Quick Walk Through History

1973 Perkin Elmer introduces the Micralign Projection Scanning Aligner, and P&E cannot make them fast enough. Improves IC yields from typical 10% to up to 50% to 70%. IC prices drop, applications become more widespread.

1975 AMAT brings out the 7600 EPI Reactor which becomes their "Flagship" product and this makes AMAT a major supplier.



1976 GCA Corp. (General Cable) offers Mann 4800 Direct Step-on-Wafer Photolithography Repeater which could reach 1 micron feature size. It took a long time to become the stepper of choice.



1977 IBM invented the Electron Beam Litho System (Model EL-1). Featured 2.5 µm dimensions on 100mm wafers but it was slow, at 1 exposure/hour. Typical steppers were 20-30 exposures/hour.

Check out: www.emergingtechbrew.com/stories/2021/10/21/a-200-year-timeline-of-the-semiconductor-industry

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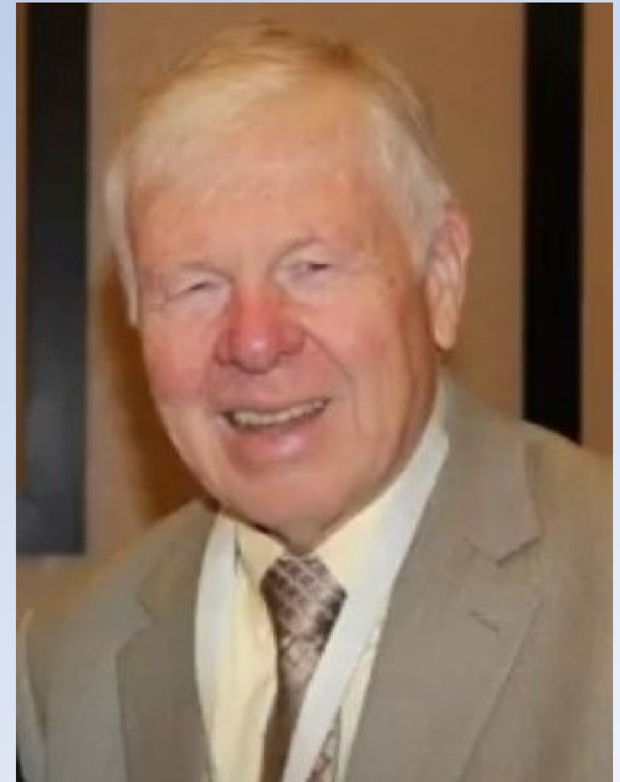
A Quick Walk Through History

1966 Dr. Klaus Beyer immigrates to the United States from West Germany, where he had received his PhD in Physical Chemistry, from the University of Bonn. He begins a Post-Doctoral internship at The Ohio State University to study semiconductor doping processes and several other process steps including the chemical surface cleaning of raw silicon substrates.

1968 Klaus Beyer joins IBM.

1976 Klaus joins the technical staff of the IBM Reliability Lab.

1981 Klaus transfers to the wafer production facility and is asked to solve a microscratch problem caused by the brush cleaning of wafers that were coated with slurry. NOTE: Major semiconductor companies (IBM, Motorola, TI, etc.), were growing their own silicon ingots (boules) from melted silicon solution. These companies were vertically integrated and had their own ingot growth-to-epi wafer processing facilities. This gave Klaus access to the IBM polishing department.



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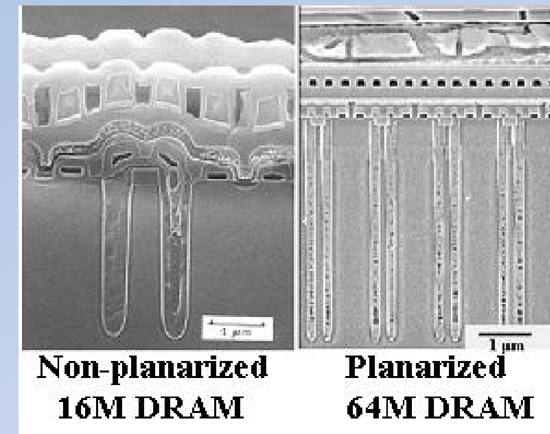
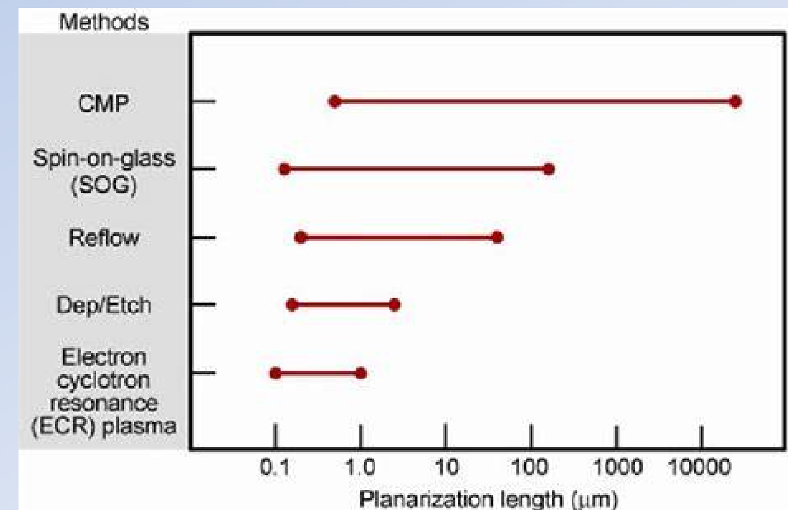
Other Planarization Methods:

- Thermal flow
  - Dielectric planarization (BPSG)
  - High temperature, ~ 1000° C
- Sputtering etchback
- Photoresist etchback
  - Apply spin coat
  - Wet chemical etchback
  - Plasma etch with CF_4/O_2 (Carbon Tetrafluoride)
- Spun-on-Glass (SOG) etchback
  - replaced Photoresist etchback
  - Useful even when features sizes were as small as 0.5 µm
- Ion milling
  - A true competitive technology, but…
  - Too slow, too expensive, poor global planarization



5.4 Summary to 5: Integrated Circuits - Process Integration www.tf.uni-keil.de



www.researchgate.net by Prof. Jin-Goo Park

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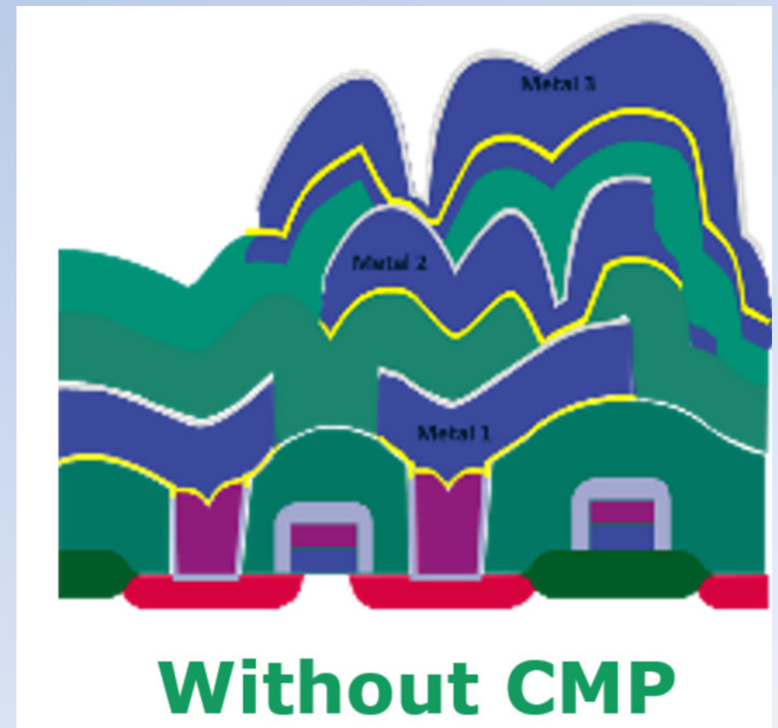
What are the overriding driving forces that brought on the demand for Chemical Mechanical Polishing?

Without CMP it was difficult to overcome:

- The limitations of the depth of focus of the lithography systems.
- Large thickness etch required
- Poor step coverage



Planarization | Merck KGaA, Darmstadt, Germany

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What happened next?

- Klaus assigned to work on microscratching problem
- Became interested in Megasonic cleaning. Ultrasonics were known to damage the surface of the wafer, so there was sceptisim about megasonics. Klaus was running experiments in the IBM polishing department to try to use megasonics to remove residual polishing slurry.
- Klaus was also assigned part-time to the team trying to solve a wafer stress problem related to glass-filled trench isolation caused by "humps and bumps" on the surface.
  - Glass reflow techniques were being used but this method was only effective over short distances.
  - Covering a larger area was problematic because the glass flow did not planarize very well and caused localized glass bulges.

…and now, in the words of Dr. Klaus Beyer, this is the rest of the story….

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NOTE: The following is a combination of portions of papers written by Dr. Klaus Beyer, IBM Fellow (retired). One of these papers was first published in "IBM MicroNews, Vol.5, No. 4, November 1999, and later published in "Future Fab International." An additional reference is from an article in a Japanese publication named "Coffee Break" the date of which is unknown. This information refers to his discovery/application of Chemical Mechanical Polishing for the Planarization of Thin Films.

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Conceiving the Idea

As far as I could see, no existing planarization concept could solve that problem with the non-planar glass surfaces. In one last ditch effort in early (January) 1983, I took a trench wafer covered by re-flown lead-silicate glass to the polishing tables in the silicon wafer production area. I speculated that polishing might smooth out these bulging glass humps. Polishing, of course, produces severe contamination but since by then I had become adept at the process of Megasonic particle removal, I decided to use this cleaning technology on polished glass coated trench wafers.

To my amazement and delight, the last step delivered not only a clean looking trench wafer, but microscopic analysis confirmed an entirely planarized glass surface, the likes of which I had never seen before. Our uneven glass surface problem was solved!

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For two weeks, I kept these results to myself. I was fully aware that I was successfully using an unacceptable, dirty process. Nevertheless, I was able to clean up the dirty polishing slurry. The next step for this controversial planarization was finding support for manpower and hardware. I thought that potential applications for oxide planarization would be in the chip wiring and trench isolation sectors. The IBM corporation had an Open-Door policy to access upper management, used mostly for personal problems, but in my case, I stated that I discovered a solution for two serious problems. To my surprise, upper IBM management was very interested in my proposal and I got support for a small team to study oxide planarization using chemical mechanical polishing. After approximately ten months of studying the impact of oxide planarization by CMP on actual device wafers no problems were discovered and IBM management approved the use of CMP for actual product wafers.

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Perhaps there are some lessons to be learned about innovation from this experience. The history of science proves time and time again, how unquestioned assumptions can restrict avenues of inquiry. Most thinking is circumscribed by what Alfred North Whitehead called, "The Climate Opinion." Innovation on the other hand, can result from questioning what appears to be unquestionable.

Another lesson is the value of cross-discipline experience and communication. So it was that with a unique combination of experiences my freedom from the assumption that mechanical polishing was too dirty, plus some imagination, and also some luck, we discovered that a Chemical-Mechanical approach to planarization led to a long sought-after solution.

Respectfully yours,

Dr. Klaus Beyer

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Thank you.

Klaus sends his best regards, and wishes he could be with us today. To those of us who have made a career out of CMP, he is a true hero.

Please share Klaus' story with the employees and friends that are working with you because nothing could make him happier than to know that the CMP story of innovation and perseverance will continue.