Strategies for Probe to Enable Advanced Packaging

NCCAVS Joint User Group Meeting, 8/21/2024

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Strategies for Probe to Enable Advanced Packaging

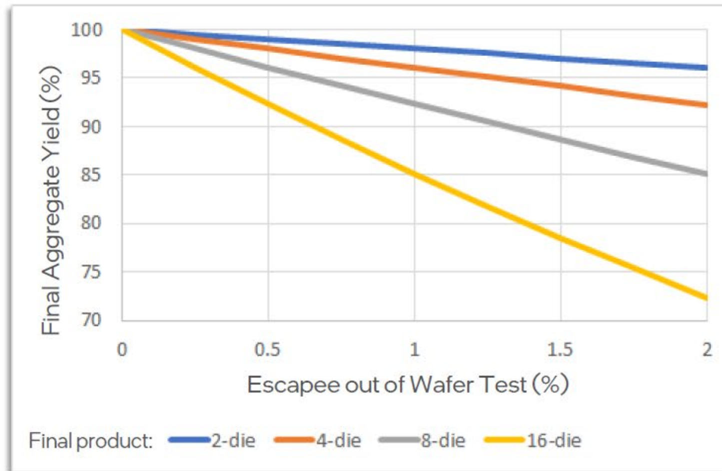
A brief summary to get us started

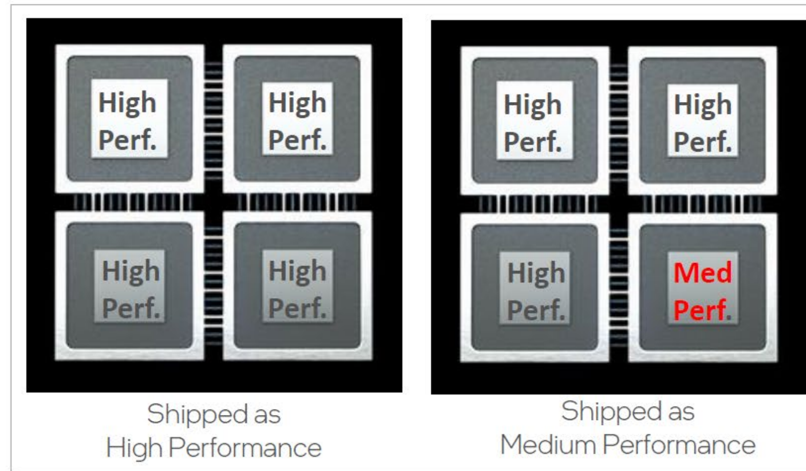
- Wafer probe/sort/test is increasing in importance and test intensity is on the rise
  - Probe card spending as % of semiconductor revenue up from ~0.35% mid-2010s to >0.4% today
- This increase is driven by multiple compounding factors
  - Shifting test content from final test to wafer test
    - Faster time to results, fewer bad die into assembly
  - Advanced packaging (=disaggregation=chiplets=tiles=stacks) composite-yield math is sobering
    - Compels need for test coverage approaching Known-Good-Die into assembly
  - Driving up not only test coverage, but also test complexity (eg, speed, stress) at probe
- Historically, packaging interconnect structures have also served as probe interfaces
  - Works well at flip-chip pitches, but smaller than that causes significant technical+cost challenges
- About FormFactor: broad-based supplier of test & measurement products
  - #1 probe-card market share, engineering probers, cryogenics for quantum computing
  - $700M trailing 12-month revenues, ~2150 employees worldwide

Wafer Test/Probe is a Key Enabler for Advanced Packaging

The "chain" of chiplets is no stronger than its weakest chiplet

Impact to Test from Heterogenous Integration & Die Disaggregation





KGD has historically been associated with yield and the goal of minimizing number of defects escaping wafer test

In addition to yield, die disaggregation demands an accurate prediction of device performance in the final package & system environment

Assembly and Test Technology Development

intel. 21

Source: Advanced Packaging Architectures, Opportunities and Challenges; Hamid Azimi, SEMICON West '21

- Economically viable multi-chiplet products require near-KGD component chiplets
  - This requirement is especially acute as the number of chiplets in the product increases
- Matching of component chiplet performance bins (right) is more subtle, but is also an important factor

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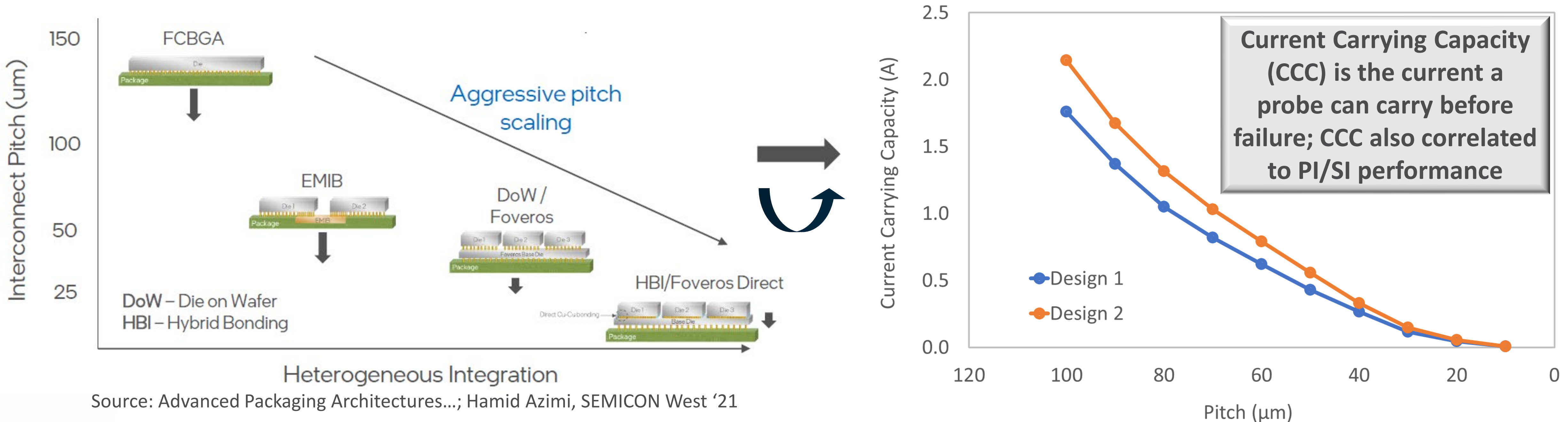
Chiplet-to-Chiplet Interconnect Scaling Poses Challenges for Probe

Probing the assembly interconnects means pitch (and probably performance) reduction



Source: Advanced Packaging Architectures…; Hamid Azimi, SEMICON West '21

- Historically, wafer probe has used the packaging interconnects (eg, flip-chip bumps) to connect to the die
- For a given probe design, geometric scaling generally results in reduced performance, eg, CCC at right
  - Lower CCC = more probe damage (repairs and downtime) and higher power impedance (yield and coverage)
- Potential advantage in decoupling packaging interconnect from probing contacts/interfaces
  - Ex: Dedicated test pads in TSV-packaged HBM DRAM enable one-touchdown parallelism, lowering cost of test

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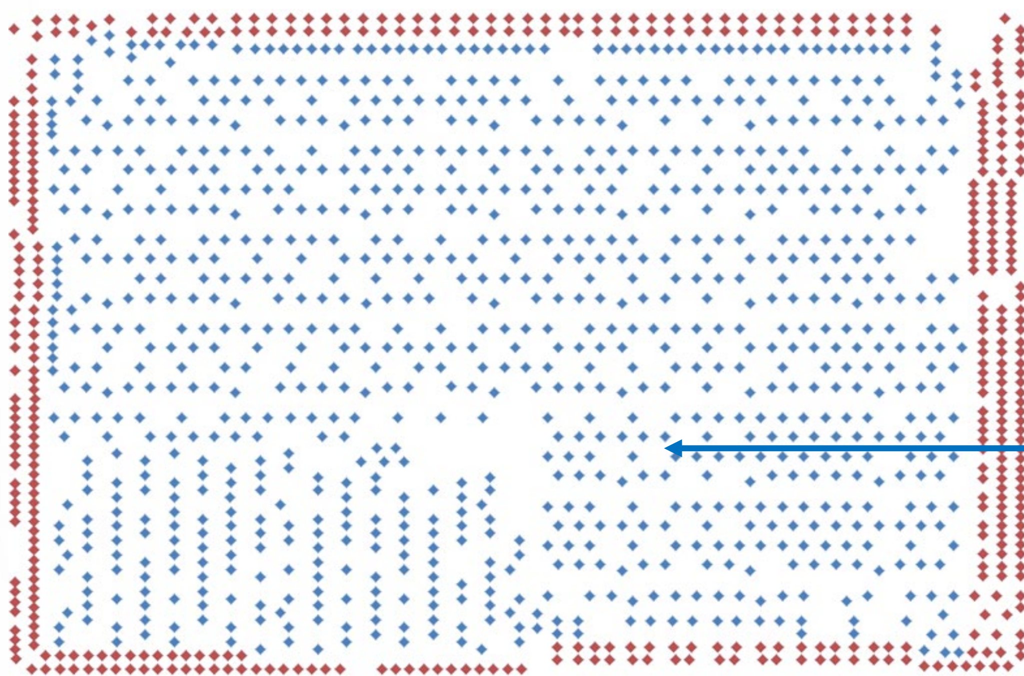
Optimizing Use of Packaging Interconnects - the "Hybrid" Probe Card

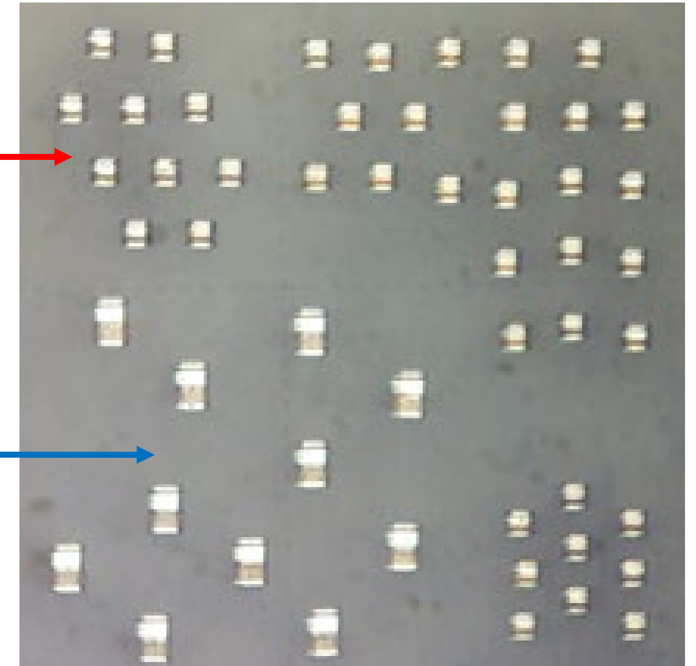
Use different probe designs in different areas of the die to do different jobs



Die Bump Layout

Utilize smaller probes for I/Os at tighter pitch

Utilize larger probes for power and ground with higher CCC requirements



Local Image of Hybrid Probe Tips
(image is small sub-section of probe card)

- Layout of power and ground interconnects are often at larger pitches than the high-density fine-pitch I/Os
  - Hybrid probe cards exploit this, using larger probes with higher CCC on the powers+grounds (where it's needed)
- Benefit: Higher MTBF from less probe damage/repair, better test coverage from lower power impedance
- Variations on this general theme are possible, for example, a single probe that contacts multiple bumps

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Q&A