Improved CMP processes through architecture & design optimization

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Dr. Knut Gottfried

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Outline

- Background
- Example IR imager
- Hybrid bonding
- Reminder ICPT 2024

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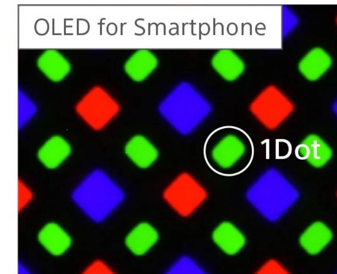
Background

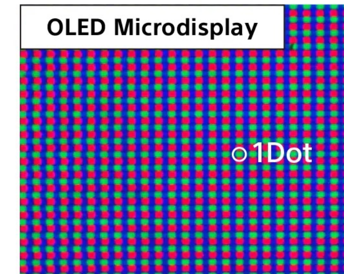
Wafer level integration concepts as needed for:

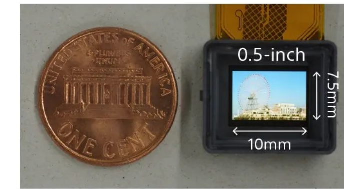
- CMOS imagers
- IR imagers (bolometer)
- Micro displays for VR / AR applications
- Hybrid ICs (combining devices from different technologies)

Fabrication of such devices may require several CMP steps, depending on specific fabrication technology

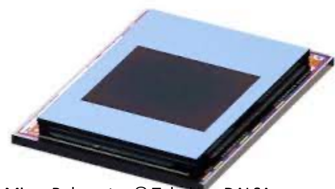
- Oxide / insulator CMP
- Metal CMP (Cu/barrier)
- Backside CMP



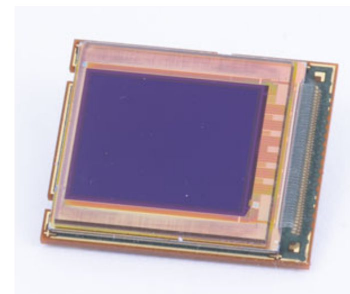




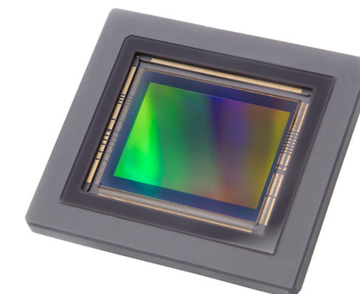
Sony OLED Displays © Sony



Micro Bolometer © Teledyne DALSA



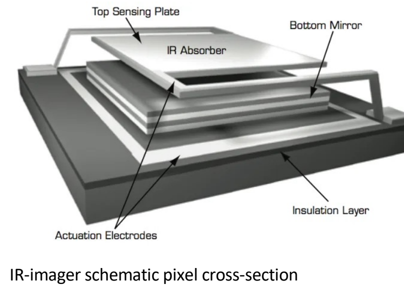
Micro OLED Display © VECTED GmbH



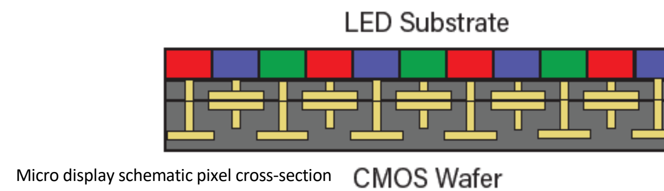
Canon CMOS Image Sensor
13272H x 9176V © Canon

Device characteristics

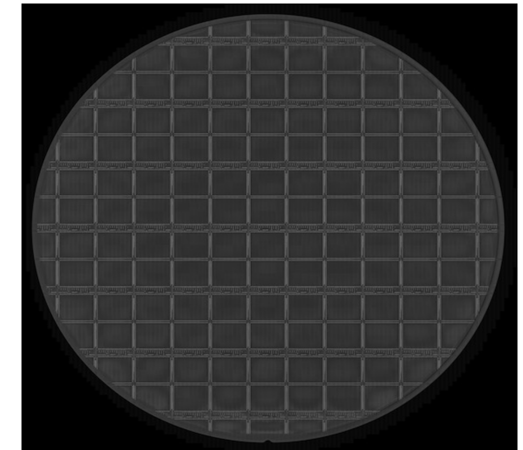
- High vertical integration level (wafer level integration)
  - Integration on-top-of-CMOS (e.g. IR imagers)
  - Hybrid wafer bonding (e.g. micro displays, hybrid ICs)
- Rather large dies – several mm to inch size
- Pixel arrays / pixel areas
  - Pixels size / pitch in lower µm range
  - Very uniform pattern density and size ☺
  - Very uniform pitch ☺
- Surrounding circuitry ☹
- Dicing lanes ☹



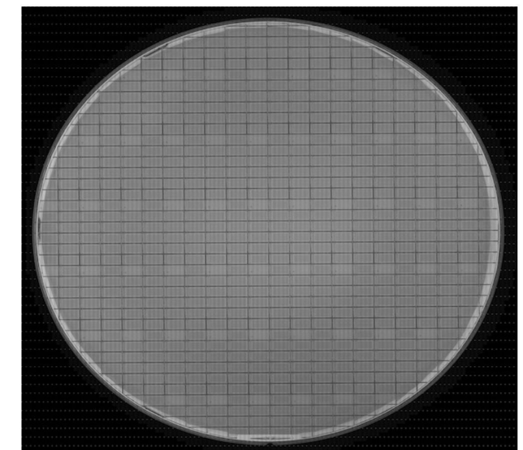
IR-imager schematic pixel cross-section



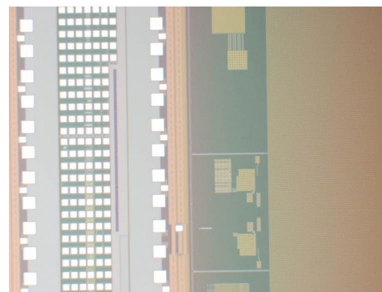
Micro display schematic pixel cross-section


CMOS backplane for IR-mager

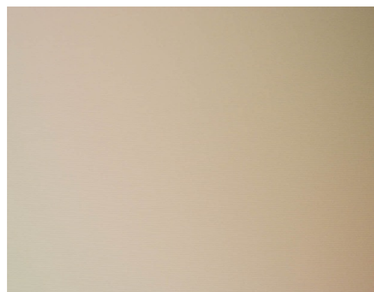
CMOS backplane for micro display fabrication



IR-imager – dicing lane and circuitry



IR-imager – pixel array

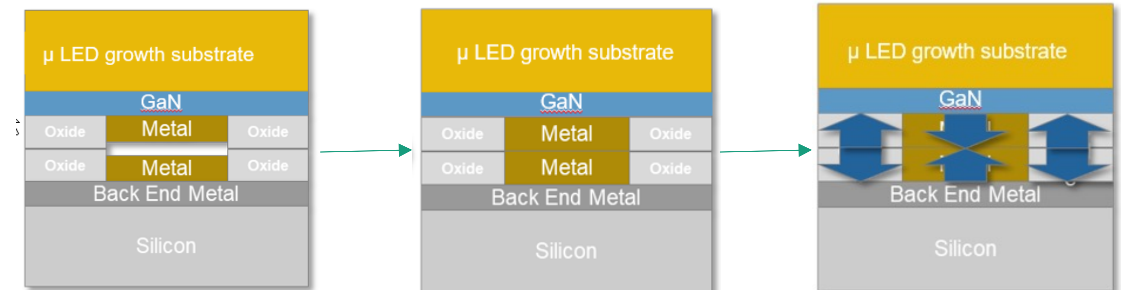


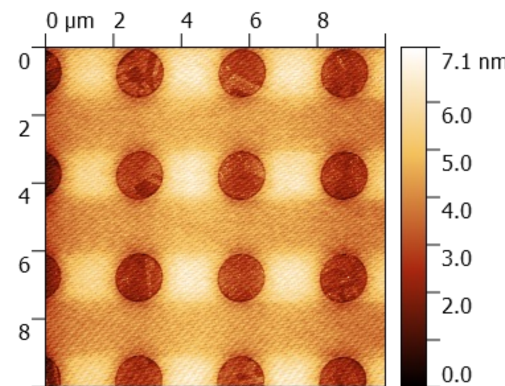
Process requirements

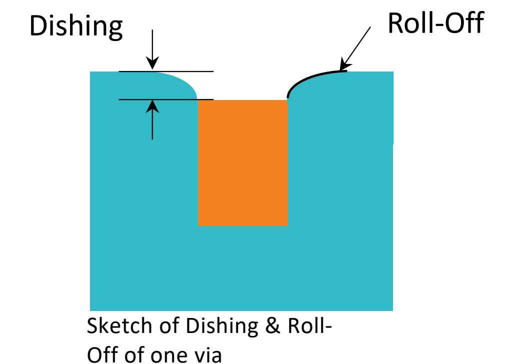
- Good uniformity: within die, within wafer, wtw
- Low remaining topography
- Low roughness

Specific to hybrid bonding applications

- Oxide roughness: same as direct bonding < 0.5 nm
- Oxide rounding: < 1 nm / µm
- Cu roughness in lower nm range
- Dishing: no rule of thumb, depends on via size and temperature budget (typ. 1 nm … 10 nm)
- Low remaining long-range topography (typ. less than 10 nm)
- Trenching: as low as possible (undesired effect)





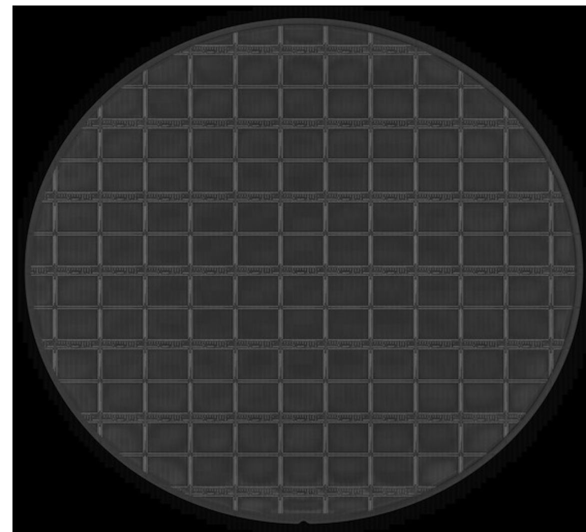


Sketch of Dishing & Roll-Off of one via

What's the meaning for CMP?

- Perfect process control
  - Process parameters / process window
  - Endpoint
  - Consumables
- Process strategy
  - Over polish
  - Selective / non-selective
  - Dishing – protrusion – dishing
- Fast and reliable inline metrology

- Design (layout, architecture) adaption & optimization
  - Design for functionality
  - **Design for fabrication**



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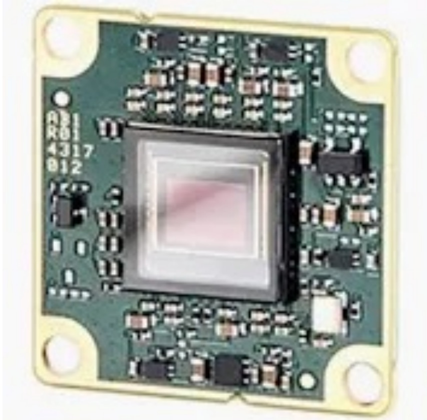
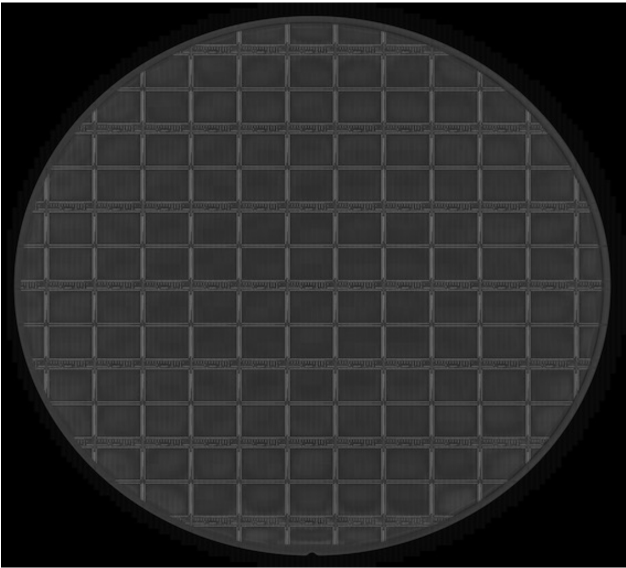
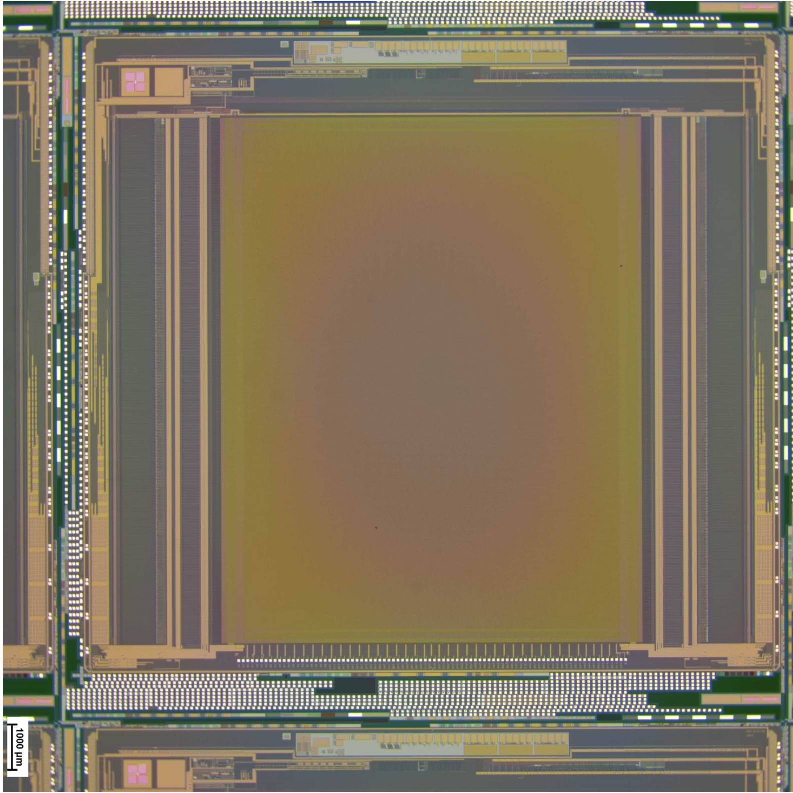
Example IR-Imager







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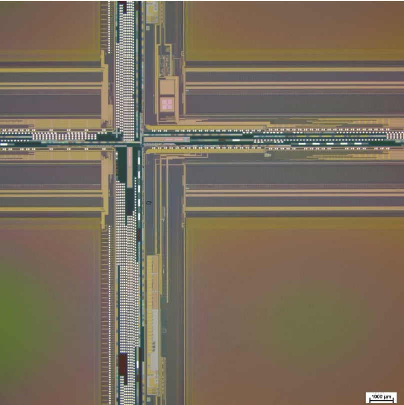
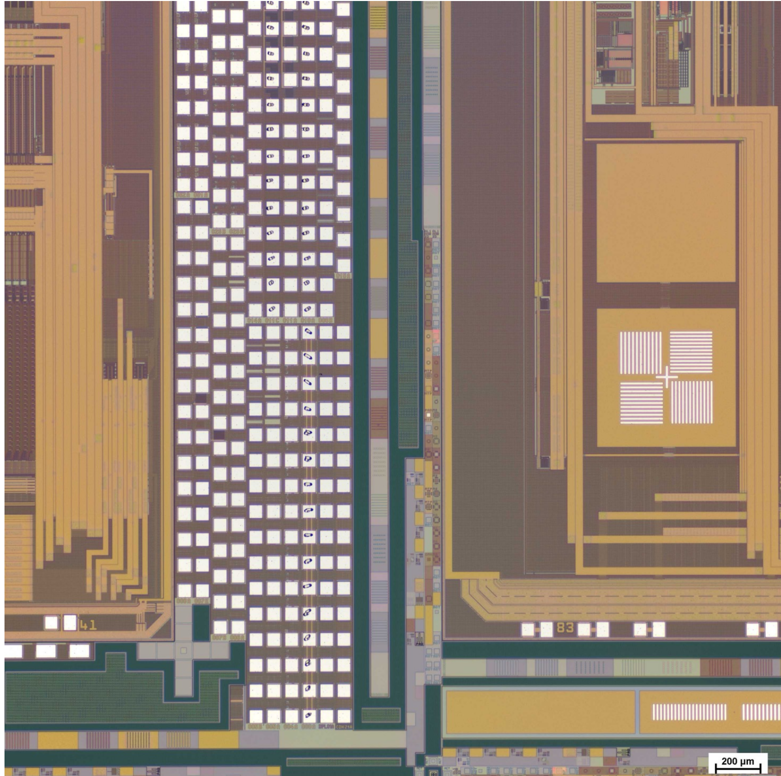
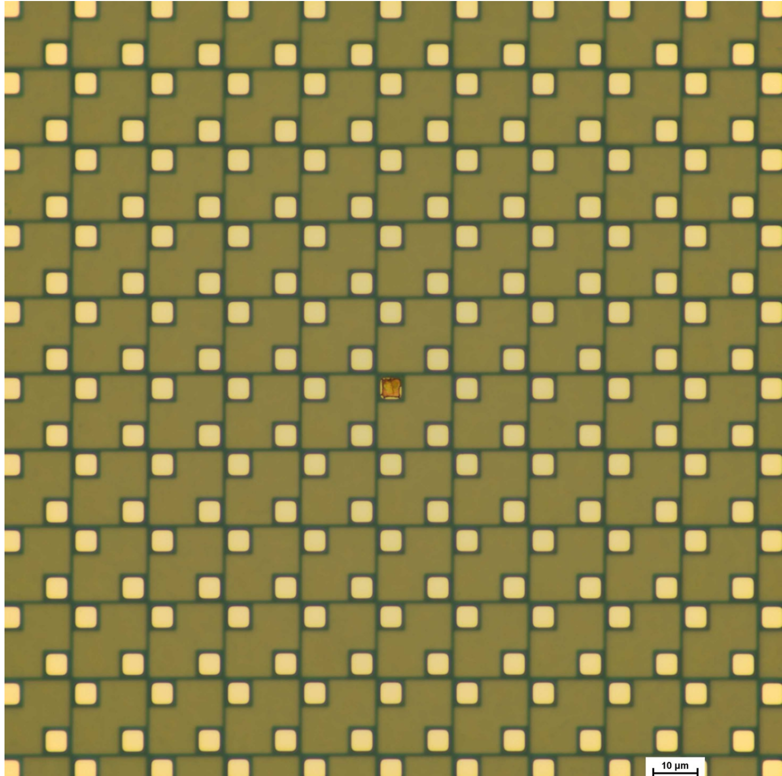
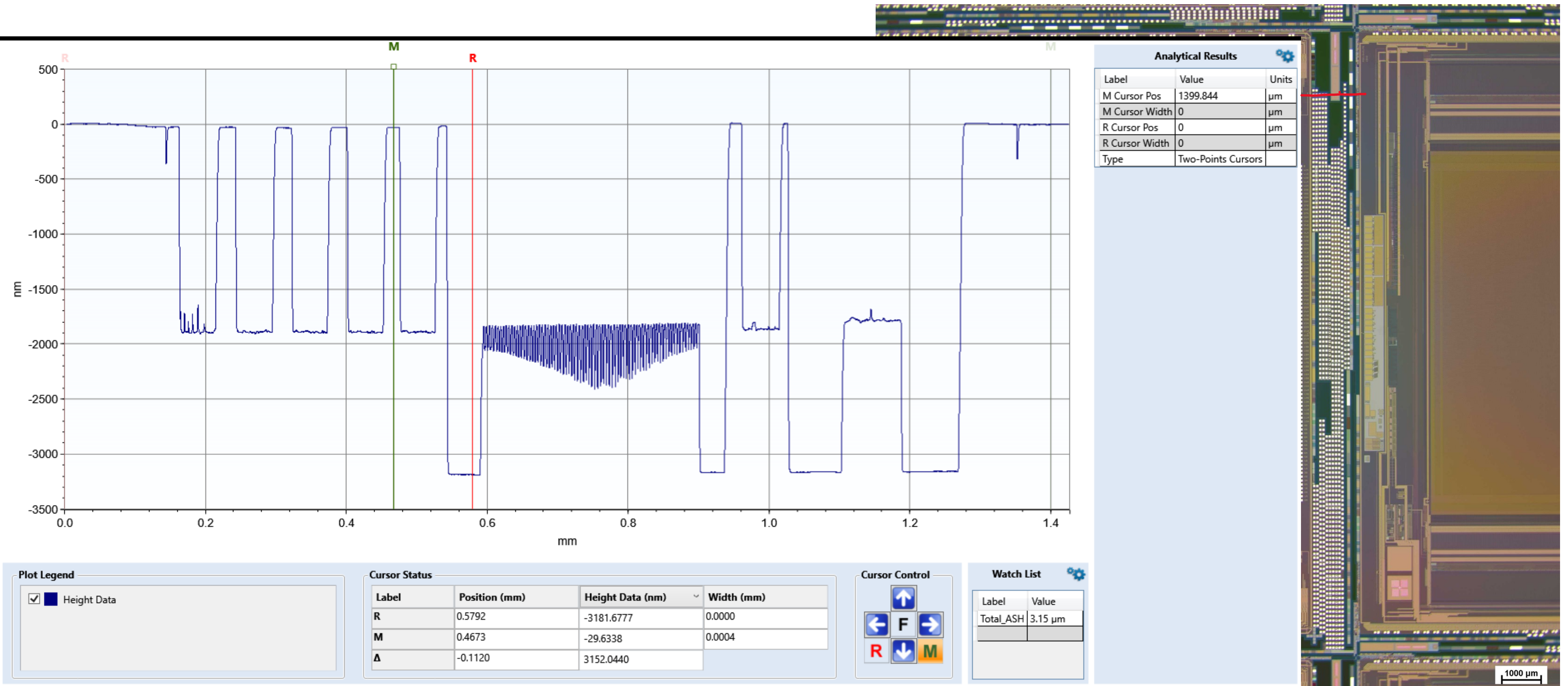
Sensor design – different feature sizes and different pattern density







Profile across IO-pads and dicing lane – starting situation



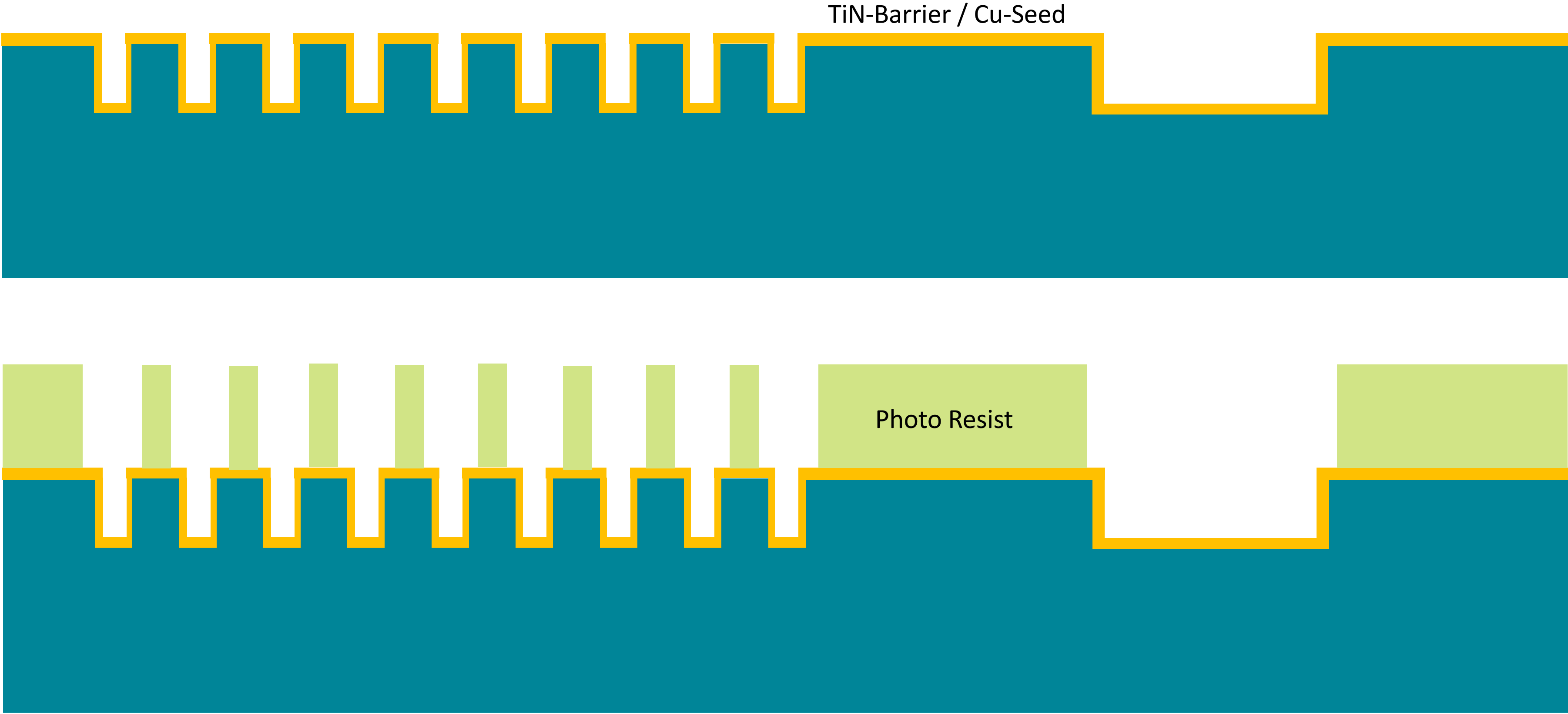
Common fabrication approach

- Ti/TiN-Barrier / Cu-Seed deposition by PVD
- Full wafer plating – Cu thickness according maximum pattern depth
- Cu / Barrier CMP

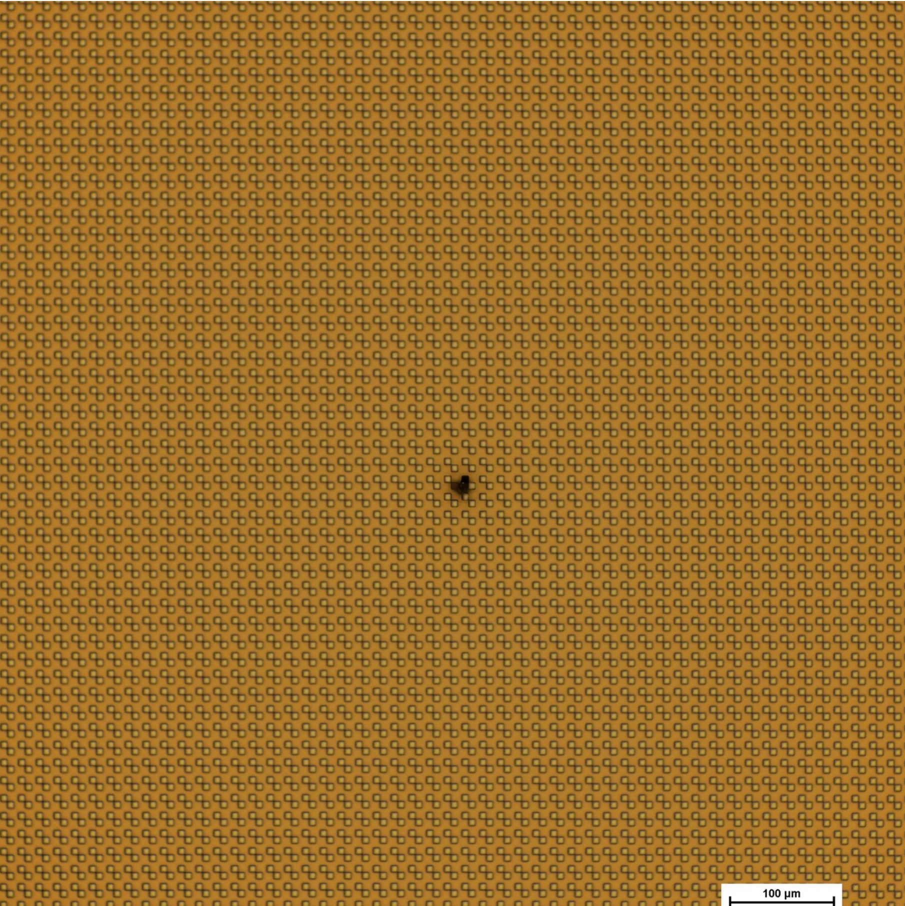
Disadvantages

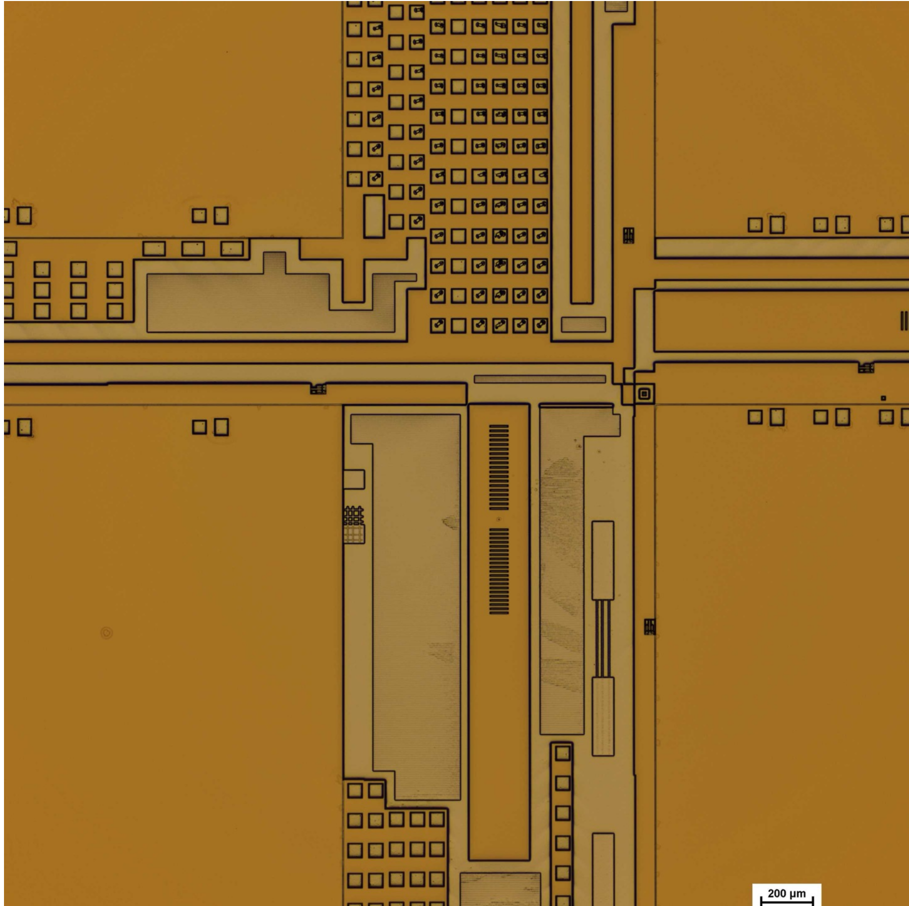
- Thick copper
  - Long polish time
  - Uniformity issues

Selective plating / pattern plating

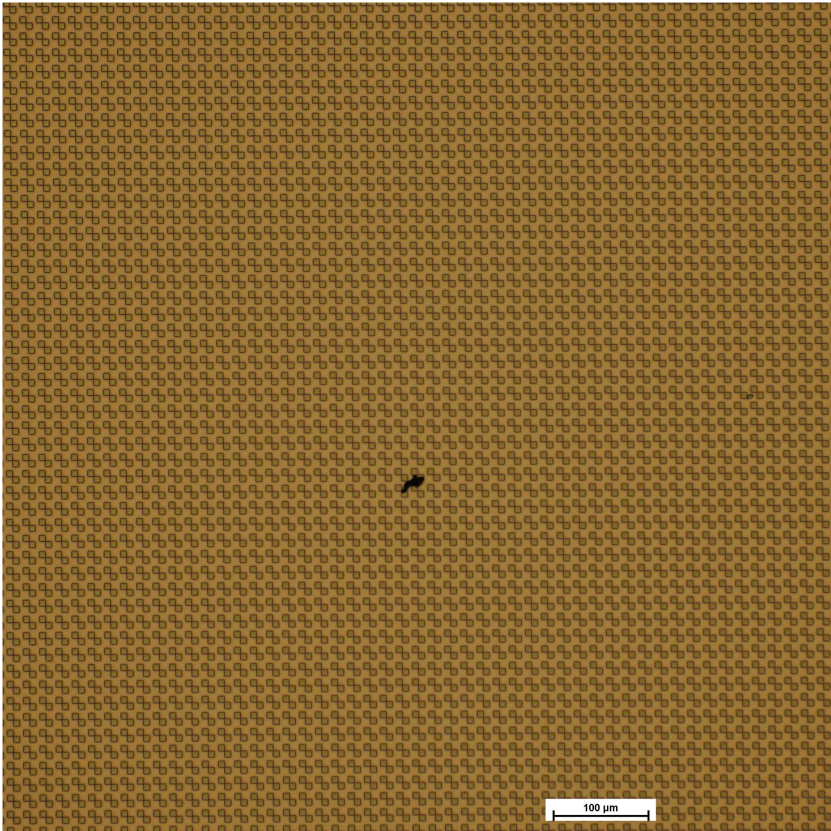


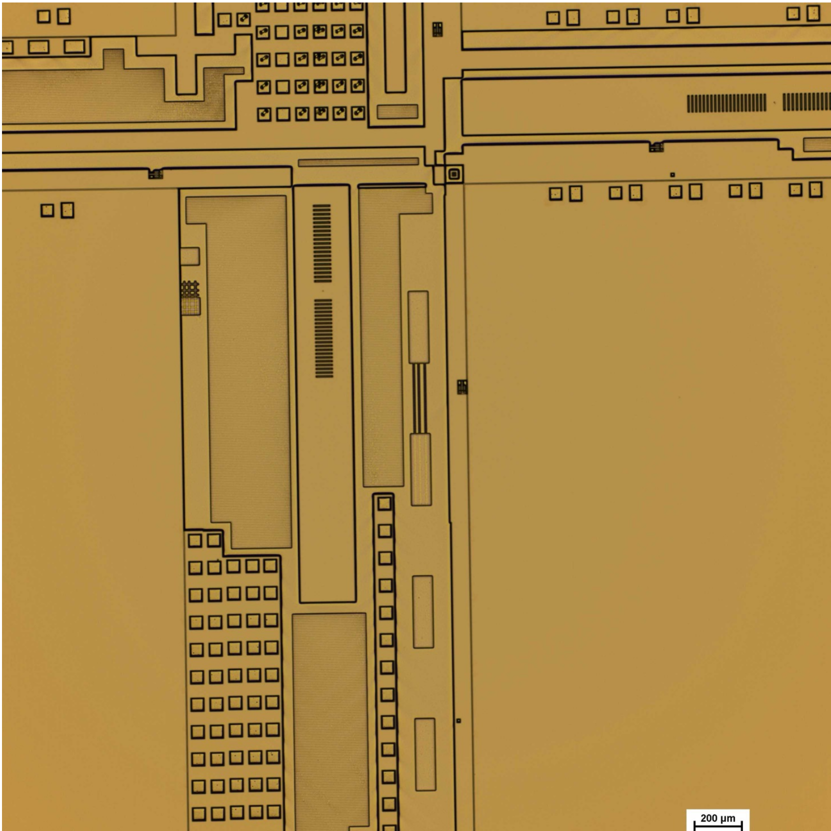
Wafer after selective ECD with resist in place



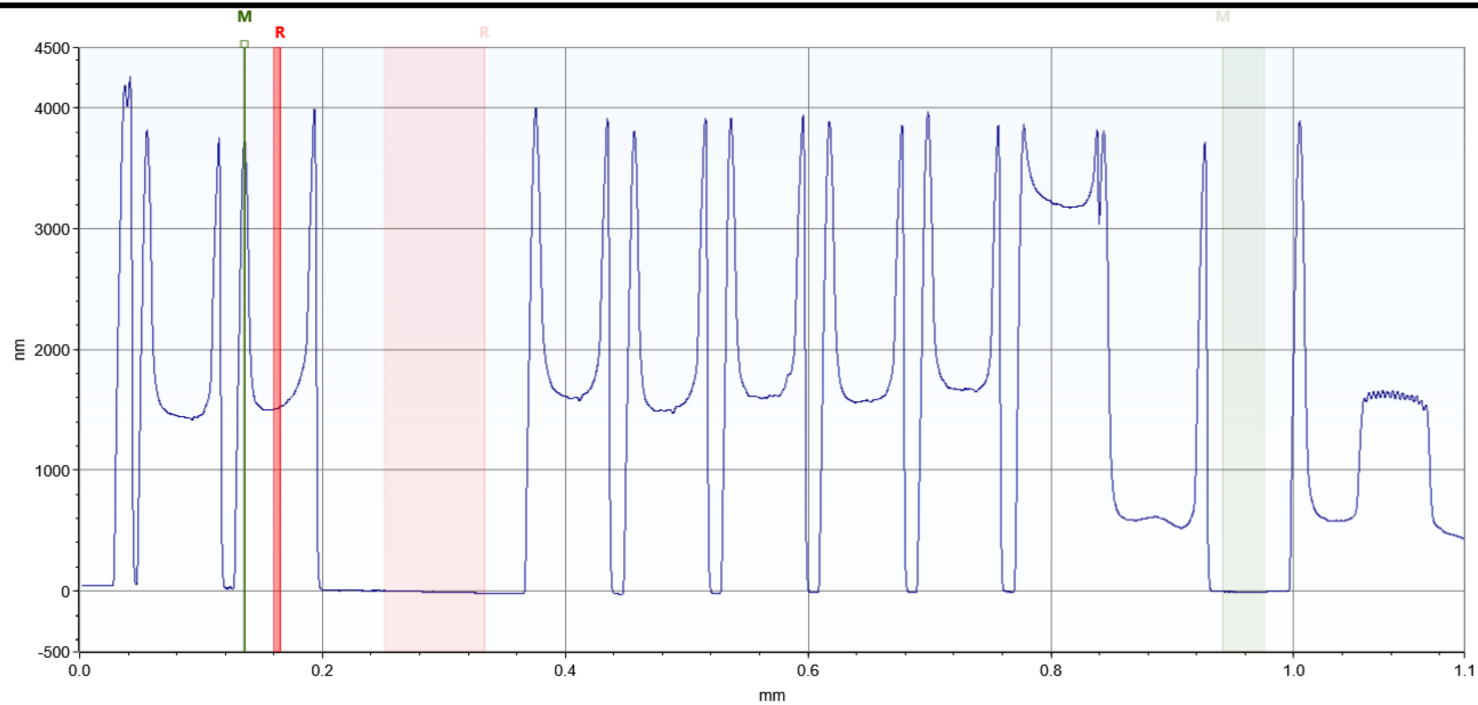


Wafer after selective ECD and resist removal





Metal profile after selective ECD and resist removal



Analytical Results

Label	Value	Units
M Cursor Pos	0.942	mm
M Cursor Width	0.034	mm
R Cursor Pos	0.333	mm
R Cursor Width	-0.082	mm
Type	Two-Points Cursors	

Plot Legend

☑ Height Data

Cursor Status

Label	Position (mm)	Height Data (nm)	Width (mm)
R	0.1651	1519.3616	-0.0053
M	0.1361	3680.6542	-0.0012
Δ	-0.0290	2161.2926	

Cursor Control

F R M

Watch List

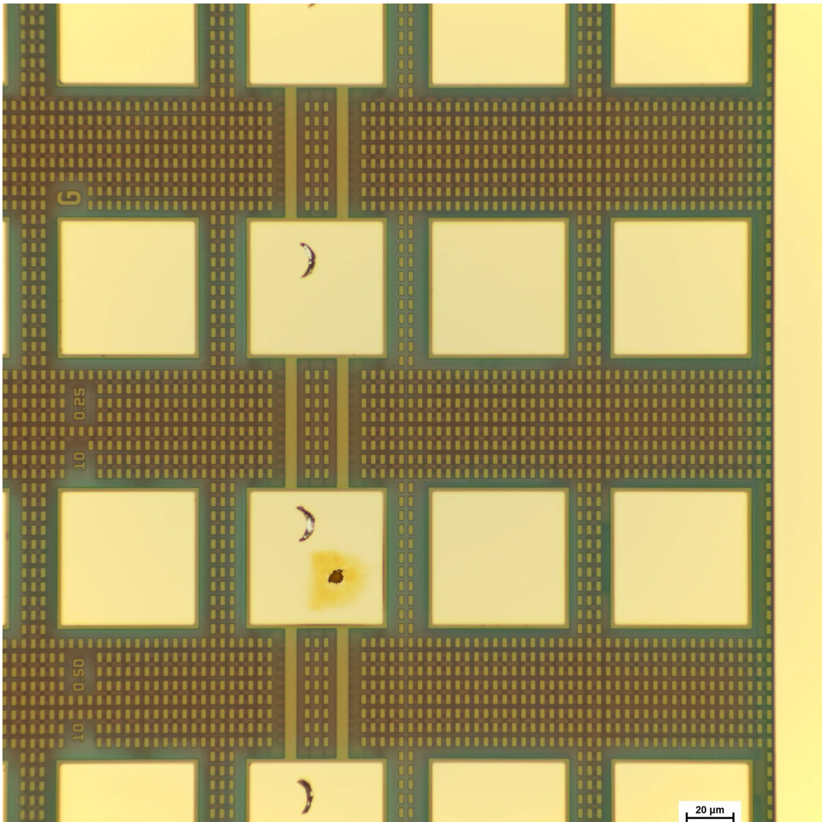
Label	Value
Total_ASH	2.16 µm

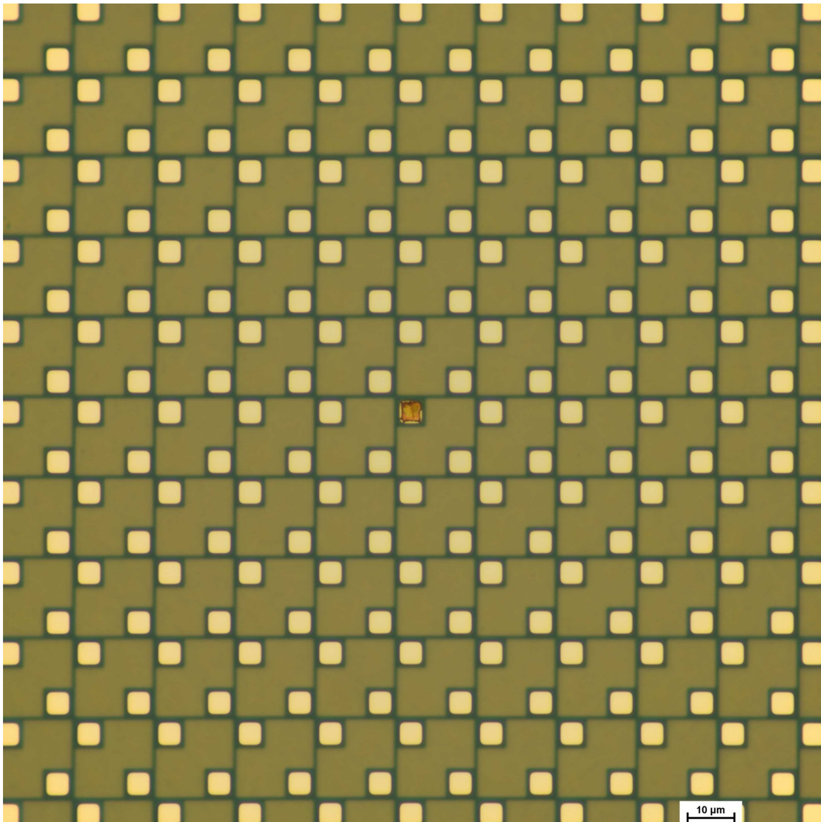
CMP process

- Axus Surface polisher with Crystal polish head
- Alkaline Cu-slurry with app. 10% H_2O_2 content (commodity HV slurry)
- Alkaline barrier slurry with tunable selectivity (commodity HV slurry)
- Hard pad (comparable to IC1000 class)
- Pad conditioner with “new grade diamonds”

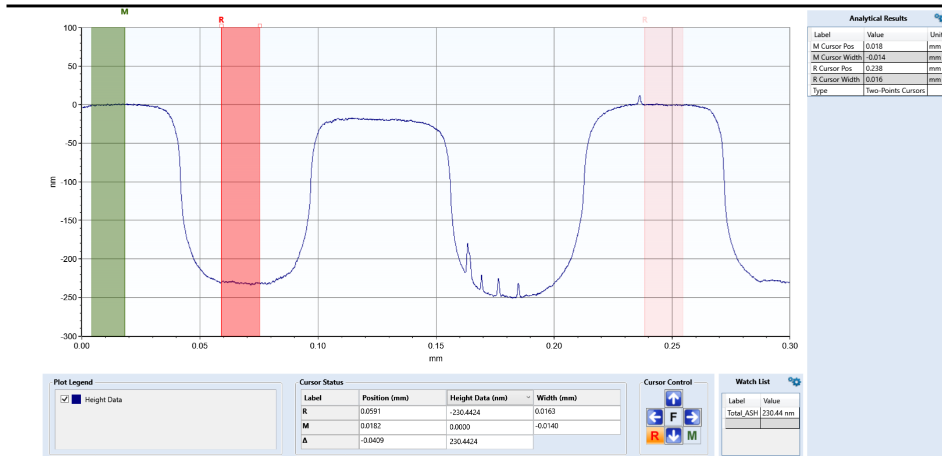
- Brush clean (G&P412R) using DI-water and alkaline post-CMP cleaning chemistry

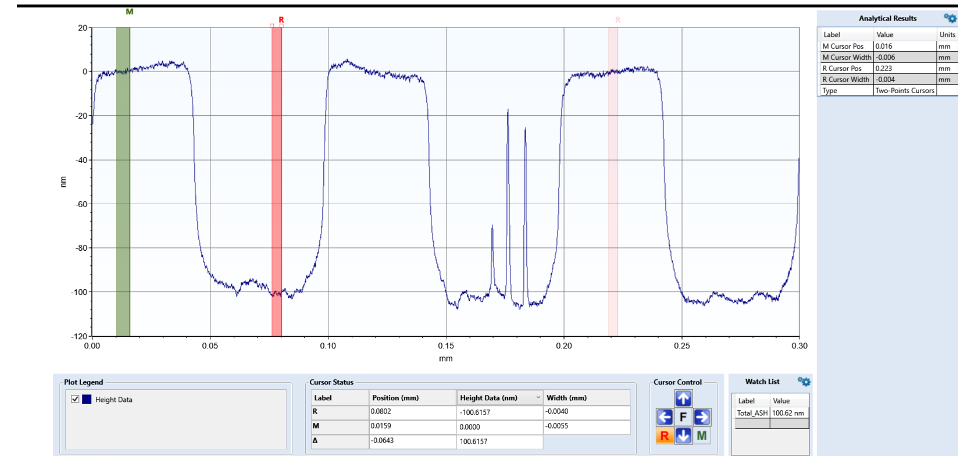
Wafer after Cu and barrier CMP

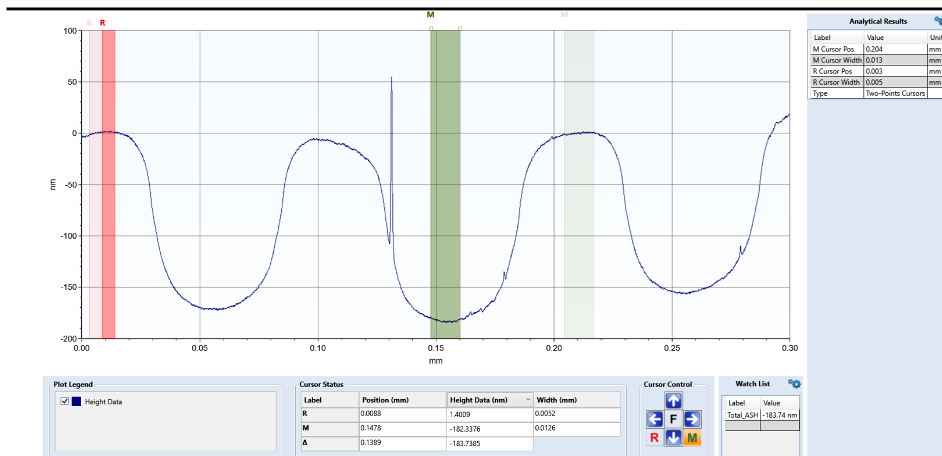




Metal profile IO-pads after CMP







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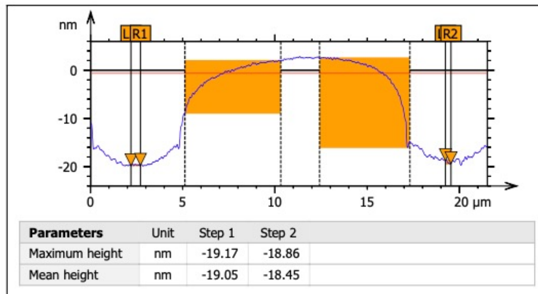
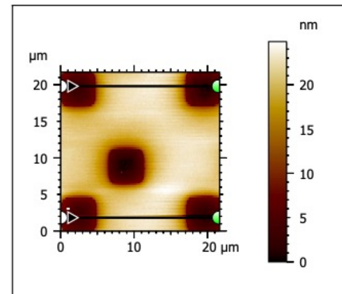
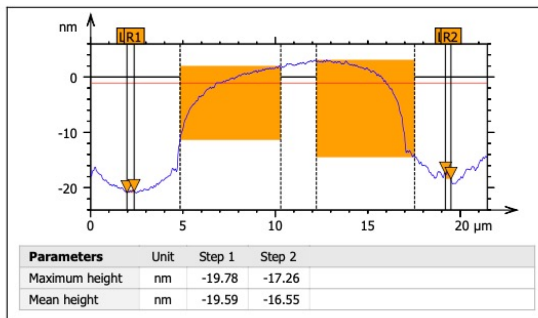
Dishing in vias



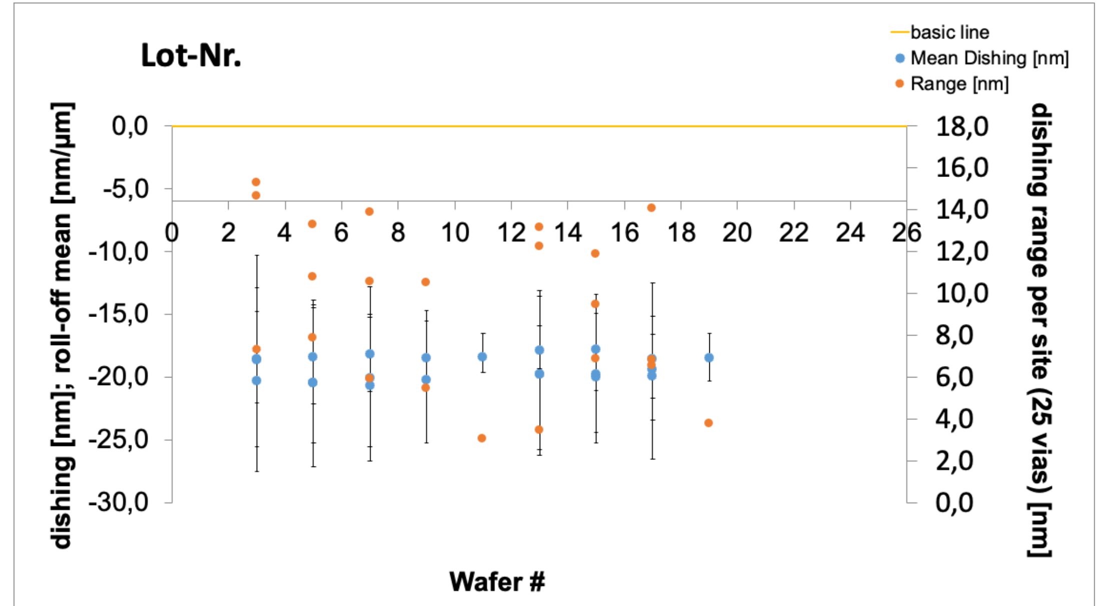
Parameters	Unit	Step 1	Step 2
Maximum height	nm	-19.17	-18.86
Mean height	nm	-19.05	-18.45





Parameters	Unit	Step 1	Step 2
Maximum height	nm	-19.78	-17.26
Mean height	nm	-19.59	-16.55

Parameters	Value	Unit
Mean height - Mean	-18.75	nm
Mean height - Std dev	0.3014	nm
Mean height - Min	-19.05	nm
Mean height - Max	-18.45	nm
Mean height - Range	0.6027	nm
Mean height - Mean	-18.07	nm
Mean height - Std dev	1.523	nm
Mean height - Min	-19.59	nm
Mean height - Max	-16.55	nm
Mean height - Range	3.045	nm



Statistical summary						
Parameters	Mean	Std dev	Min	Max	Range	Unit
Mean height	-18.41	1.149	-19.59	-16.55	3.045	nm

Summary pattern plating / selective plating for IR-imagers

- Over-all polish time: app. **3:30 minutes**
  - For comparison - polish time for a fully plated wafer of the same product: **9:50 minutes**

- **60% reduction of CMP process time**
  - Significant cost savings
  - Better uniformity
  - Less topography issues

- Additional efforts for this approach
  - Photomask
  - Litho step (1:1 lithography)
  - Resist strip

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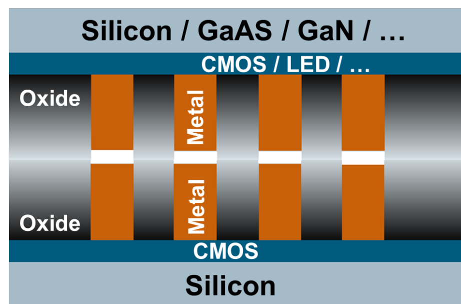
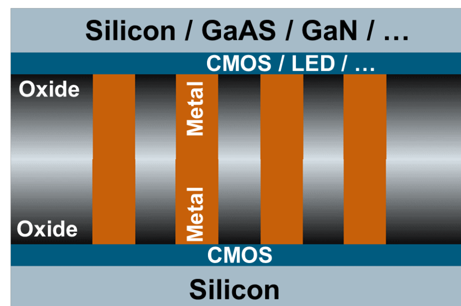
Example hybrid bonding

Oxide to Oxide bond at room temperature



Heat closes dishing gap (metal CTE > Oxide CTE)



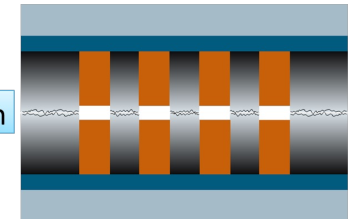
Critical parameters for bonding

- Roughness Oxide
- Dishing
- Erosion
- Topography (from underlying layers)

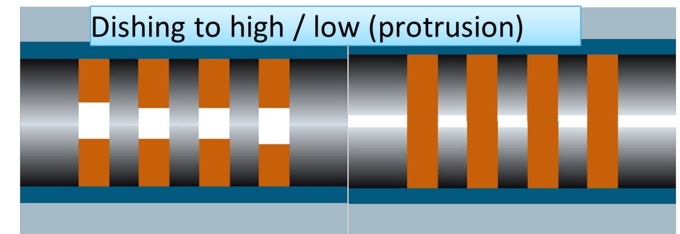
These parameters have to be measured during processing in an adequate way to increase homogeneity, quality, yield, …

Failure modes, which prevent bonding

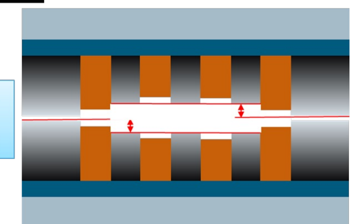
Roughness to high



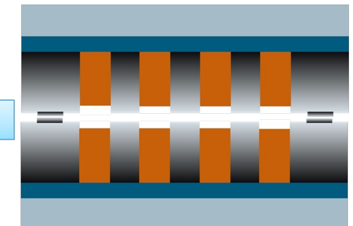
Dishing to high / low (protrusion)



Erosion (higher CMP rate at higher pattern density)

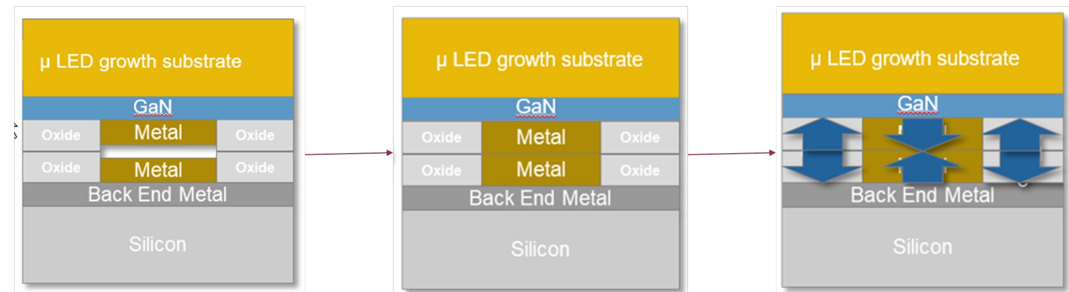


Other topography



Hybrid bonding – process requirements

- Good uniformity: within die, within wafer, wtw
- Low remaining topography
- Low roughness



Specific to hybrid bonding applications

- Oxide roughness: same as direct bonding < 0.5 nm
- Oxide rounding: < 1 nm / µm
- Cu roughness in lower nm range
- Dishing: no rule of thumb, depends on via size (Cu-volume) and temperature budget (typ. 1 nm … 10 nm)
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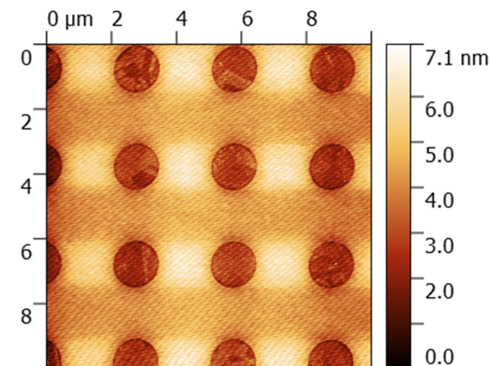
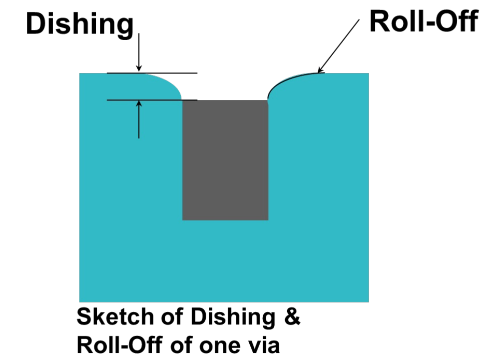
- Trenching: as low as possible (undesired effect)





Sketch of Dishing & Roll-Off of one via

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How to achieve these requirements?

- Most elegant: the topmost layer (hybrid bond layer) is already perfect for hybrid bonding
  - No topography, even in dicing lanes
  - Very uniform pattern size and pattern distribution

- Reality
  - Last layer has different metal patterns with different pattern sizes
  - Still topography in 10th of nanometer scale from underlying layers and dicing streets

- Common workaround: adding another oxide layer(s) with embedded barrier and Cu
  - Oxide layer and CMP will help to eliminate any remaining topography from lower layers and dicing streets
  - Metal patterns in this oxide layer can be designed to adopt pattern size and pattern distribution
  - Downside - additional efforts, such as photo masks, litho, oxide patterning, resist stripping, CMP

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ICPT 2024 – only 7 weeks to go!

Early bird rate ends on September 1! It saves you 100 Euro!

Think about! German beer is not as cheap as it was 5 years ago!

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ICPT 2024 is running from Tuesday to Friday!

- Tutorial Session on Tuesday, Oct 15
- Regular conference from Wednesday, Oct 16 until Friday, Oct 18

ICPT 2024 - Wiesbaden, October 15-18, 2024

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ICPT 2024 – the venue: Kurhaus Wiesbaden (spa / cure house)

ICPT 2024 – the conference room

Depending on table/chair layout up to 1350 persons

We are looking forward seeing you in at ICPT 2024 in Wiesbaden, Germany!

Thank you for your attention!

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