SiC CMP – A Process Perspective

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CMPUG Spring Meeting
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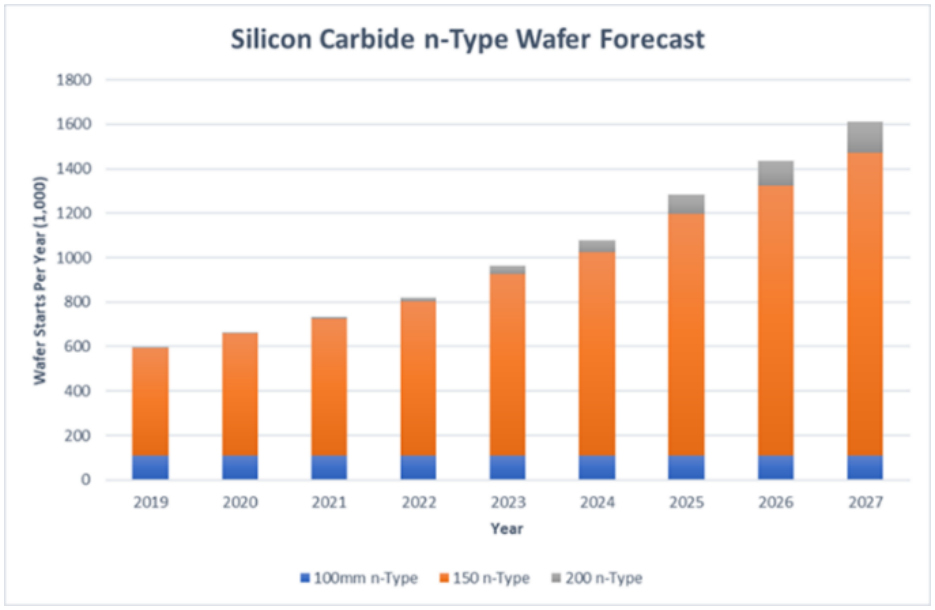
SiC Market Snapshot 2024Q2

SiC demand continues to grow … but less quickly than past 3 years

Growth is Driven by 3 Very Different End Markets

- Power Devices (MOSFETs & diodes)
  - Steady growth in power applications (motors drivers, etc.)
  - Strong adoption for green energy management (wind, solar)
- EV - Power inverters for drive train and supercharging stations
  - Was feverish for >3 years, partially driven by hype
  - Consumer acceptance of EV is not as strong as expected
- Data centers and 5G infrastructure – Gaining strength



SiC Substrate Demand by Year (2023 Techcet Report)

Pace of device market growth is constrained by SiC wafer supply

- Extremely hard and chemically inert
- Long process times for nearly every process (saw, grind, polish)
- Previous experience with Si or III-V materials does not transfer easily
- Most development teams need more process expertise
- Many pieces of process equipment require redesign for SiC

EV Market

RECENT EV TRENDS

- Growing % of new vehicles are EV, but growth is not as fast as was predicted for past 3 years
- Consumer acceptance is lower than expected
- Charging and range issues frustrate drivers during harsh winter conditions
- Used EV market is soft

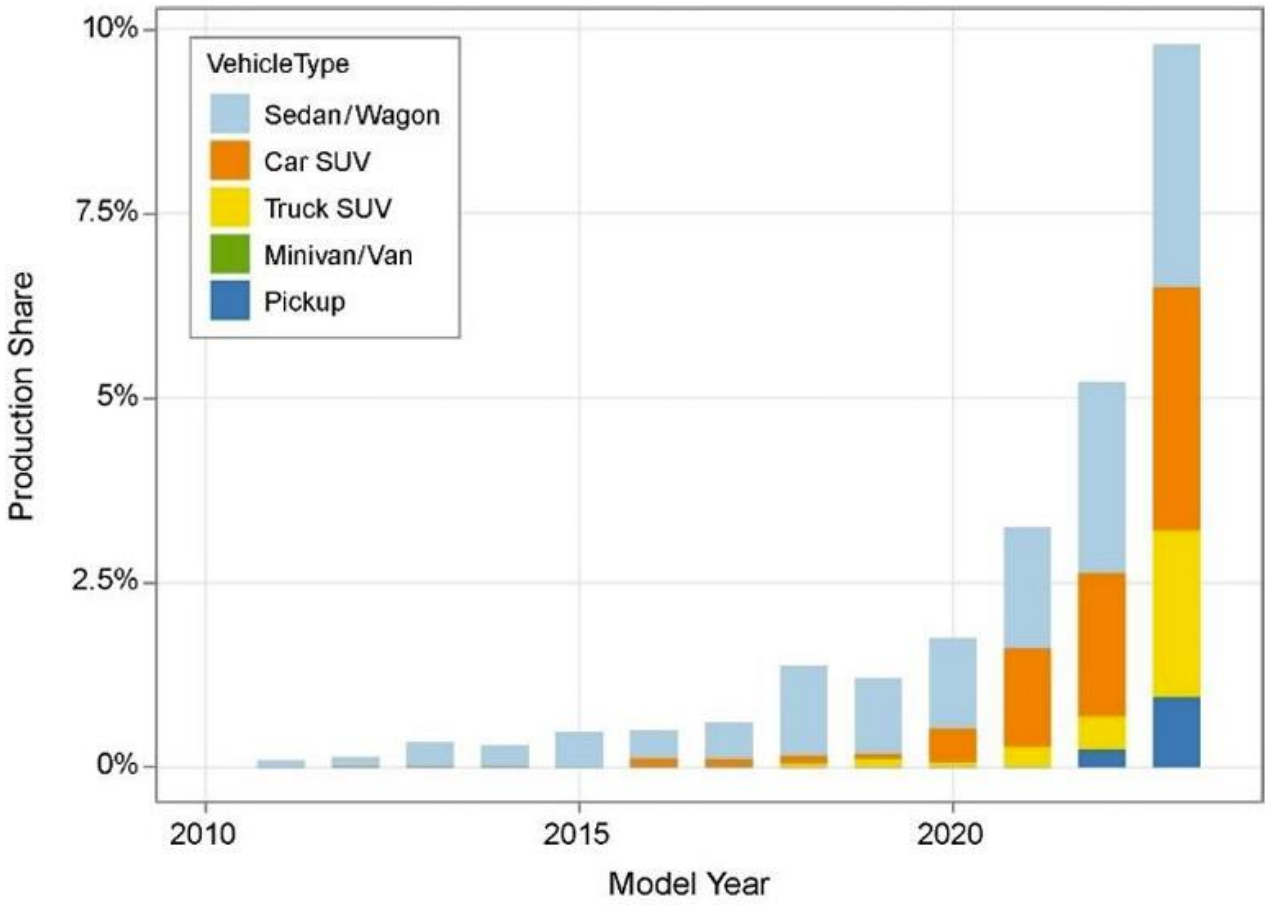
CNN Business Markets Tech Media Calculators Videos

Hertz is selling 20,000 electric vehicles to buy gasoline cars instead

By Peter Valdes-Dapena, CNN
3 minute read · Published 1:11 PM EST, Thu January 11, 2024

CNN Headline
Jan 11, 2024

Market share approaching 10%



2023 EPA Automotive Trends Report

So the SiC sky is falling … Right??

NO!!

The linkage between EV growth and the fate of SiC has been forged more from bandwagon politics and oversimplification than sound technical reasoning.

Numerous other applications and markets can benefit from SiC device performance.

Most SiC wafer suppliers can use a little breathing room to catch up on ramp plans.

Qualification in some of these markets will be easier (and cheaper) than meeting automotive requirements … and now they might have a chance to get a share of the allocation of SiC devices.

Source: iStock photos

Silicon versus Silicon Carbide

Silicon

Material Properties
- Hard and Brittle
- Low Thermal Conductivity
- Easily Oxidized, Chemically Active

Growth
- Inexpensive process, long crystals
- Liquid phase growth
- Small seeds
- High Stacking Fault Energy – Low Defects

Wafer Fabrication
- Thick Wafers (>650um)
- Damage Easily Removed
- CMP Uses Colloidal Slurries, Can Recirculate
- High CMP Removal Rates
- Consumable Costs Low

Silicon Carbide

Material Properties
- *3X Harder* and Brittle
- High Thermal Conductivity
- Difficult to Oxidize, Chemically Inert

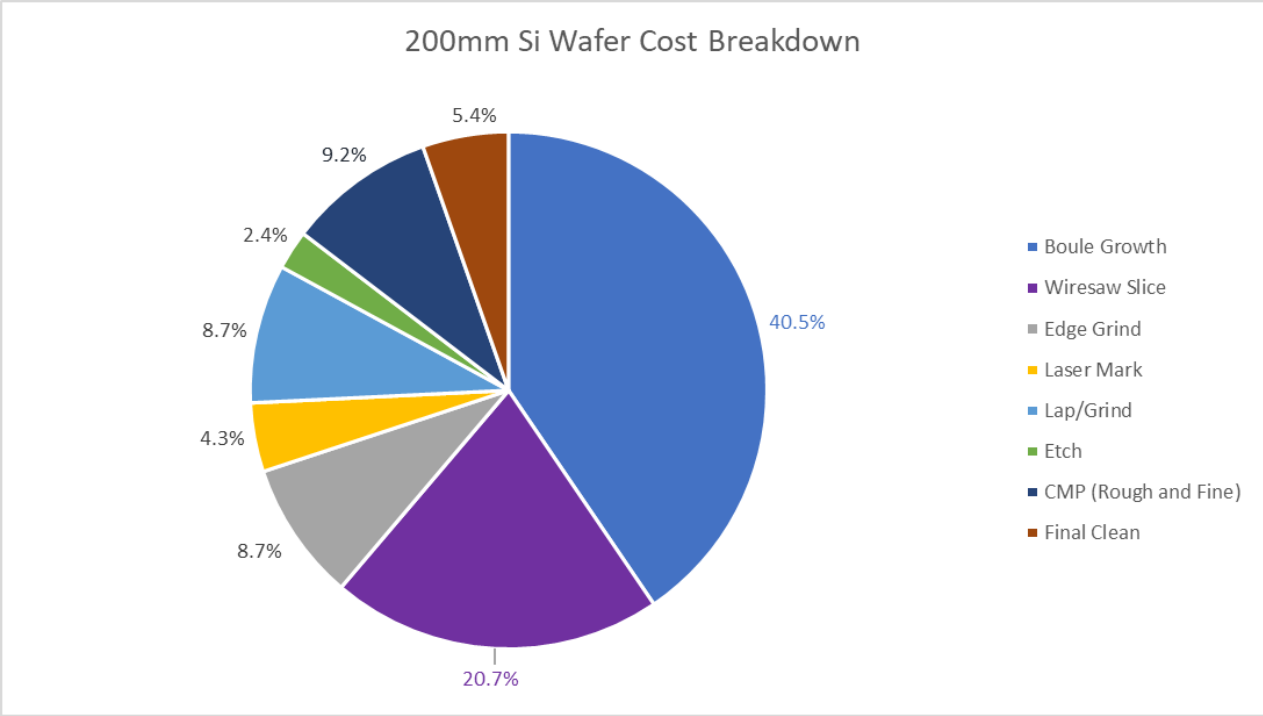
Growth
- Expensive process, short crystals
- Sublimation vapor transport
- Large seeds
- Low Stacking Fault Energy – High Defects

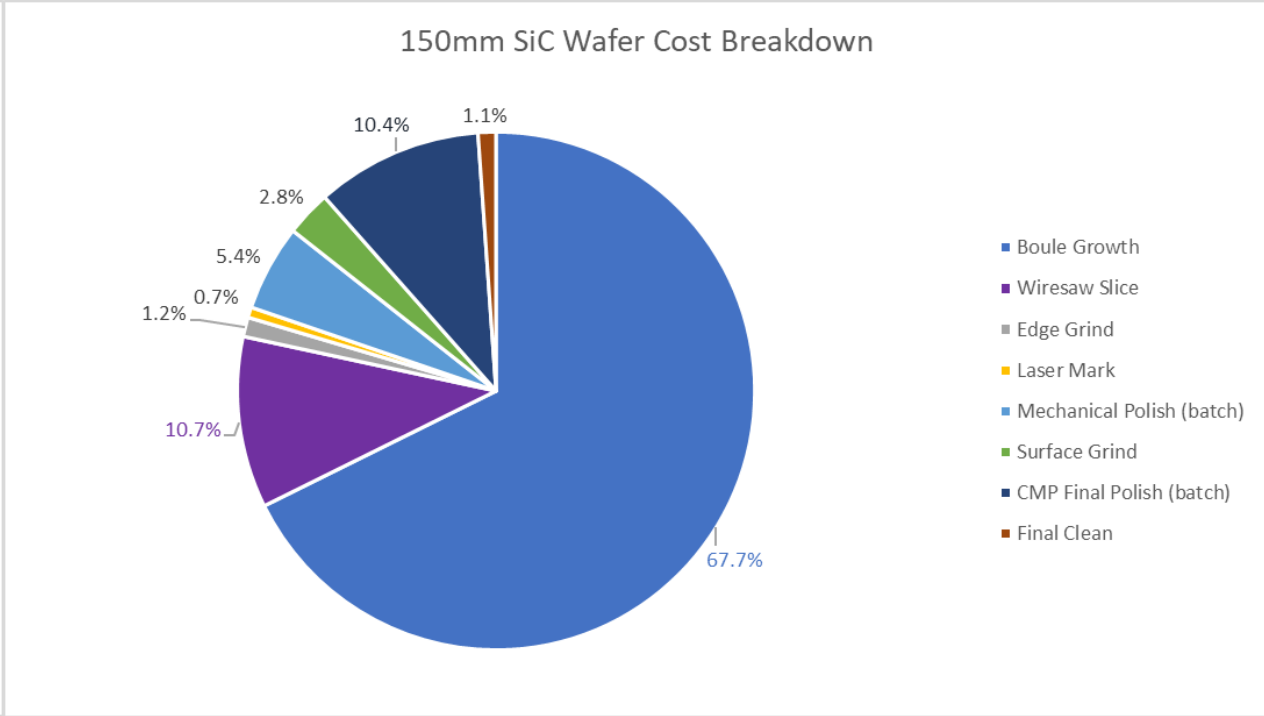
Wafer Fabrication
- Thin Wafers (<375um)
- Damage Difficult to Remove
- CMP Uses Unique, Non-Colloidal Slurries
- Low CMP Removal Rates
- Consumable Costs High

Silicon Wafer Fabrication Driven to Minimize Costs

Silicon Carbide Fabrication Driven to Maximize Good Wafers Per Ingot

Silicon vs. SiC Cost Breakdown

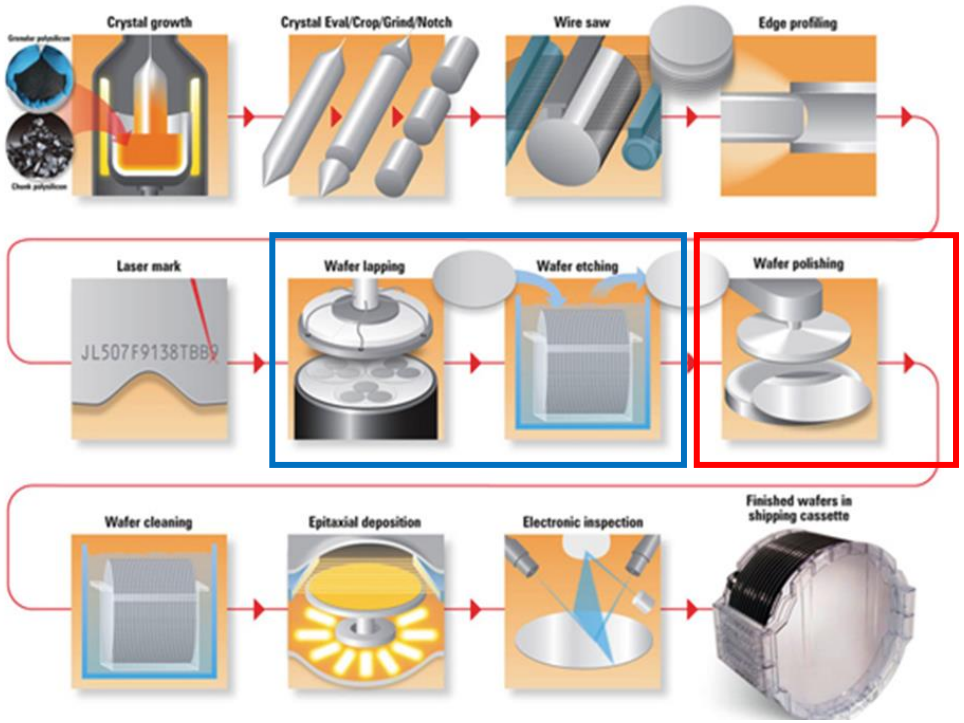


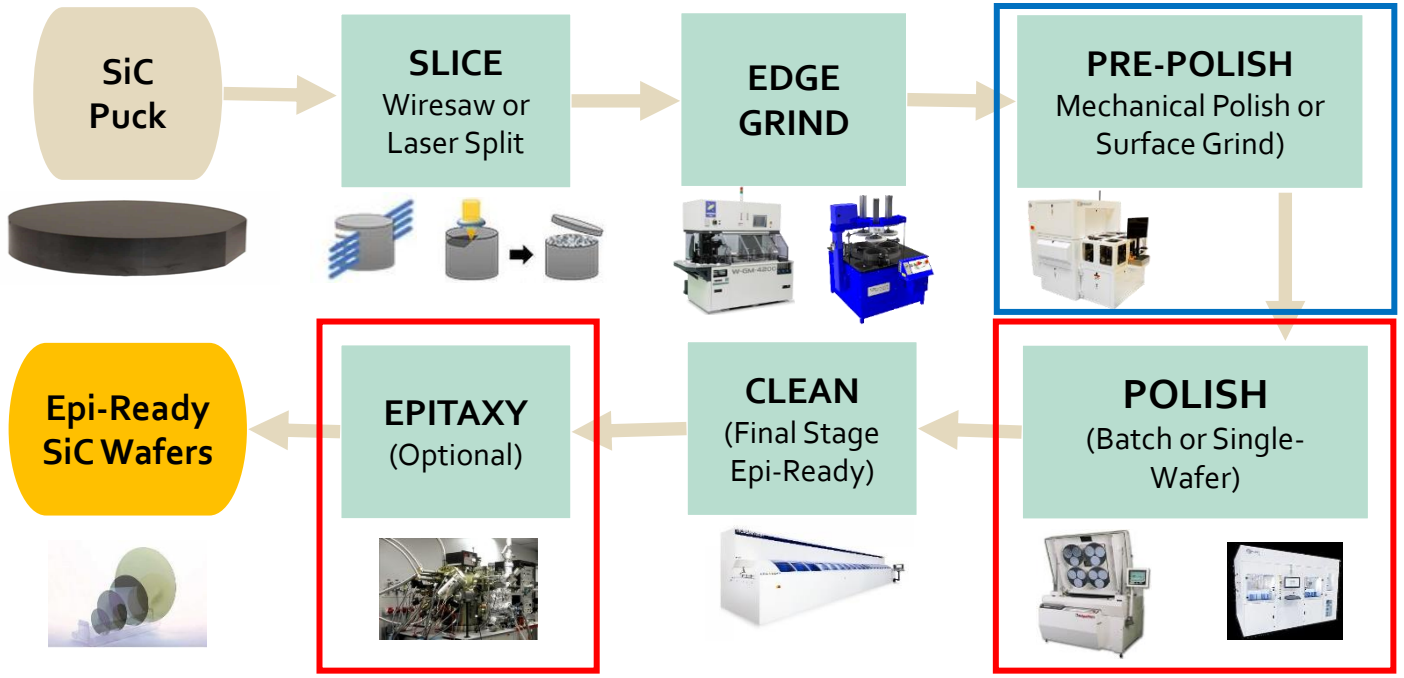


- **$50-$60 Wafer Sales Price**
- 50% Margin, Means About $3 for CMP
- Less drive to reduce costs
- Cost reduction routes:
  - Slicing is largest unit process cost after growth
  - All other processes are comparable cost

- **$900-$1000 Wafer Sales Price – *but market is pushing to cut this in half***
- 50% Margin Means $45-$50 for CMP
- Major drive to reduce costs:
  - Growth dominates cost – reduce kerf!
  - In wafering, CMP and Slicing dominate – *more can be spent on pre-polish steps if it reduces the CMP time*

Wafer Fabrication Processes





- Silicon wafer fabrication flows are very mature and stable
  - Far less variation – requalification costs overwhelm potential improvements
  - Prior to planarization steps, CMP appears only after lapping/etching

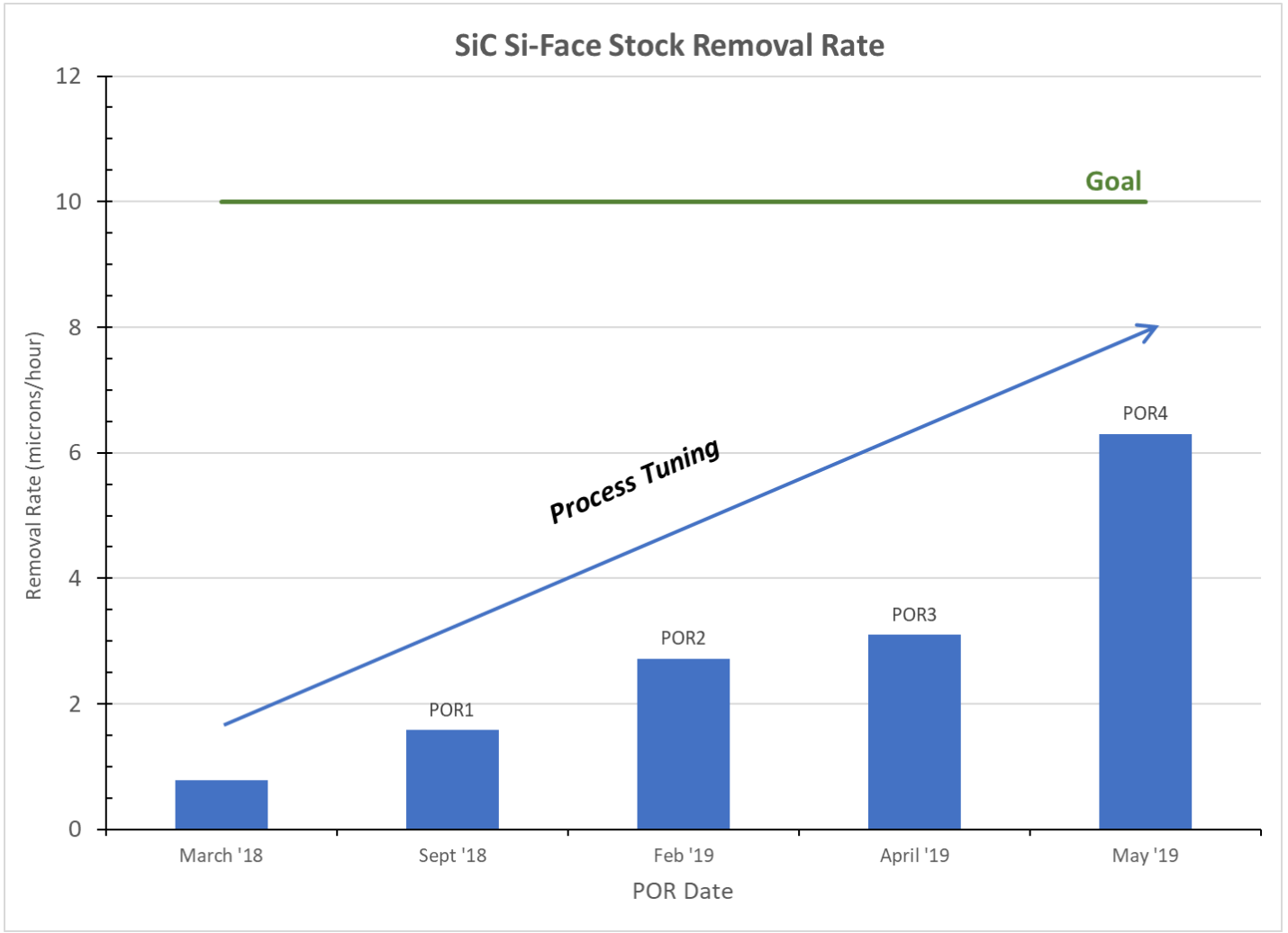
- SiC wafer fabrication flows are far more driven to experiment to improve yields, lower costs
  - *Single wafer versus batch processing?*
  - *Large opportunity to improve process by reducing damage in the pre-polish step*
  - *Potentially, short CMP after epitaxial growth is an opportunity to improve device yield*

SiC Requires the Full Process Be Considered For Optimization, Not Just Individual Steps

SiC CMP Process

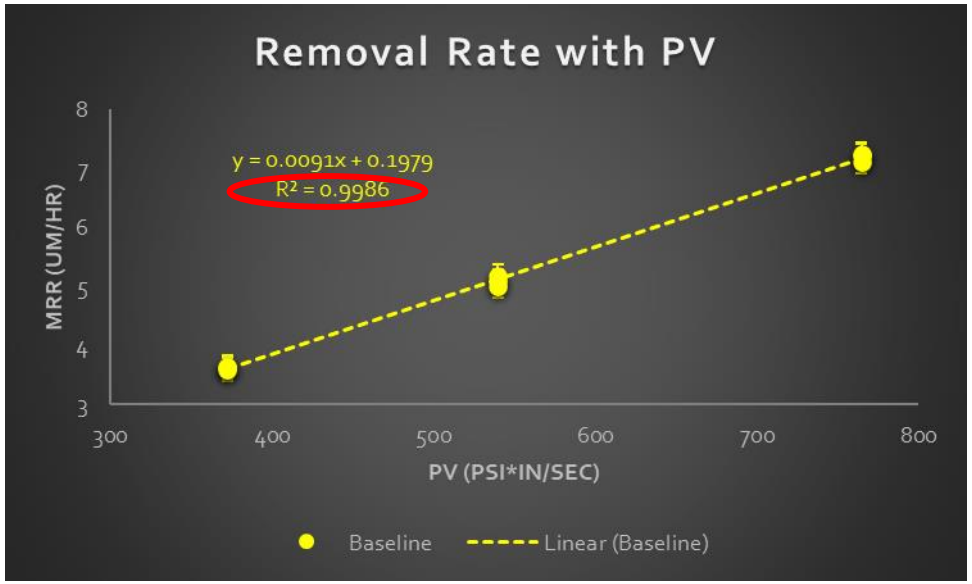
SiC Polish Rate (Historical)

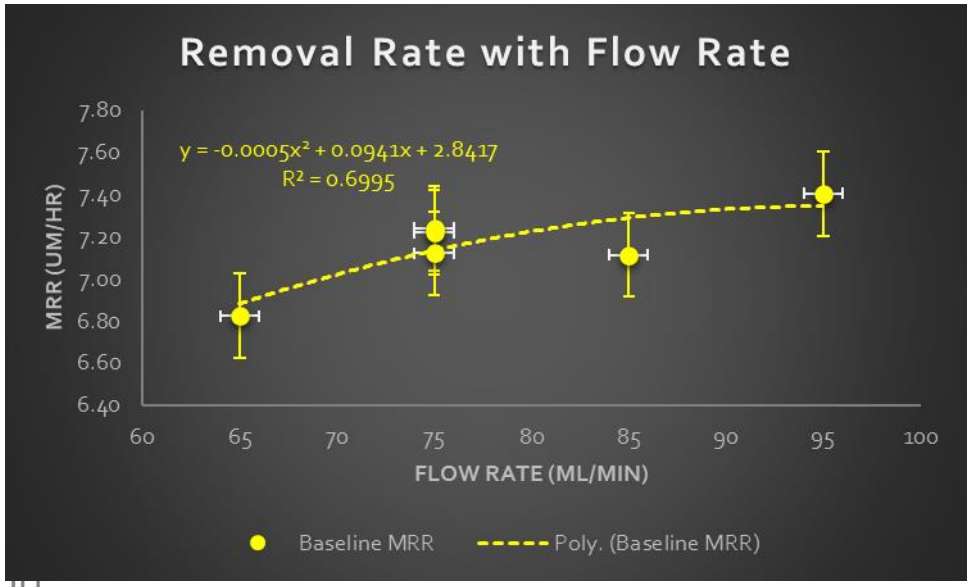
- CMP removal rates are much lower than Si or typical thin film CMP, even with dramatic improvement in recent years (see graph at right)
- Higher removal rates enable cost per wafer to be reduced, esp for single wafer polishers
- Dramatic difference in rate between Si-face and C-face of 4H SiC wafers is driven by chemical effects
  - Reduces viability of double-sided CMP
- Formulation efforts continue at all major slurry suppliers to boost removal rates and lower process cost



Source: "Evolution of SiC Substrate Processing", ICPT 2019

SiC CMP Process - General





Silicon and SiC Process Parameters Have Similar Effects

- Like silicon CMP, SiC CMP is highly Prestonian
- Significant differences for SiC compared to silicon:
  - **Far lower removal rates**
    - *Longer cycle times*
    - More temperature build up
  - **Far lower slurry flow rates**
    - Saturation reached at lower flow rates
    - *Slurry recirculation is generally not successful*
  - **End results:**
    - ***Process cost is driven by slurry usage***
    - Process improvement efforts focus on using less slurry!
      - Reduce the amount of removal required – this is pre-CMP development
      - Better consistency of single-wafer process is highly desirable
      - Increase removal rate for a given flow rate – but without significantly increasing the temperature!

SiC CMP Equipment

SiC process conditions push the limits

- For Either Batch or Single Wafer Tools, Platen Cooling is Critical
  - Temperature is limiting factor for pads and for many slurries
  - More difficult on membrane carriers – acts as an insulator, retaining ring on pad generates a lot of frictional heat
- Chemical Compatibility is Equally Important
  - Inserts, Template, Membranes, Load Cup Pads must withstand acidic conditions and powerful oxidizers – Chemically Resistant material must be specified
  - Plastics, metals inside tool must be resistant to oxidizers and corrosion (rust)
- Single-Wafer Tools Must Achieve Higher Pressures/Speeds
  - Minimum 4psi, desirable to run in the 7-9psi range
  - Typical platen speeds of 120-150 RPM
- Wafer Handling is Vitally important for the Thin Wafers
  - Modification to insert plates for loading / unloading
  - Load and Unload once per side to minimize risk
  - Ideally, can flip wafers to process both sides
- Available tools
  - Single-Wafer: AMAT Mirra/Durum, Axus Capstone
  - Batch Tools: Gigamat, Speedfam, Lapmaster-Wolters

AMAT Mirra is one of the few proven single-wafer tools

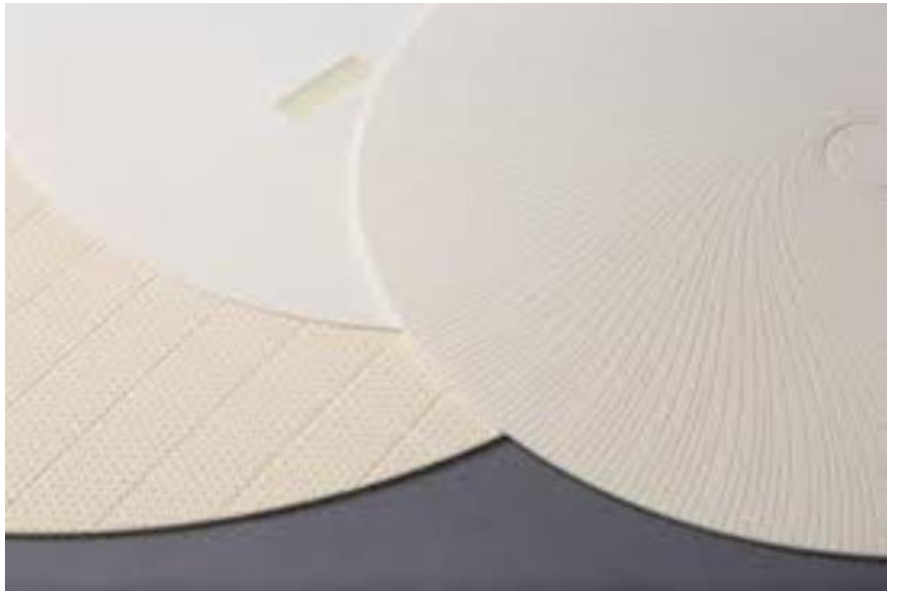
Carriers must be modified to handle thin wafers and wafers with flats

Materials selection for durability is essential

SiC CMP Process - Consumables

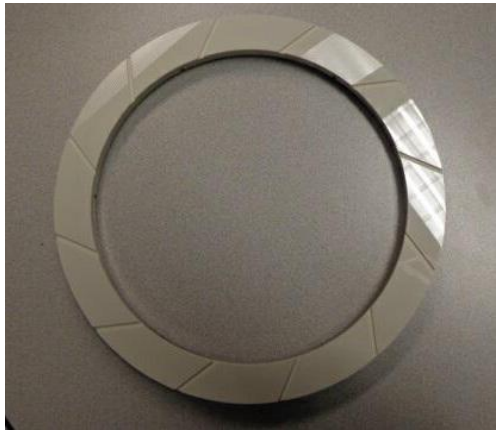
SiC Slurry Chemistry Limits Other Consumables

- Chemically dominated process
  - Potassium or Sodium Permanganate based slurry is standard
  - Extremely rough pad is generally desired
  - Ex-situ necessary, *but recent improvements allow some in-situ conditioning*
  - ***Removal rate is extremely different on the two sides of a 4H wafer***
- Compliant layers, inserts, load cup materials must be resistant material to avoid breaking down and contaminating the process
- Membranes of high durometer silicon rubber work best
- Pads must be extremely durable,
  - Hardness in the 55-65 Shore D range
  - Tightly controlled porosity
  - *No subpad – acts as insulator*
- *Conditioners cannot be electroplated or sintered*
  - CVD or brazed preferred to withstand acidic oxidizing chemistry
- *PEEK retaining rings are preferred and edge must be kept very sharp to avoid wafer slips*



Pads are Typically Porous Polyurethane

Kinik Pyradia



PEEK Ring

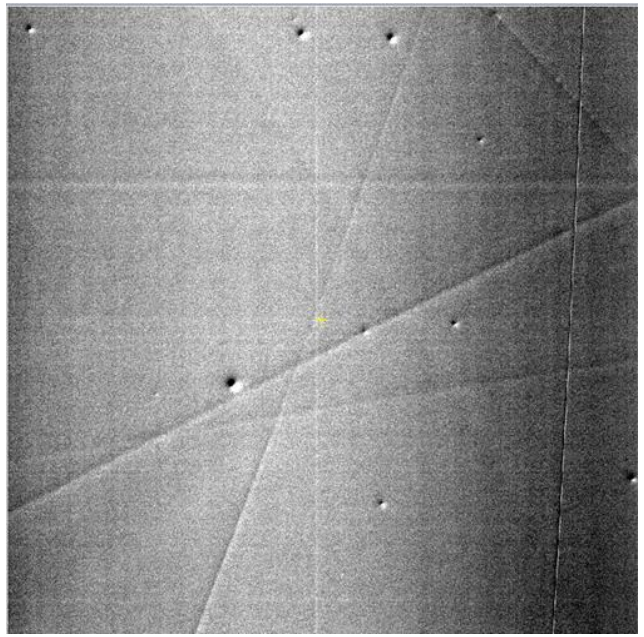
SiC CMP Process - Slurry

SiC Slurry Limits Other Consumables

- Typical Composition
  - Permanganate Oxidizer – Potassium or Sodium
  - Co-Oxidizers or Catalysts
  - Low concentration of particles (alumina / zirconia)
  - Dispersants (often static)
  - Surfactants
- Mechanism
  - Oxidize the surface of the wafers
  - Particles cut through this – expose new material
  - Particle concentration does not need to be high – a saturation point is reached
  - More oxidizer allows higher particle concentration
- Challenges
  - Older slurries are often pH adjusted – this must be very tightly controlled
  - Newer slurries do not require this, but are generally in the range of 2-4 pH
  - ***Requires constant mixing or abrasives can easily settle out***
  - Proper conditioning is essential
  - Slurry capture and recirculation is usually not viable

Purple color typical of permanganate slurry

SiC CMP Process – Common Issues, CMP Related

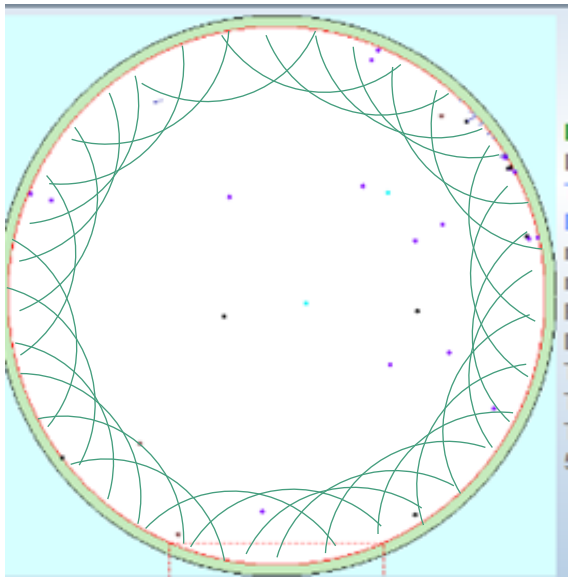


Conditioner / Diamond Particle Scratch

- Causes
  - Common with electroplated or sintered conditioners
  - Can happen with damaged CVD or brazed conditioners
- Identify
  - Loose particles roll, leaving deeper pits where the 111 plane collides
  - If particle does not embed, there is no consistent pattern
  - Earlier scratches will be washed out – conditioner particle scratches look fresh and sharp

CMP Pad Contamination

- Causes
  - Debris embeds in pad
  - May come from a chip or broken wafer, environment, conditioner, etc.
- Identify
  - Repeating pattern at a consistent radius
  - Pad can often be recovered through a long conditioning cycle
  - Can be distinguished from pre-polishing damage by the ***particular radius of curvature of the scratch***



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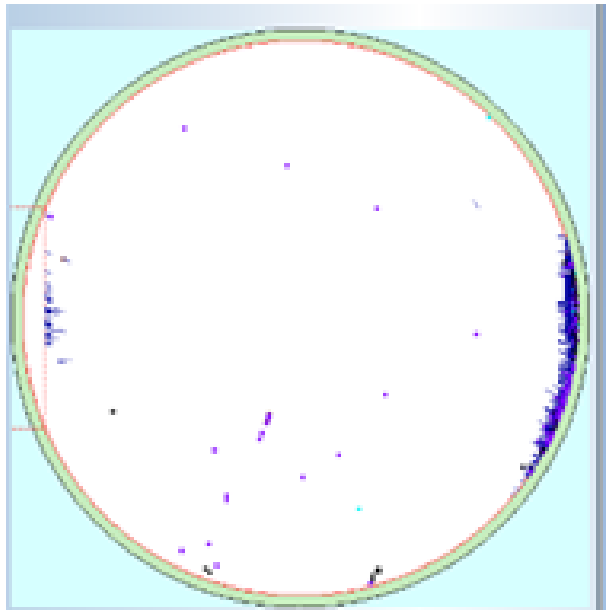
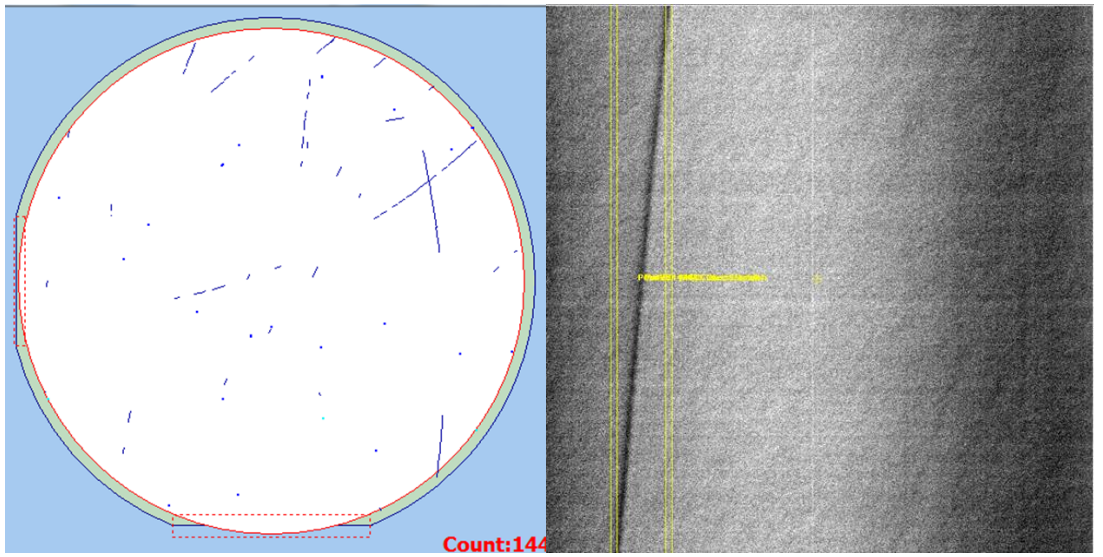


Edge Rounding / Texture

- Causes
  - Excessively soft pad or pad rebound
  - Pressures too high for pad, high temperatures softening pad
  - Particle concentration in slurry too high
  - Slow carrier speed relative to platen speed can exaggerate the issue
- Identify
  - Dense scratching or waviness confined to the edge
  - Scratching does not extend beyond the edge roll zone

Random Scratching

- Causes
  - Particle concentration too high or high count of hard agglomerates
  - Slurry failure due to temperature or chemical incompatibility
  - Pad glazing
- Identify
  - Scratches are polished with rounded edges and of consistent depth
  - No repeating pattern, but scratches typically start at edge
  - Scratches have the characteristic radius of curvature of the CMP process



SiC CMP Process – Other Common Issues

Identifying Other CMP Related Signatures

- Low Removal Rate
  - pH too Low – also results in random scratching
  - Insufficient conditioning
  - Excessive damage in incoming material
- Excessive Edge Roll
  - Pressure is too high for pad
  - Pad insufficiently stiff
  - High temperature softening pad
- Waviness / Texture / Orange Peel
  - Local temperature too high
  - Insufficient particle concentration
- Cleaning Issues
  - High temperature baked on residue
  - Cleaning chemistry incorrect for particles used

Identifying Other NON-CMP Related Signatures

- Deep Damage on Incoming Wafer
  - Deep median cracks can result in low removal rate which gradually increases along with pad temperature and torque
  - This type of damage can come from an uncontrolled grind or even insufficient removal of damage from the wire saw – look for residual wire marks
- High Bow / Warp
  - Generally comes from 1) stress in the crystal or 2) slicing issues
  - Dominantly spherical bow is usually due to crystal stress
  - Dominantly C or D-shaped profile is due to slicing
- Pre-CMP Scratching
  - Often results in rounded, partially washed out scratches
  - Radius of curvature will not match the CMP process, but will match a previous process
- Handling Issues
  - Scratching which is not a smooth curve, possibly jagged
  - Look for contaminated handling tools, end effectors

SiC CMP Process
Areas for Improvement

Transition 150mm to 200mm

Batch Process Sequence (well established for SiC through 150mm wafer size)

Source: Advantages of Single Wafer Processing," Rhoades, ESCRM 2019

Factors That Favor Single-Wafer Processing for 200mm SiC Wafers

- Individual process control for each wafer → Tighter process specs
- Much easier to implement full automation
- Can push pressures/speeds higher
- Lower risk of breakage, especially for very thin wafers
- When a wafer does break, only lose 1 wafer instead of entire batch
- Eliminates pre-sorting by thickness
- Substantially reduced labor cost
- Greatly reduced rework
- Lower defectivity
- Higher yield

Sidebar Observation

A similar transition occurred for many of the process steps in silicon device fabs (PVD, CVD, wet etch, cleans, etc.) driven by similar needs to tighten control and improve yields

Equipment

SiC Tool Improvements

- Throughput improvements
  - Must be able to reach 10-12psi on 200mm SiC
  - Must be able to reach 160 RPM platen RPM

- Must be able to safely handle thin, brittle wafers
  - Ideally, can flip the wafers
  - Reliable loading without breakage – modification of the load cup and insert plate

- Improved slurry handling
  - All materials must withstand acidic environment and strong oxidizers
  - Slurry path should prevent settling – accommodate the non-colloidal slurries
    - Avoid pushing slurry upward if possible
    - Lines should be consistently flushed when idle

- Improved cooling for pad surface temperature control
  - Chilled platens
  - Secondary slurry or platen cooling systems may help beyond this

- Improved feedback for process development and control
  - New methods for wafer slip detection / wafer loss during polish are needed
  - Feedback for pad surface temperature and platen/carrier motor loads

Slurry and Other Consumables

SiC CMP Slurry Requirements

- Slurry needs to be able to reach >10um/hr on the Si-face in a production process (not just R&D)
  - Optimize particle type and size distribution
  - Optimize chemistry and oxidizer composition
  - Possibly incorporate new co-oxidizers and catalysts
- Slurry should perform at lower temperatures than current formulations
- Improve particle suspension to avoid clogs and maintenance issues, improve consistency through mix batch

Other SiC CMP Consumables Requirements

- Pads and inserts which can withstand higher temperatures for longer life
- Pad conditioners with longer usable life

Process Flow

SiC Wafer Fabrication - Process Improvements

- Reduce the Subsurface Damage
  - Use Ductile Mode Grinding For Damage Reduction – 30k+ Grit Grinds
  - Less CMP Removal for Higher Throughput, Lower Cost
  - Risk Reduction – Grind Generally Higher Yield Than CMP

- More Uniform Material
  - Doping and Resistivity Levels Vary – This Affect the Removal Rates and Yields
  - Crystal Stress is Extremely Inconsistent
    - High stress requires lower pressure, removal rates
    - Bow and Warp cause yield loses
    - High bow material is more difficult to load

- Minimize Edge Chips, Adjust to a Rounder Edge Profile to Protect Membranes

Technology Trends Impacting SiC CMP

TRANSITION TO 200mm AND RAMP AS FAST AS POSSIBLE

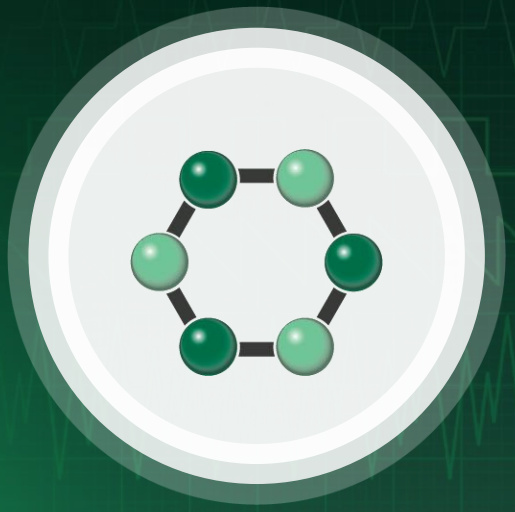
- Numerous business drivers are pushing for 200mm wafers
- Boule growth, breakage risk, and wafering yields are technical barriers
- Likely transition from batch to single-wafer processing

DRIVE TO IMPROVE CRYSTAL GROWTH AND YIELDS

- Sources of defects in PVT growth (seeds, thermal gradients, purity)
- Orientation constraints: N-type epi dep is most efficient at 4deg off axis
  - Off-axis crystal growth is prone to even more defects
  - On-axis growth leads to geometrical loss at slicing step
- Minimize stress variation within the boule (drives bow/warp, LTV, etc.)

MAXIMIZE WAFERS PER BOULE

- Hyperfocus on cost per wafer means slice as thin as possible
- Original target was 500µm → Now industry is pushing for 350µm
  - For reference, standard thickness for a 200mm silicon wafer is 725µm



THANK YOU

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