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Electronics Materials Information

Advanced Semiconductor Technology Roadmaps and Implications to CMP Materials

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Outline

- Drivers of Technology & Implications
- Logic Roadmaps & CMP
- 3D NAND Roadmaps & CMP
- DRAM Roadmaps & CMP
- CMP Market Forecast

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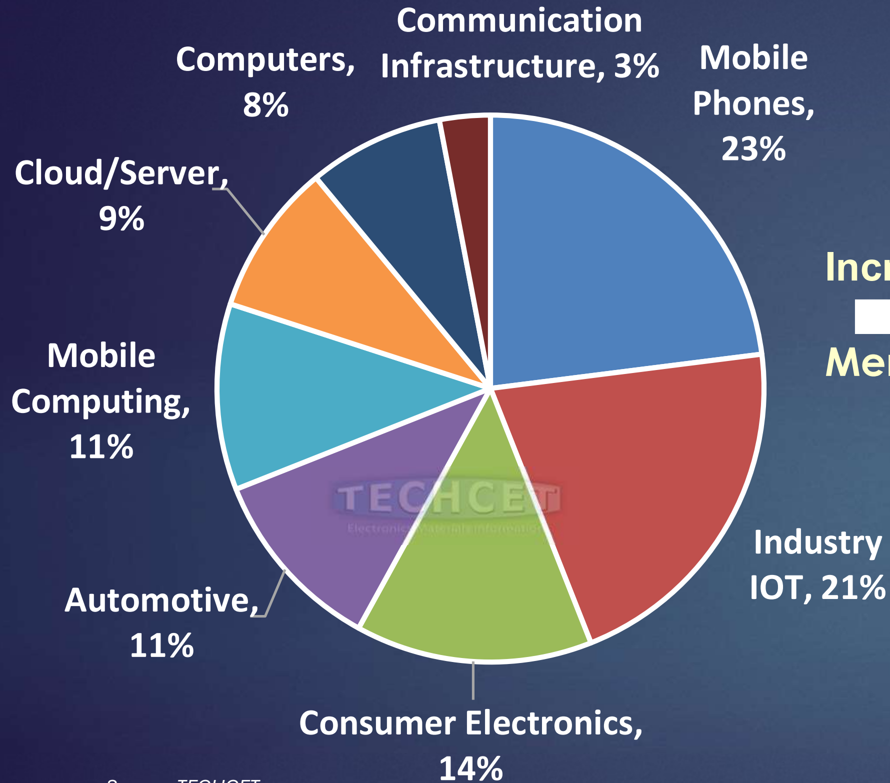
Application Driven Technologies



2023 TOTAL REVENUE $572 B

AI!

Increasing Demand

Memory & Logic

Growing Materials Demands

- ALD (esp Plasma)
- CVD
- Litho (esp. EUV & Hard Masks)
- Etch (Selective & High Aspect Ratios)

- **CMP – More steps, and new steps, and new materials**

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Adv. Logic Roadmaps

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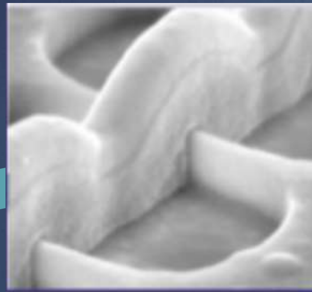
Advanced Logic Transistor Est. Roadmap

2000

Planar High-k Metal Gate

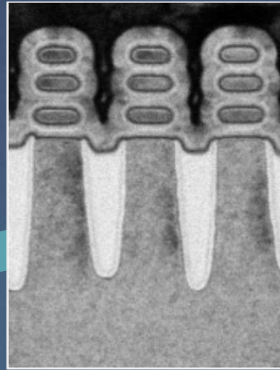
2011

Si FinFET High-k Metal Gate



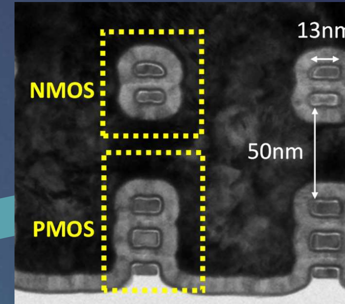
2023

Gate-all-Around Horizontal Si Nanosheets



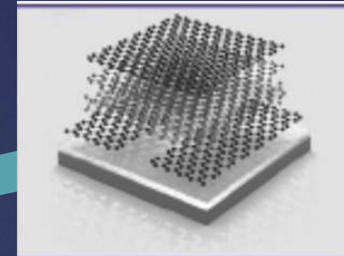
>2030

CFET Stacked GAA Nanosheets



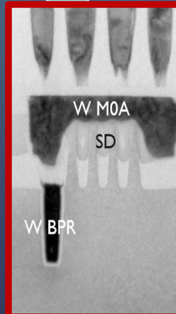
CFET

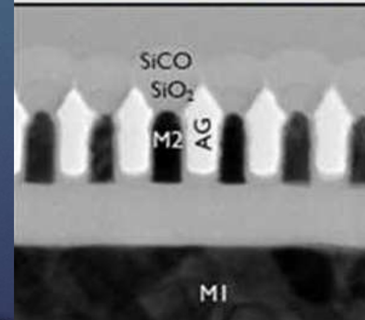
2D Semiconductor Transistors



MoS_2, WS_2, or ??

GAA Gen 2 Buried Power Rail





imec

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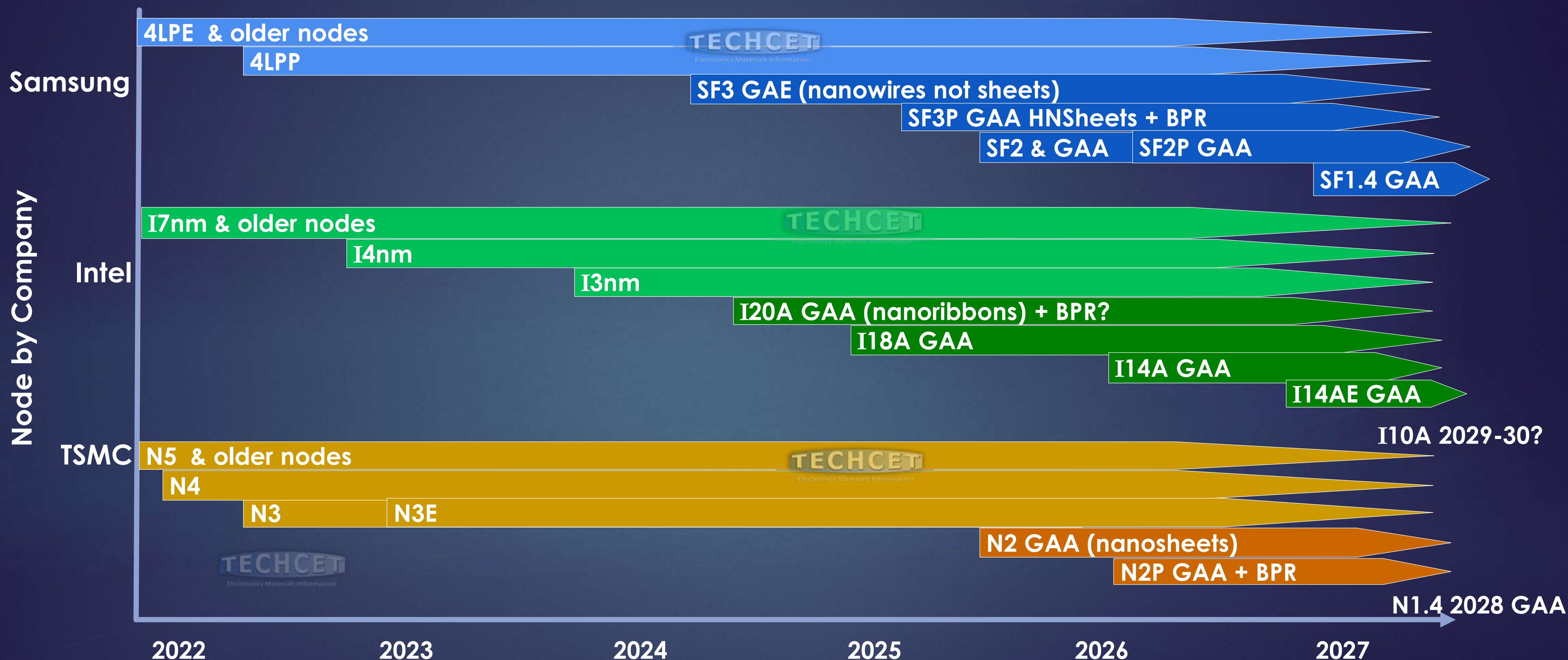
Advanced Logic (Foundry) Node HVM Estimate



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Logic Future Technology Challenges

- Transistor Structures: Planar → FinFET → Horizontal NanoSheets GAA → ForkFET (?) → CFET → Si Vertical Sheets → 2D: WS_2, MoS_2 ??
- Low Temp Dielectric CMP
- More Interconnects & New/More CMP
  - Replace Co & W with – Mo? Ru? Ru alloy? V? Ir? ???
  - Buried Power Rail & Backside Power – new CMP
- 2D FETs target sub-10nm gates – more density, new materials (MoS_2)

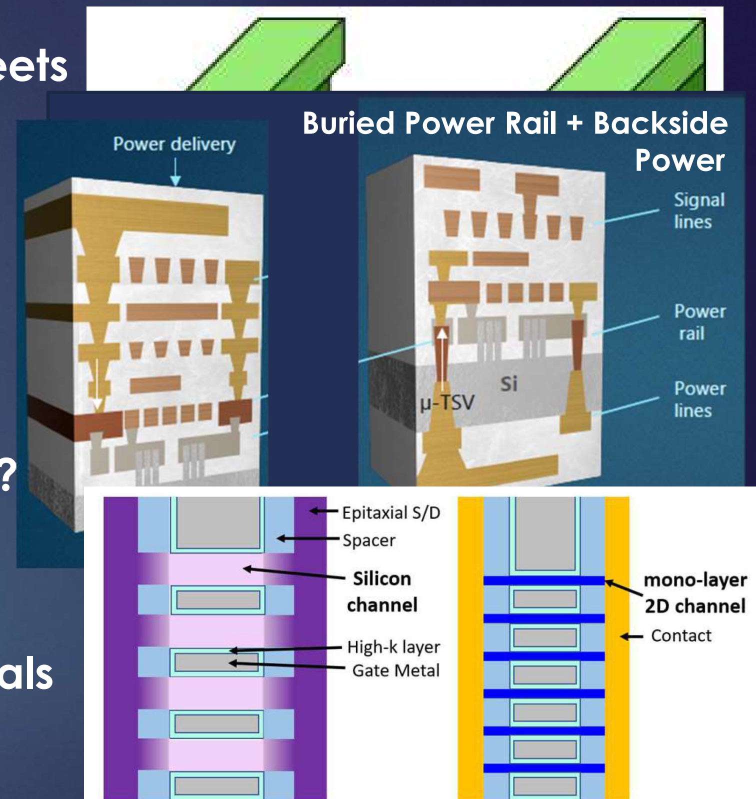

Fig. 1. 2D mono-layer nanosheet channels allow for ultra-scaled gate lengths and increased number of channels per stack height.

Mono-layer 2D FETs scaling beyond silicon
Shorter gate lengths leveraging ultra-thin 2D materials such as MoS2 (ref: Intel 2D integration IEDM 2023)

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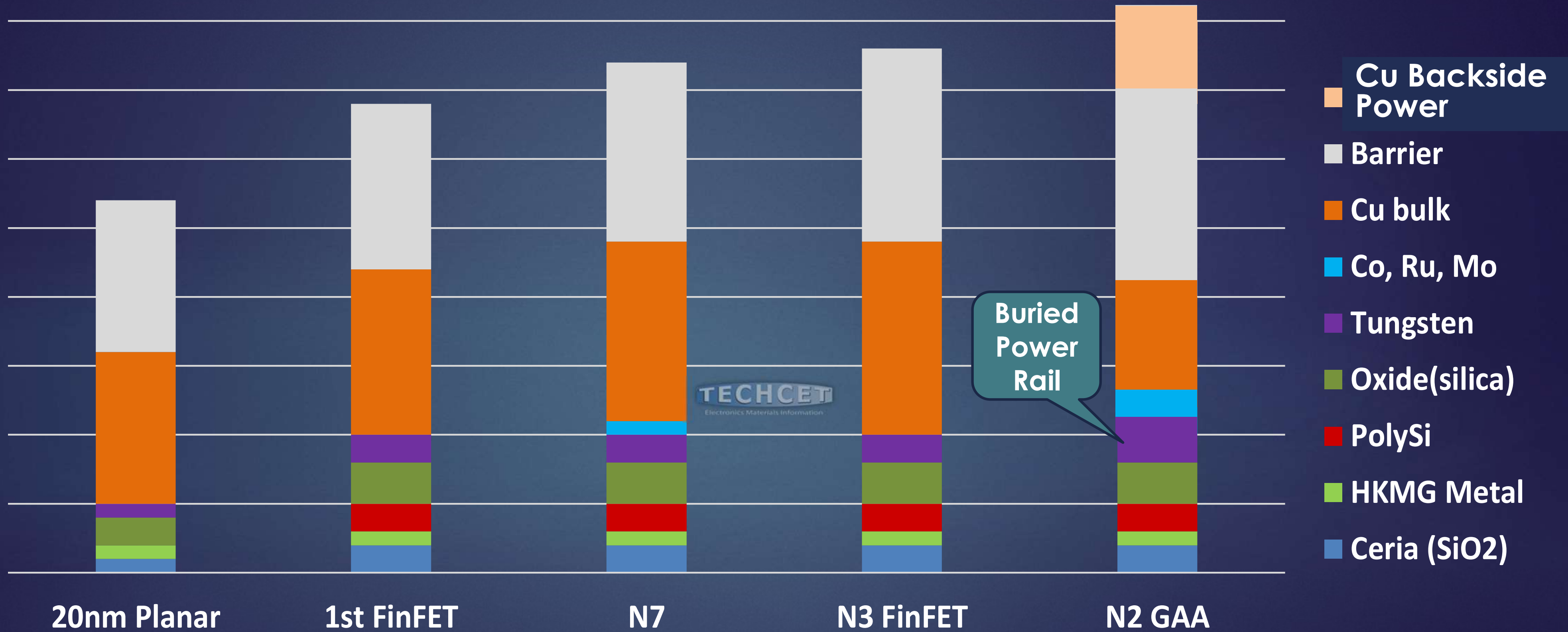
Adv. Logic CMP Process Steps Increasing



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NAND Roadmaps

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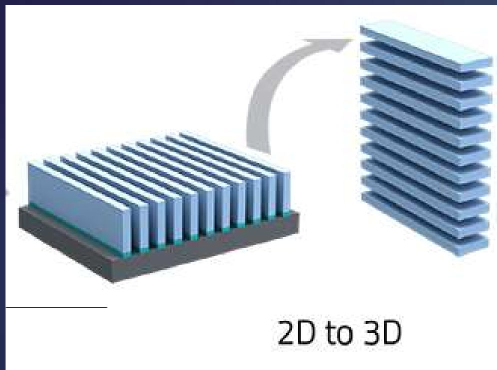
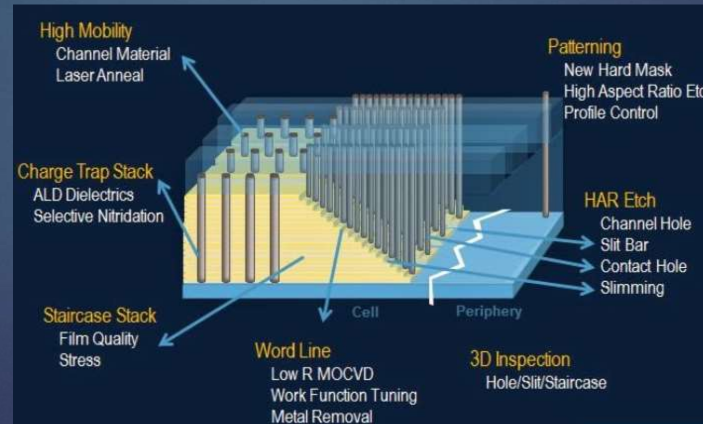
3D NAND Levels w/ Stacks/Tiers



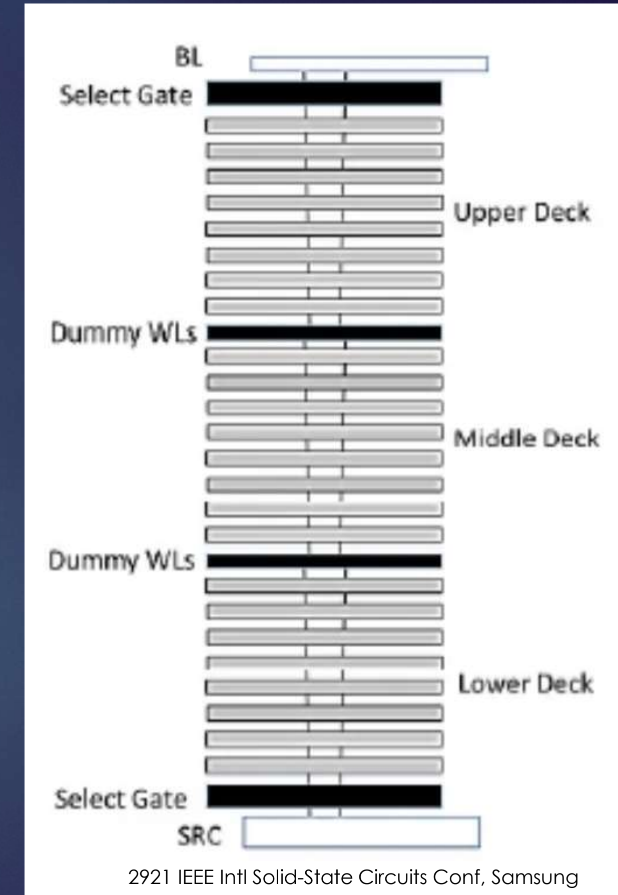
Layers

Currently 2-3 Decks/Stacks/Tiers/Strings
3 and 4 coming
Moving towards 500-1000L

Repeat Many CMP Steps with Each New Stack



http://www.maltiel.com/index.html



2921 IEEE Intl Solid-State Circuits Conf, Samsung

https://www.semianalysis.com/p/2022-nand-process-technology-comparison

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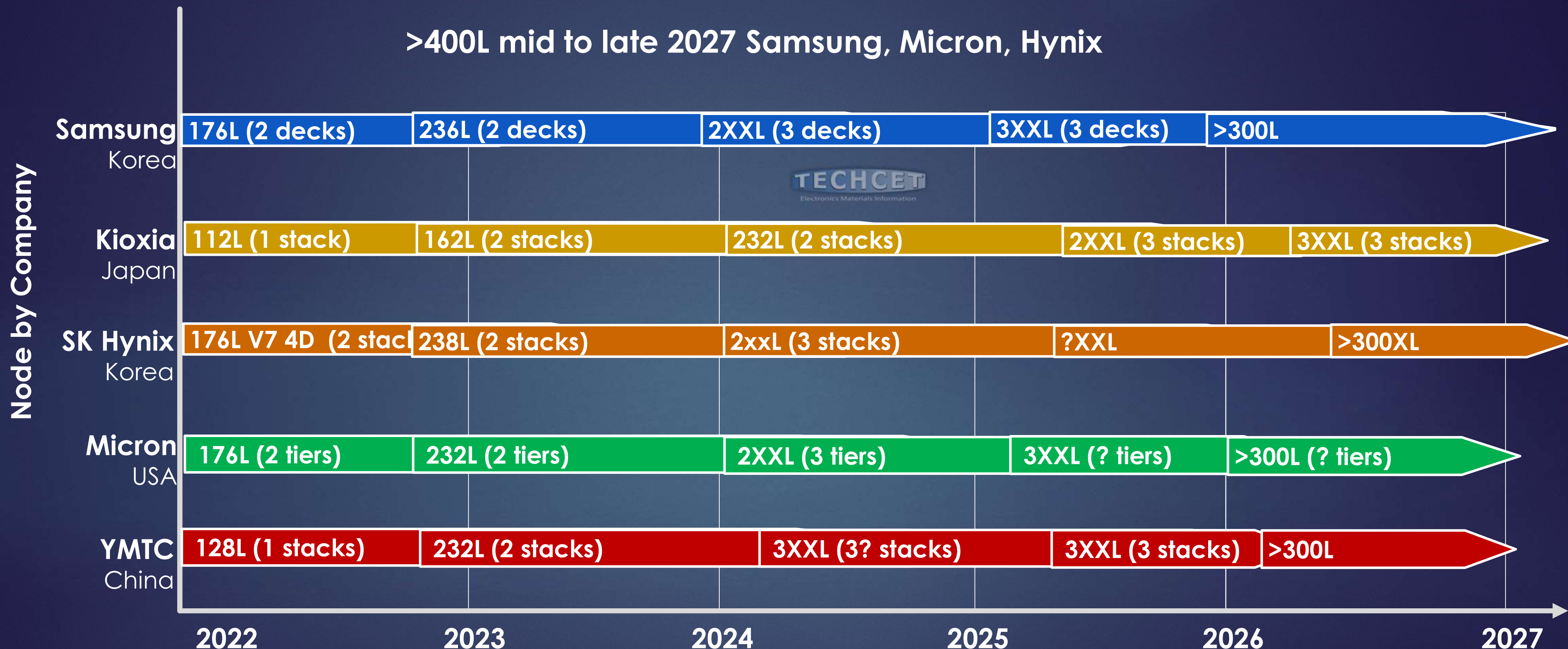
3D NAND Node HVM* Start Estimate



* Includes “Risk” Production

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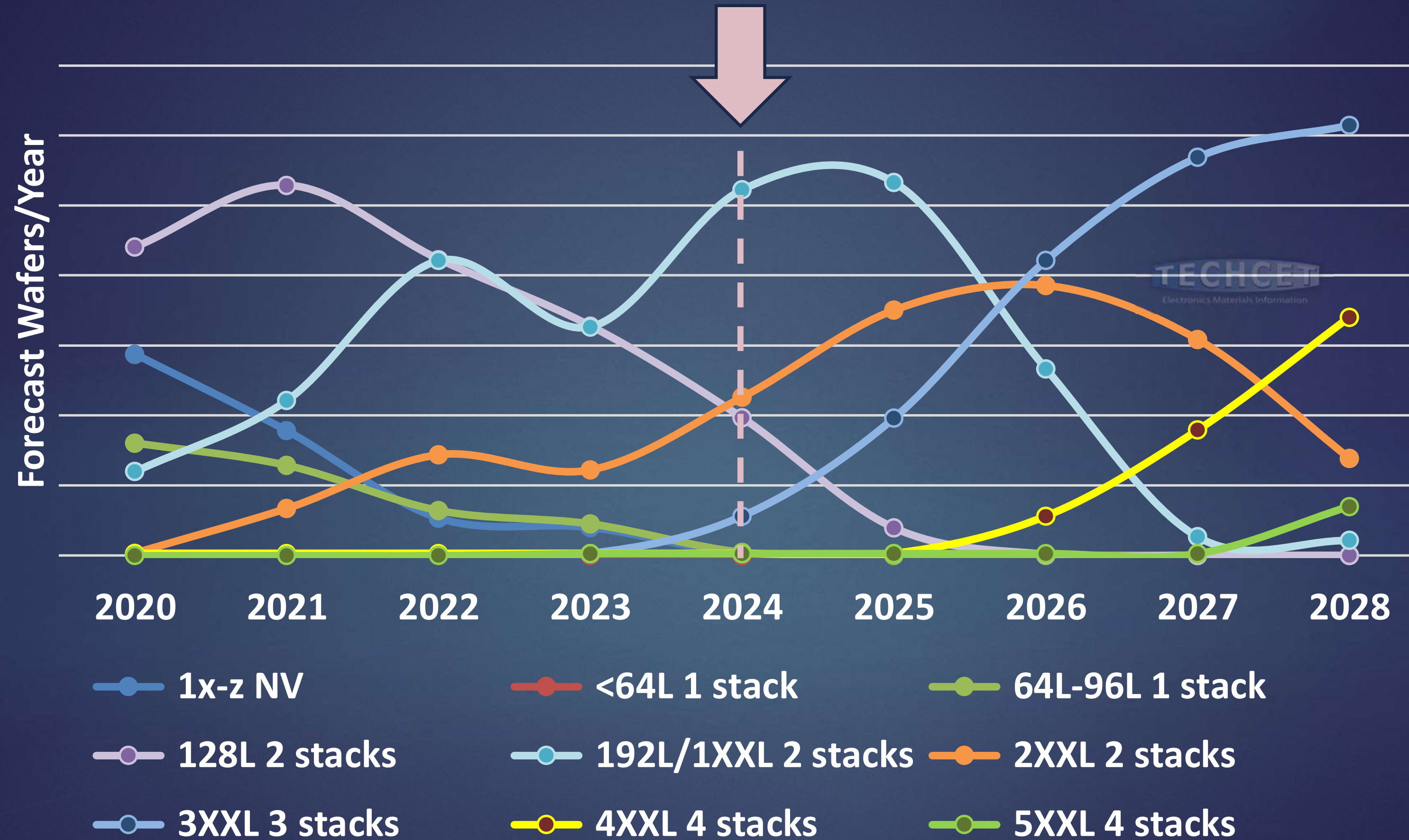
3D NAND Node Growth/Decline Examples (DRAM similar)



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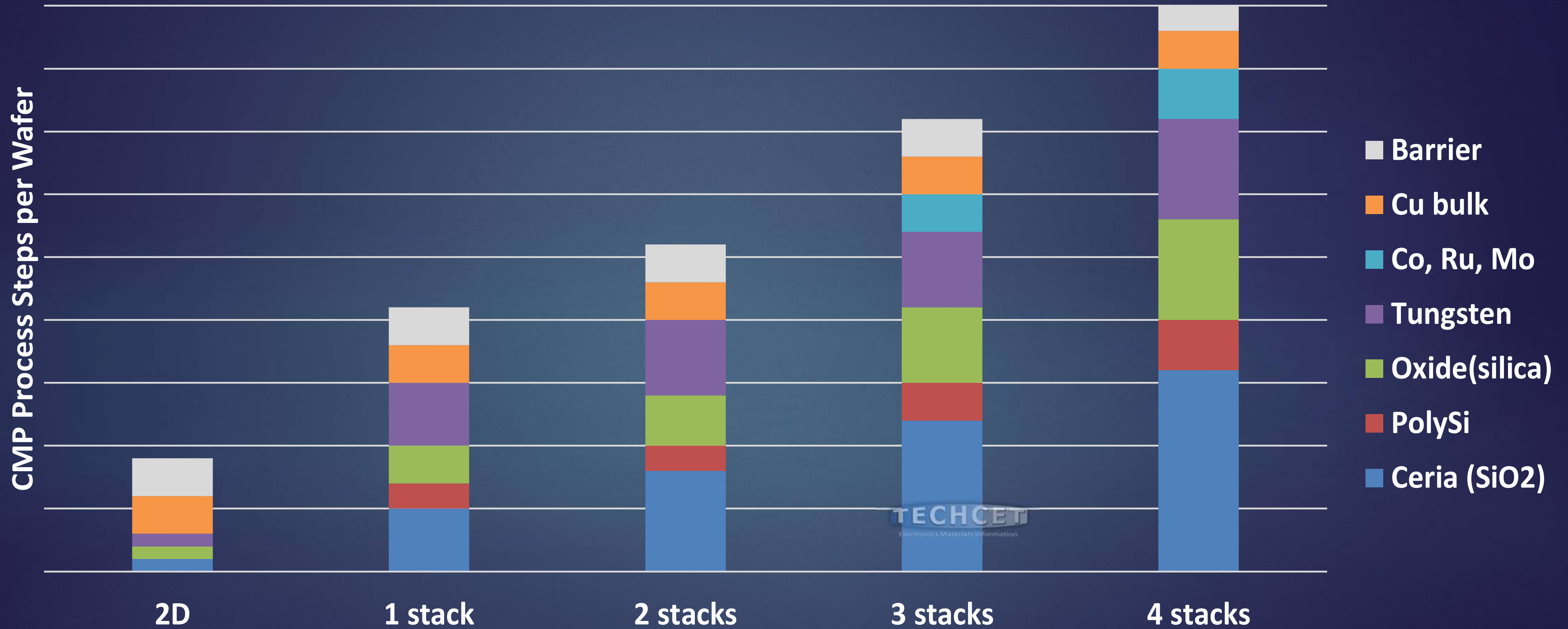
Increasing CMP Steps for 3D NAND



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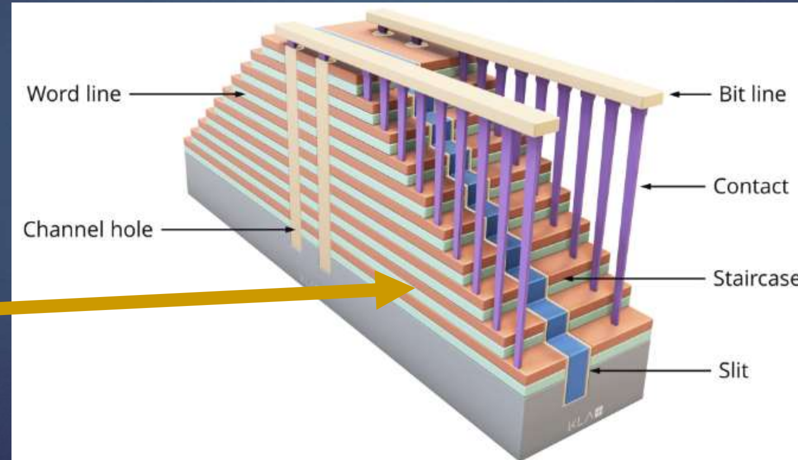
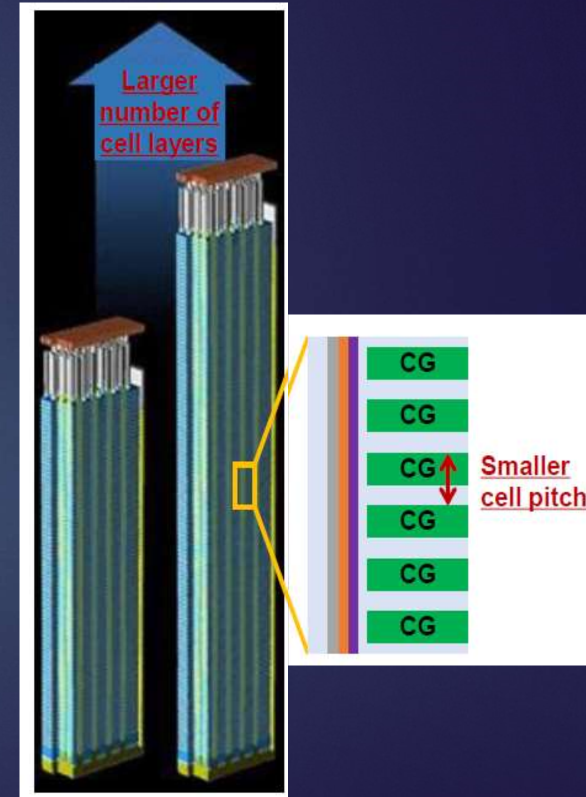
3D NAND Process Advances Required

Layers and Stacks increase – Larger Stair Case & >30% More Process Steps

- Tungsten to Moly → allows more layers per stack
- Some thick SiO2 CMP ➔ Ceria
- Staircase Adds
  Many New Steps

Staircase expands with
each added cell layer
Need tighter cells





https://www.kla.com/advance/innovation/pwg5-the-complete-wafer-geometry-system-for-ic-fabs

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DRAM Roadmaps

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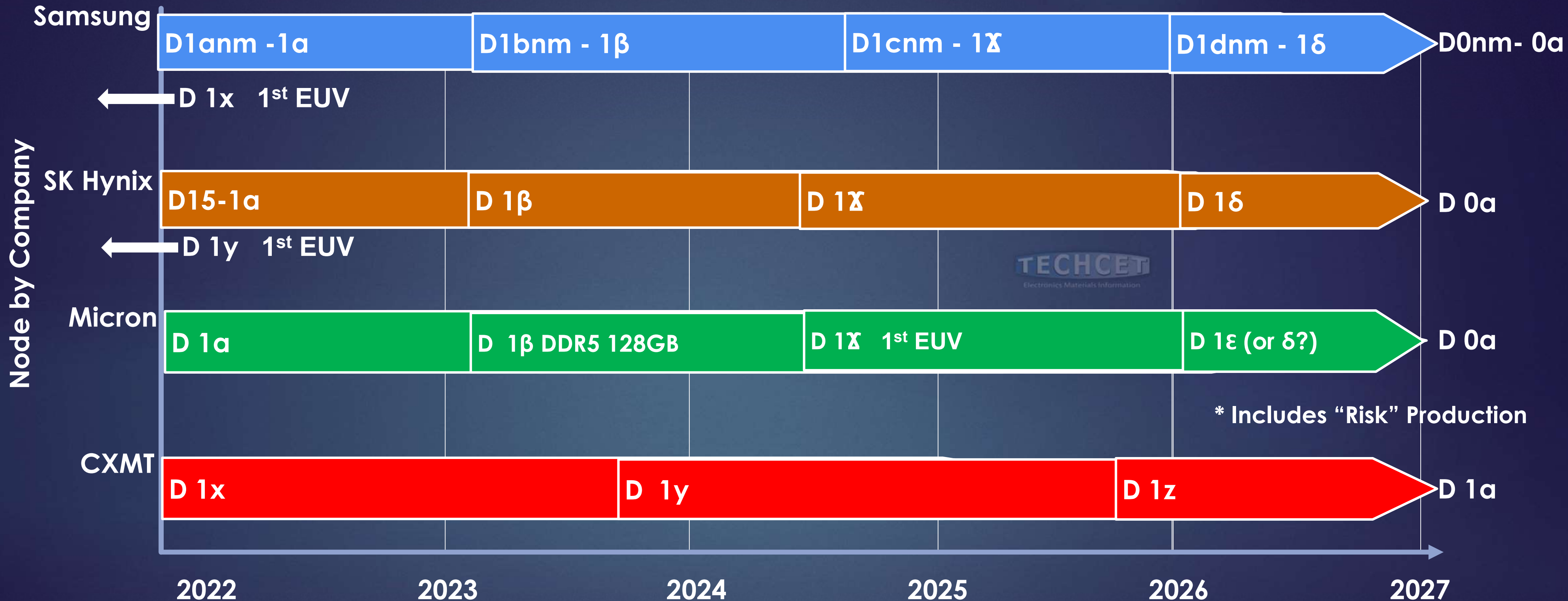
DRAM Node HVM* Estimate



Note: DRAM nodes no longer are shown as half-pitches, e.g., 1α is the fourth generation of the 10nm class where pitch ranges from 10 to 19nm. The nodes "continue to shrink", but the DRAM producers moved to node names: 1x, 1y, 1z to 1α, 1β, 1ɣ, then 0α, 0β, 0ɣ.

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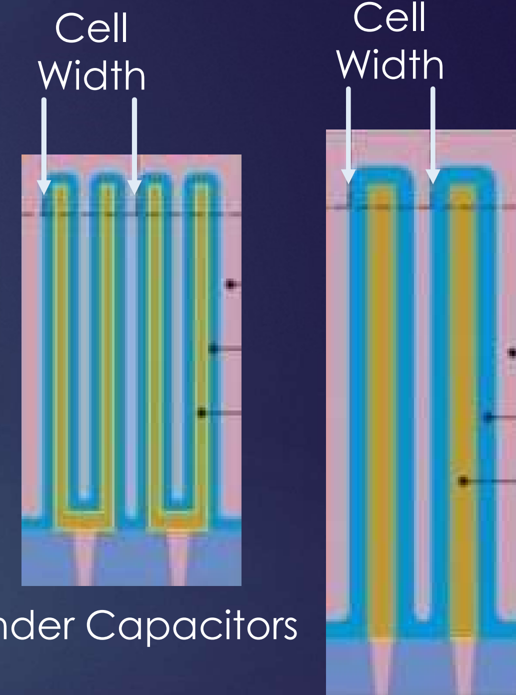
DRAM Capacitor Advances Required

Capacitors Significantly Control the Bits per Device

- New Capacitor Materials & Structures – Cylinders to Pillars
  - Pillars with triple MESH with TiON/ZAO/TiN
  - Ru/SrTiO3/Ru for capacitor or $BaSrTiO_3$, La_2O_3, Nb_2O_5, $Al2O_3$, AlN
  - More and New CMP processes

- Capacitorless/Horizontal Capacitors for 3D DRAMs (after 0x)
  - IGZO (InGaZnO) or
  - Ferroelectric HfO_2



Cylinder Capacitors

Pillar Capacitors

https://semiwiki.com/semiconductor-services/ic-knowledge/8022-lithovision-2019-semiconductor-technology-trends-and-their-impact-on-lithography/

https://www.electronicsweekly.com/uncategorised/capacitorless-3d-dram-2021-12/

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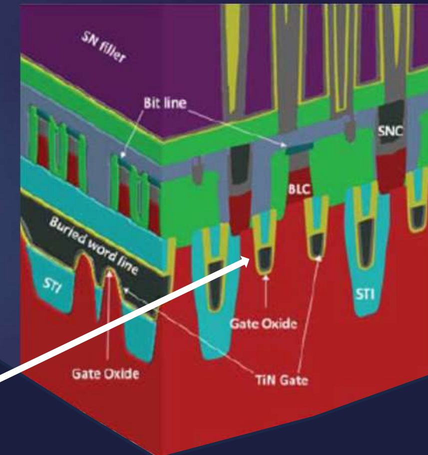
DRAM Process Advances Required, Con't

- **Transistors for Control**
  - Planar with HkMG to FinFET (Samsung) – GAA?

- **Buried Word Lines – New Materials Improve Scaling Performance**
  - Mo/WCN?Hf/SiON or WN/CoSi/Poly-Si/HfSiON
  - Potential Alternatives after Mo?
  - New CMP Processes



Buried Word Line

Source: Hong Xiao, "3D IC devices, technologies, and manufacturing", SPIE Press

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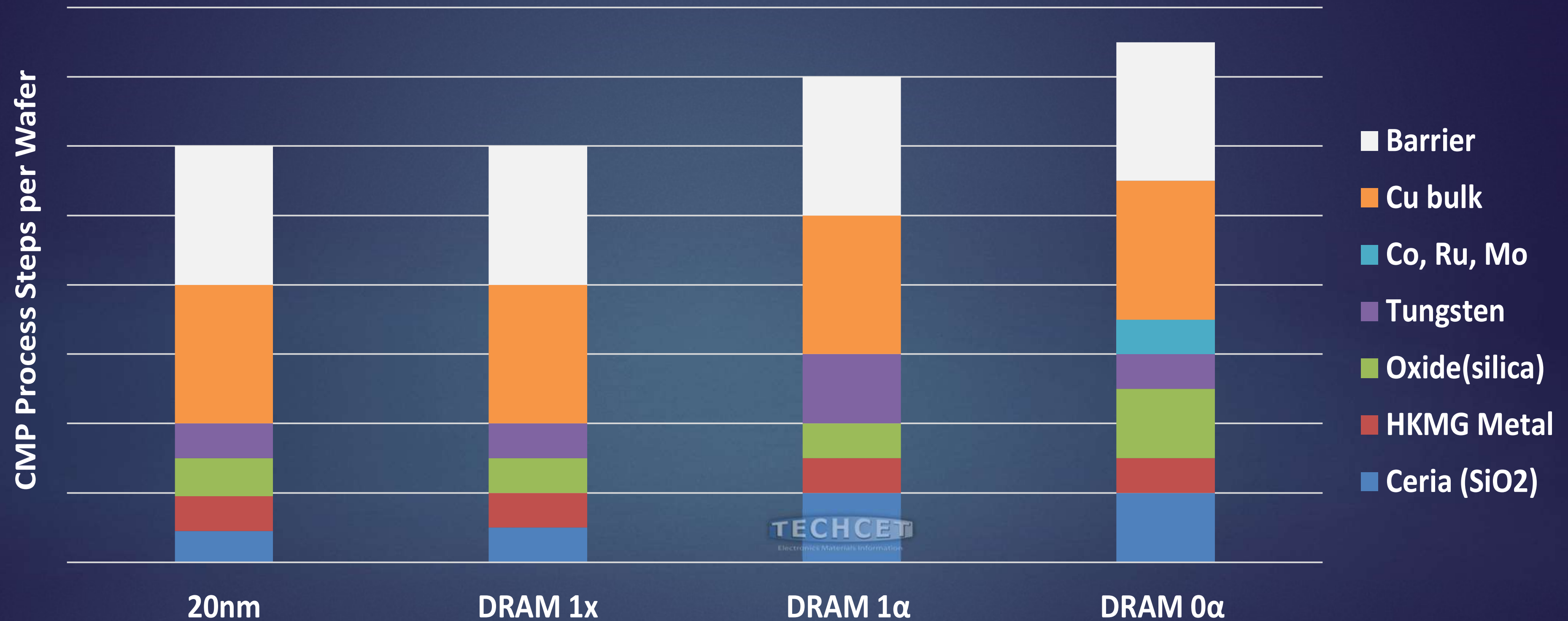
Increasing CMP Steps for DRAM



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CMP Market Forecast

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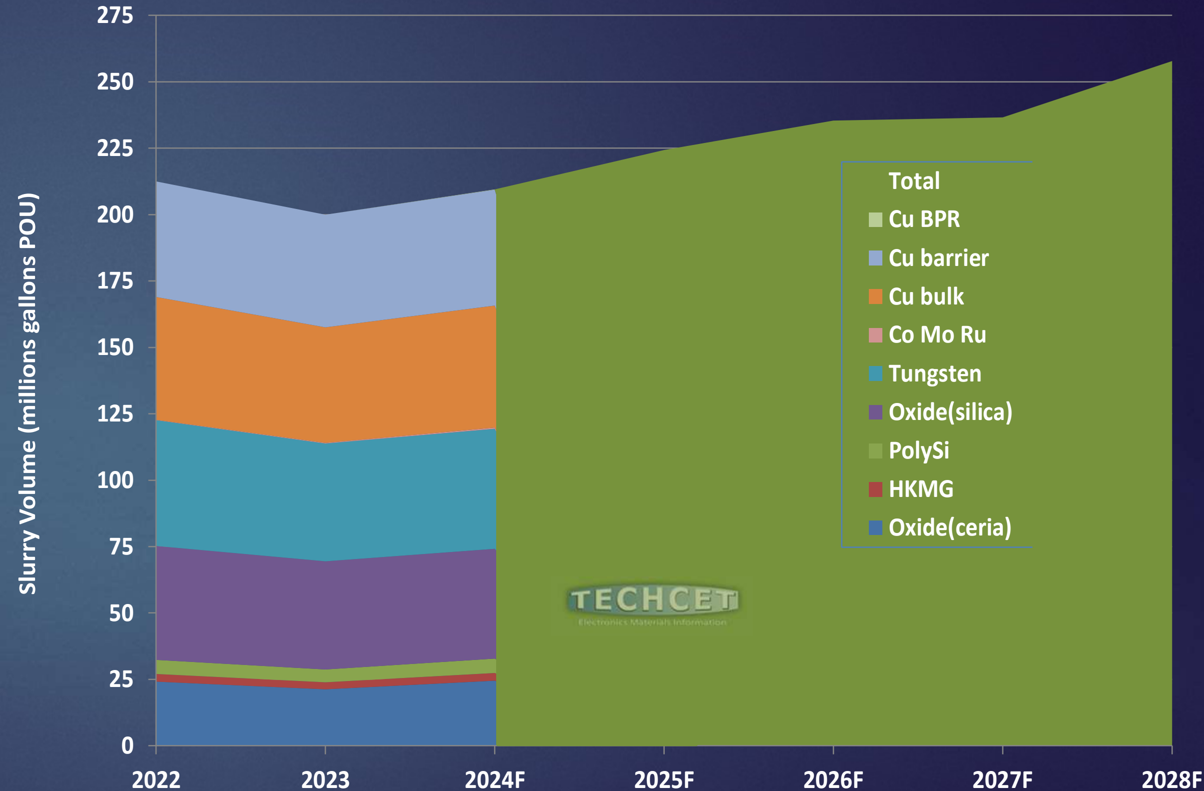
CMP Slurries 5-Year Forecast by Process Type

- 2023 CMP slurry revenue was -6.5% decline from 2022
- 2024 TAM forecasted to grow by 5.1%
- 5-yr CAGR 5.9% for 2023-2028
- Strongest growth = new processes
  - Mo, Ru or ??
  - Cu Backside Power



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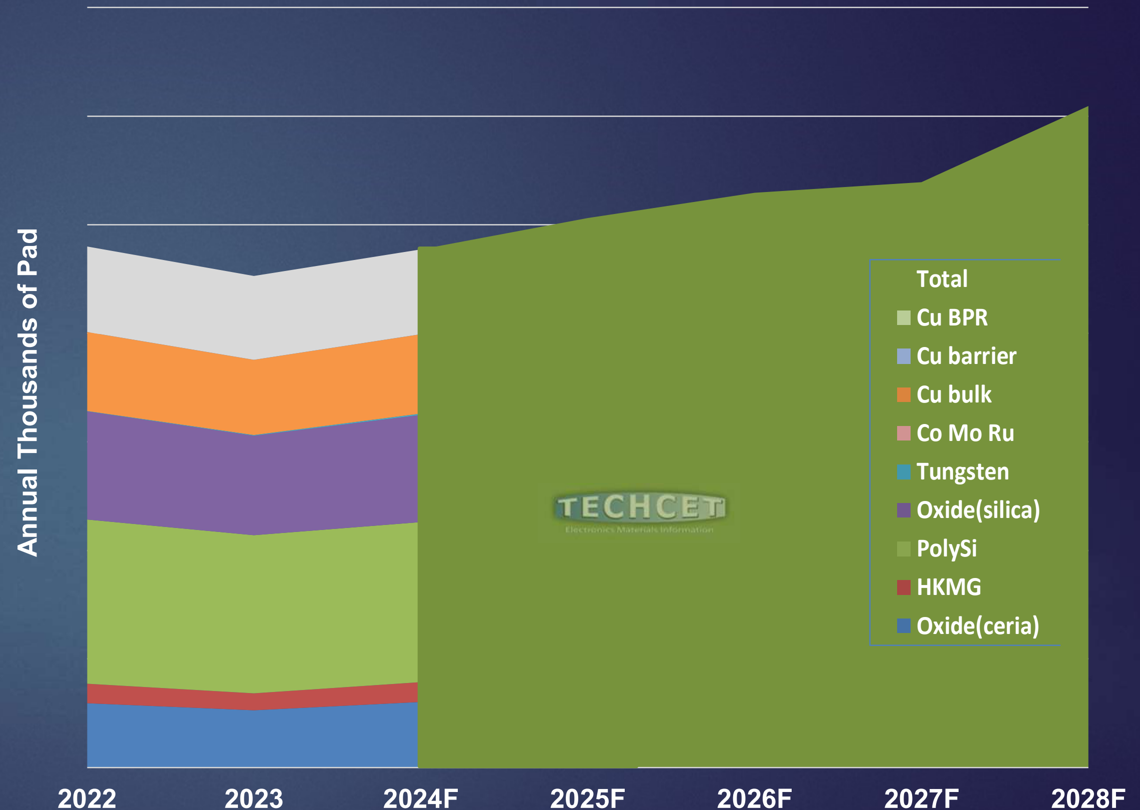
CMP Pads Forecast by Application

- Pad market contracted -6.6% in 2023 to US$1.36 B
- 2024 TAM of US$1.46 B, up 8 %
- 5-yr CAGR 6.3% for 2023 to 2028
- Oxide Ceria, PolySi and HKMG Oxide pad revenues are expected to grow by 10 to 14% each



Summary of Advancing Technologies Implication to CMP

- Logic adds more process steps
  - New Materials to Planarize
  - New Transistor Designs Coming! CFET >2030
- 3D NAND adds more layers and Decks/Stacks/Tiers/Strings
  - 30% Increase in number of CMP process steps
  - 4 Stacks is coming! >2027
- DRAM New Capacitors and Transistor Structures
  - Increased CMP process steps
  - New Materials or Process Steps to Planarize
  - 3D DRAM with "Capacitorless" Technology is coming! >2030

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TECHCET's Critical Materials Expert Data & Consulting

★ 1	CMP Consumables (Pads & Slurry)
★ 2	CMP Equipment Ancillaries (Conditioners, Filters, etc.)
3	CVD /ALD Hi K Precursors
4	CVD DIELECTRIC Precursors
5	Equipment Components – Quartz
6	Equipment Components – Silicon
7	Equipment Components – SiC/Ceramics
8	Gases - Electronic Specialty, Bulk & Rare Gases
9	Metal Plating Chemicals
10	Photoresists, Ancillaries & Extension Materials
11	Sputtering Targets
12	Wafers: Silicon, SOI
13	SiC Wafers & Manufacturing
13	Wet Chemicals / Specialty Cleans
15	Packaging Materials (die attach, underfill, lead frames, wire, etc.)
16	Impact of Chip Expansions on Material Supply-Chains

THANK YOU!

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