Advanced Semiconductor Technology Roadmaps and Implications to CMP Materials

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Outline

- Drivers of Technology & Implications
- Logic Roadmaps & CMP
- 3D NAND Roadmaps & CMP
- DRAM Roadmaps & CMP
- CMP Market Forecast
Application Driven Technologies

- Mobile Phones, 23%
- Industry IOT, 21%
- Consumer Electronics, 14%
- Automotive, 11%
- Mobile Computing, 11%
- Computers, 8%
- Cloud/Server, 9%

Growing Materials Demands
- ALD (esp Plasma)
- CVD
- Litho (esp. EUV & Hard Masks)
- Etch (Selective & High Aspect Ratios)

- CMP – More steps, and new steps, and new materials

2023 TOTAL REVENUE $572 B

Source: TECHCET

AI!
Increasing Demand
Memory & Logic

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Adv. Logic Roadmaps
Advanced Logic Transistor Est. Roadmap

2000
Planar
High-k Metal Gate

2011
Si FinFET
High-k Metal Gate

2023
Gate-all-Around Horizontal Si Nanosheets

>2030
CFET Stacked GAA Nanosheets

2D Semiconductor Transistors
MoS$_2$, WS$_2$, or ??

GAA Gen 2
Buried Power Rail

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Logic Future Technology Challenges

- **Transistor Structures:** Planar → FinFET → Horizontal NanoSheets → GAA → ForkFET (?) → CFET → Si Vertical Sheets → 2D: WS$_2$, MoS$_2$ ??
  - 2D FETs target sub-10nm gates – more density, new materials (MoS$_2$)

- **Low Temp Dielectric CMP**

- **More Interconnects & New/More CMP**

- **Buried Power Rail & Backside Power** – new CMP

- 2D FETs target sub-10nm gates – more density, new materials (MoS$_2$)

Fig. 1. 2D mono-layer nanosheet channels allow for ultra-scaled gate lengths and increased number of channels per stack height. Mono-layer 2D FETs scaling beyond silicon. Shorter gate lengths leveraging ultra-thin 2D materials such as MoS$_2$ (ref: Intel 2D integration IEDM 2023)
Adv. Logic CMP Process Steps Increasing

CMP Process Steps per Wafer

- 20nm Planar
- 1st FinFET
- N7
- N3 FinFET
- N2 GAA

Materials:
- Cu Backside Power
- Barrier
- Cu bulk
- Co, Ru, Mo
- Tungsten
- Oxide(silica)
- HKMG Metal
- Ceria (SiO2)
- PolySi
- Buried Power Rail
NAND Roadmaps
3D NAND Levels w/ Stacks/Tiers

Currently 2-3 Decks/Stacks/Tiers/Strings
3 and 4 coming
Moving towards 500-1000L

Repeat Many CMP Steps with Each New Stack

Layers

2D to 3D
3D NAND Node HVM* Start Estimate

>400L mid to late 2027 Samsung, Micron, Hynix

<table>
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<tr>
<th>Node by Company</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
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<td>Samsung</td>
<td>176L (2 decks)</td>
<td>236L (2 decks)</td>
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<td>3XXL (3 decks)</td>
<td>&gt;300L</td>
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<td>YMTC</td>
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* Includes “Risk” Production
Increasing CMP Steps for 3D NAND

- 2D
- 1 stack
- 2 stacks
- 3 stacks
- 4 stacks

- Barrier
- Cu bulk
- Co, Ru, Mo
- Tungsten
- Oxide(silica)
- PolySi
- Ceria (SiO2)
3D NAND Process Advances Required

Layers and Stacks increase – Larger Stair Case & >30% More Process Steps

- Tungsten to Moly → allows more layers per stack
- Some thick SiO2 CMP ➔ Ceria
- Staircase Adds Many New Steps

Staircase expands with each added cell layer
Need tighter cells

https://www.kla.com/advance/innovation/pwg5-the-complete-wafer-geometry-system-for-ic-fabs

2024 CMPUG Mtg – Karey Holland, PhD
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DRAM Roadmaps
Note: DRAM nodes no longer are shown as half-pitches, e.g., 1α is the fourth generation of the 10nm class where pitch ranges from 10 to 19nm. The nodes “continue to shrink”, but the DRAM producers moved to node names: 1x, 1y, 1z to 1α, 1β, 1χ, then 0α, 0β, 0χ.
Capacitors Significantly Control the Bits per Device

- **New Capacitor Materials & Structures – Cylinders to Pillars**
  - Pillars with triple MESH with TiON/ZAO/TiN
  - Ru/SrTiO3/Ru for capacitor or BaSrTiO$_3$, La$_2$O$_3$, Nb$_2$O$_5$, Al2O$_3$, AlN
  - More and New CMP processes

- **Capacitorless/Horizontal Capacitors for 3D DRAMs (after 0X)**
  - IGZO (InGaZnO) or
  - Ferroelectric HfO$_2$

https://www.electronicsweekly.com/unategorised/capacitorless-3d-dram-2021-12/
DRAM Process Advances Required, Con’t

- Transistors for Control
  - Planar with HkMG to FinFET (Samsung) – GAA?

- Buried Word Lines – New Materials Improve Scaling Performance
  - Mo/WCN?Hf/SiON or WN/CoSi/Poly-Si/HfSiON
  - Potential Alternatives after Mo?
  - New CMP Processes

Source: Hong Xiao, “3D IC devices, technologies, and manufacturing”, SPIE Press
Increasing CMP Steps for DRAM
CMP Market Forecast
2023 CMP slurry revenue was -6.5% decline from 2022
2024 TAM forecasted to grow by 5.1%
5-yr CAGR 5.9% for 2023-2028
Strongest growth = new processes
- Mo, Ru or ??
- Cu Backside Power
Pad market contracted -6.6% in 2023 to US$1.36 B

- 2024 TAM of US$1.46 B, up 8%
- 5-yr CAGR 6.3% for 2023 to 2028
- Oxide Ceria, PolySi and HKMG Oxide pad revenues are expected to grow by 10 to 14% each
Summary of Advancing Technologies Implication to CMP

- Logic adds more process steps
  - New Materials to Planarize
  - New Transistor Designs Coming! CFET >2030

- 3D NAND adds more layers and Decks/Stacks/Tiers/Strings
  - 30% Increase in number of CMP process steps
  - 4 Stacks is coming! >2027

- DRAM New Capacitors and Transistor Structures
  - Increased CMP process steps
  - New Materials or Process Steps to Planarize
  - 3D DRAM with “Capacitorless” Technology is coming! >2030
TECHCET’s Critical Materials Expert Data & Consulting

1. CMP Consumables (Pads & Slurry)
2. CMP Equipment Ancillaries (Conditioners, Filters, etc.)
3. CVD /ALD Hi K Precursors
4. CVD DIELECTRIC Precursors
5. Equipment Components – Quartz
6. Equipment Components – Silicon
7. Equipment Components – SiC/Ceramics
8. Gases - Electronic Specialty, Bulk & Rare Gases
9. Metal Plating Chemicals
10. Photoresists, Ancillaries & Extension Materials
11. Sputtering Targets
12. Wafers: Silicon, SOI
13. SiC Wafers & Manufacturing
14. Wet Chemicals / Specialty Cleans
15. Packaging Materials (die attach, underfill, lead frames, wire, etc.)

THANK YOU!

For more Info check out
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Https://cmcfabs.org

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