**NCCAVS Joint User Group Meeting Agenda (CMPUG, PAG, & TFUG)**

## Topic: Packaging Beyond the Mainstream

**Meeting Date:** Wednesday, September 13, 2023
**Time:** 12:30 – 3:20pm PT (**TIMEZONE CONVERTER**)

**FREE TO ATTEND!** ***ADVANCE REGISTRATION REQUIRED – Zoom login details provided upon registration!***

## REGISTER FREE

**Co-Chairs:**
**Rob Rhoades**, X-trinsic, **zestrion@gmail.com**
**Jeff Shields**, GlobalFoundries, **jeffrey.shields@att.net**
**Paul Werbaneth**, Independent Consultant, **pfwerbaneth@gmail.com**

The Northern California Chapter of the American Vacuum Society invites you to participate in a Joint User Group Meeting on Wednesday, September 13, 2023. The meeting is being hosted by NCCAVS via the CMP Users Group, the Plasma Applications Group, and the Thin Film Users Group.

**AGENDA**

12:30 p.m. Welcome and Acknowledgement of Meeting Sponsors
Co-Chairs: Rob Rhoades, Jeff Shields, Paul Werbaneth

12:40 p.m. **Knut Gottfried**, ErzM and Fraunhofer ENAS, *"Waferbonding and CMP – A Perfect Couple"*

**Abstract:**
Waferbonding is one of the fundamental wafer level packaging technologies. Although it has been established for many years, it still has huge, unfolded potential for semiconductor and MEMS fabrication. It exists in various process variants whereby it can cover almost unlimited applications.
Joining wafers on its full surface are requires well defined surface properties, such as planarity, roughness, and topography. Especially direct and hybrid bonding technologies may come along with extreme tight requirements regarding these surface parameters. Thus, Chemical Mechanical Polishing (CMP) is an ideal partner for wafer bonding because it is the only technology that can address these surface attributes on full wafer scale and in needed quality. This talk will give a short overview regarding existing wafer bonding technologies and will discuss direct and hybrid bonding requirements more in detail. Finally, it will show how CMP can enable such processes. Besides CMP process related topics itself, special emphasis will be given on appropriate surface metrology techniques and strategies.

**Biography**
Knut received his Diploma degree in Electrical Engineering from Chemnitz University of Technology (TUC), Germany, in 1993. Following he worked as Research Engineer at the Chemnitz University's Center for Microtechnologies. He was mainly involved in research for

advanced interconnect systems. He graduated as Ph.D in 2004. His thesis was about interconnect schemes for SiC-based harsh environment sensor devices. In 2001 Knut took over general responsibility for semiconductor surface preparation technologies at Fraunhofer ENAS. Moreover, he is Deputy of the department "Nano Device Technologies". Knut is Chairman of the European CMP- and Wet-Users group and EC Chair of the "International Conference on Planarization Technology – ICPT". He is also Founder, Co-Owner, and CEO of ErzM-Technologies, a company that focusses on customer specific advanced semiconductor process and technology development.

1:10 p.m. **Liangyu Chen**, NASA, *"Pt / HTCC Alumina based Electronic Packaging System and Integration Processes for High Temperature Harsh Environment Applications"*

**Abstract:**
Electronic devices capable of operation at 500°C are required for long term Venus surface missions, as well as for *in situ* monitoring and control of next generation aeronautical engines. High temperature sensors and electronics can also find many applications in the military, and energy and automobile industries. Various silicon carbide (SiC) sensors and electronic devices have been developed for operation at 500 °C, and a compatible packaging system is needed for long term test and deployment of these high temperature devices. High temperature co-fired ceramics (HTCC) alumina with platinum (Pt) conductor was proposed for high temperature electronic packaging. A prototype Pt/HTCC alumina packaging system including chip-level package and circuit board has been reported previously for long-term electrical testing of SiC integrated circuits at 500 °C and brief testing at much higher temperatures. HTCC alumina is an excellent dielectric material with acceptable dielectric constant and low dielectric loss over wide temperature and frequency ranges. Pt is chemically noble and can be co-fired with HTCC alumina in air ambient producing a viable electronic packaging material system for high temperature applications. This talk presents a description of a packaging system including low power prototype packages and ceramic circuit boards (PCB) based on HTCC alumina and Pt metallization for 500°C harsh environment applications. The detailed designs of chip-level packages/circuit boards, fabrication of chip-level packages/circuit boards, materials and processes for 500 ˚C durable wire-bonding and SiC die-attach, and integration of a multi-chip circuit board are presented. Experimental test results of this packaging approach applied to SiC integrated circuits at 500 ˚C and related environments are discussed as well.

**Biography:**
Liangyu Chen received his B.S. degree in electronics/physics from Fudan University, P.R. China, and the M.S. and Ph.D. degrees in physics from Case Western Reserve University. Currently, he is a Senior Scientist at Ohio Aerospace Institute/NASA GRC in Cleveland, Ohio. His major research interests include materials, structures, process, and testing of packaging technologies for silicon carbide electronics and sensors for applications in high temperature harsh environment.

1:40 p.m. **Scott Sikorski**, IBM*, "The CHIPS Act-related National Advanced Packaging Manufacturing Program"*

**Biography:**
Dr. Scott Sikorski has responsibility for business development and offering management for the IBM Bromont OSAT facility as well as for driving the IBM Research Heterogeneous Integration and Chiplet ecosystem development. Previously he was responsible for developing IBM's AI hardware partner ecosystem. He rejoined IBM in 2020 after a decade in the broader industry. He is based out the T.J. Watson Research Center. Prior to his return to IBM, Dr. Sikorski was with STATS ChipPAC for 10 years. During this time he held leadership positions in product line management and business development before being promoted to head of Corporate Strategy in late 2012. In this role he assisted in the acquisition of the company by JCET Group in 2015. In JCET, he was named Vice President of Product Technology Marketing and in December 2017, Dr. Sikorski was appointed VP of Group Technology Strategy.

Dr. Sikorski served on the Boards of Directors of industry organizations iNEMI and MEPTEC for several years. The International Electronics Manufacturing Initiative (iNEMI) is a not-for-profit, R&D consortium forum focused on accelerating improvements in the electronics manufacturing industry. MEPTEC, the MicroElectronics Packaging and Test Engineering Council, is a trade association of semiconductor suppliers, manufacturers and vendors engaged in packaging, assembly and test.

Dr. Sikorski started his career in 1989 with IBM Microelectronics holding positions in R&D, manufacturing, product line management, business development and complex deal negotiation over a 20-year period. He received his Bachelor of Science degree from Columbia University's School of Engineering and Applied Sciences in Metallurgical Engineering and his Master's degree and Ph.D. from the Massachusetts Institute of Technology, both in Materials Engineering.

2:10 p.m. **P M Raj**, Florida International University, "*Hybrid Multiscale Manufacturing Technologies for Heterogeneous Package Integration"*

**Abstract:**
Heterogeneous integration with seamless and 3D connectivity between digital, RF, analog and passive components in a single package with unlimited bandwidth at lower power is the key to realize future electronic and bioelectronic systems. This talk describes the recent process integration breakthroughs that are making heterogeneous integration a reality with all the semiconductor and other system components in a single thin 3D package. A hybrid combination of semi-additive, subtractive and additive patterning techniques will be shown as the ideal approach for scalable and low-cost manufacturing. In the first part, nanostructured magnetic inductors, high surface area nanocapacitors and innovative 3D component designs will be described for integrated power modules. The second part focuses on material and component integration technologies for high-bandwidth 5G-6G communications. include high-gain antenna arrays in a package with integrated power dividers and combiners, low-loss THz interconnects with substrate-integrated low-loss waveguides, integrated electromagnetic interference isolation structures and integrated nanodielectrics for nonreciprocal and tunable components. The last part of the presentation describes nanopackaging technologies to enable bioelectronic systems with seamless integration between neural recording arrays, active devices and wireless interfaces for ultra-miniaturized wearable and implantable bioelectronic systems.

**Biography:**
Dr. P. M. Raj's expertise is in packaging of electronic and bioelectronic systems, with emphasis on nanoscale RF, power and bioelectronic components, and active and passive integration in ultrathin embedded modules. He is an Associate Professor in Biomedical Engineering and Electrical and Computer Engineering at Florida International University, and Adjunct Professor at Georgia Institute of Technology, Atlanta. His research led to 360 publications, which include 10 patents. He received more than 30 best-paper awards. He is the Chair of Nanopackaging Technical Committee, EPS Representative of IEEE Nanotechnology Council, IEEE Distinguished Lecturer in Nanotechnology for 2020, Associate Editor for IEEE Nanotechnology Magazine and Transactions of Components, Packaging and Manufacturing Technologies (CPMT). He got his Btech from IIT Kanpur (1993), ME from IISc (1995) and PhD from Rutgers University (1999).

2:40 p.m. **G. Bahar Basim**, Intel, *"A Review on CMP Challenges in HWB and Wafer Level Packaging"*

**Abstract:**
Chemical mechanical planarization/polishing process faces new challenges in multiple new dimensions as hybrid wafer bonding (HWB) and flip-chip technologies evolve to enable innovative integration forms in semiconductor applications. The advanced capabilities of (i) manufacturing the CMOS independent of the memory array through HWB and, (ii) selecting the fully functional chiplets at the die level for heterogenous components for flip-chip bonding, drive cost-effective and high-performance integration.
This paper is a review of the CMP challenges as these new technologies demand additional capabilities such as bonding surface planarization in addition to TSV exposure and polishing ability for backside metallization, edge trimming as well as backside thinning. The toolsets and current capabilities are reviewed in addition to the forthcoming trends of manufacturing ultrathin wafers.

**Biography:**
Dr. G. Bahar Basim is an expert in electronic materials and chemical mechanical planarization (CMP) process. Dr. Basim received her Ph.D. from the University of Florida Materials Science and Engineering Department in 2002. She worked for Intel Corporation in Santa Clara, CA and Texas Instruments Incorporated in Dallas TX, where she contributed to CMP process development, non-volatile memory product development, yield enhancement, and process integration CMOS, flash and ferroelectric memory device manufacturing.

Dr. Basim joined academia in 2009 as a founder faculty of a Private University in Europe and received the European Commission Marie Curie People Award for her research on nanoscale protective oxide film characterization and applications focusing on CMP fundamental beyond 10 nm. She has led two EU-Eureka projects and many industrially supported projects collaborating with Germany, Canada, Romania, Poland, Czech Republic, Korea, England, and Ireland. She has US and WPO patents and international patent applications in microelectronics, coatings, and surface science in addition to numerous publications and presentations. She is the organizing member of the Electrochemical Society CMP symposia since 2010 and a referee for many professional journals. Dr. Basim has been a faculty member at the Department of Materials Science and Engineering and the NSF-IUCRC Center for Particles and Surfactant

Systems at the University of Florida and recently joined back to Intel Corporation as a Senior Staff Process Engineer at Santa Clara, CA for 3-D NAND development.

3:10 p.m. Thank you and adjournment

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