A Review on CMP Challenges in Hybrid Wafer Bonding and Wafer Level Packaging

G. Bahar Basim, PhD

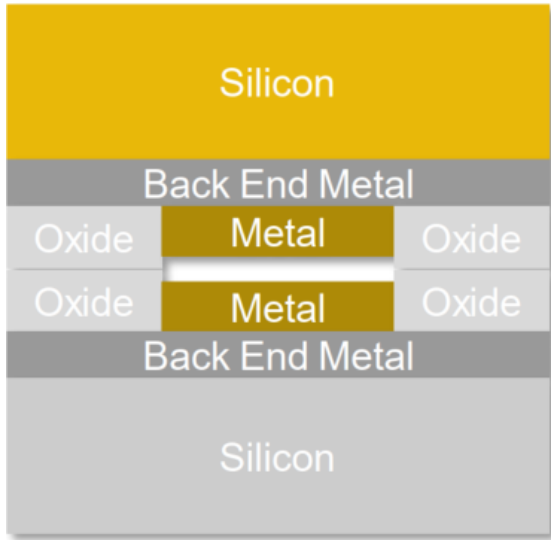
Senior Staff Process Engineer
Intel - NSG Santa Clara Architecture and Technology Scaling (ATS)

NCCAVS CMPUG Joint User Group Meeting
September 13, 2023

Outline

- Introduction
- Bonding surface CMP
  - Hybrid Bonding CMP Challenges
    - SiCN Surface Roughness
    - Cu Surface Dishing
  - Cu Pad Design Consideration
- Backside Grind/Thinning and Edge Trim
  - Edge Trim
  - Backside Grinding
  - Backside CMP
- Backside Metallization
  - TSV first/ TSV last comparison and challenges
  - TSV last CMP integration

Bonding Surface CMP



Technology Drivers

HWB improves CMOS performance with thermal budget reduction and reduces cost due to separate process flows.

3D Structures address the lithography challenges with the bottleneck shifted to etch process.

Hybrid bonding can be used to produce many stacks reliably by reducing the demands on the etch process.

TSV first, TSV last as well as TSV middle processes are available.

Key Challenges/Opportunities/Trends/Areas for Bonding Surface CMP

Challenge#1 Bonding surface energy control to increase bond strength of SiCN/SiCN

Minimum rms surface roughness of SiCN

Effective removal of residual particles on SiCN

Challenge#2 Electrical conductivity control through metal (Cu) quality, surface preparation (roughness, particles), Cu/Cu alignment

Dishing control on Cu via (Dishing height, dishing shape, dishing uniformity on wafer center to edge profile)

Planarization voids (Cu density, Cu uniformity in density/grains, Cu pad size)

Annealing voids (Cu height, annealing temperature, uniform thermal expansion)

Opportunity#1 The POR CMP set-up can be used by selection of suitable consumable set.

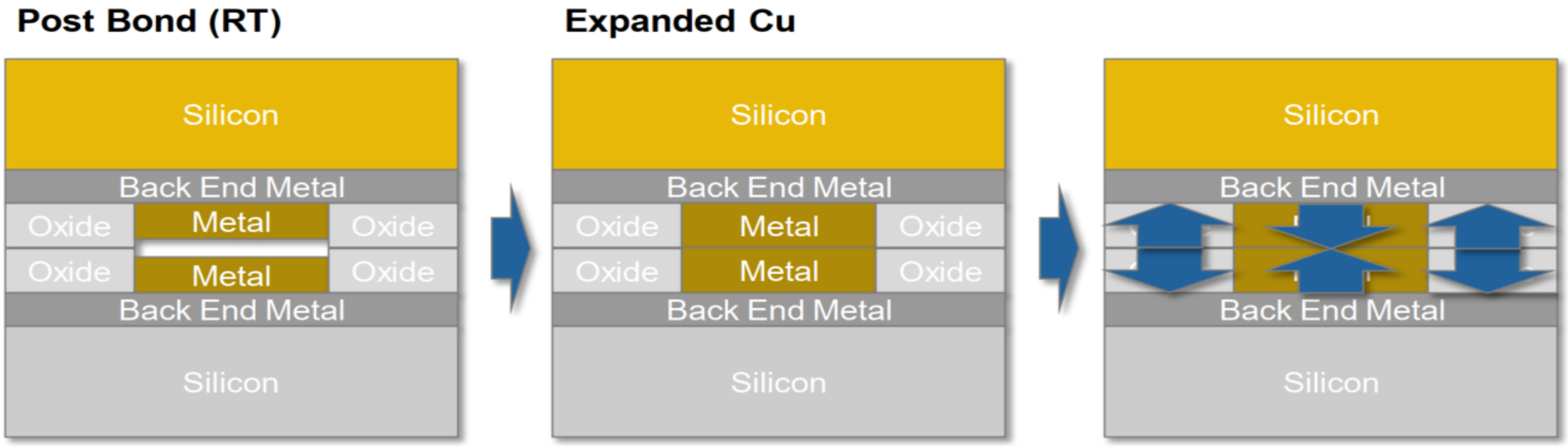
Cost

CMP tools are readily available (no fixed cost). Cost will depend on consumable sets (operational costs to be similar to any CMP application).

Supplier Landscape

Standard CMP Tools by AMAT, Ebara.

Hybrid Bonding



SiCN roughness control;

Roughness directly affects bond strength through gap closure between the two wafer surfaces.

- RMS 0.10 nm can be achieved with SiCN
- Surface cleanliness is critical
- Post CMP AFM roughness
- Particle count to be minimized

Cu Dishing Control;

Depth and shape of the Cu pad influence the electrical conductivity and potentially the bonding strength.

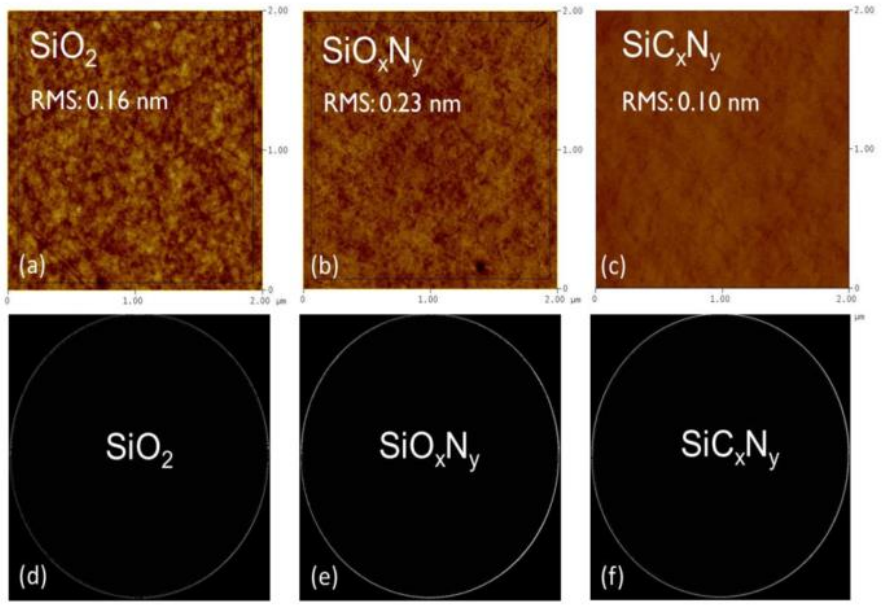
- Typically dishing is in the range of a few nm (Post CMP AFM dishing profile)
- Post CMP roughness control
- Particle count to be minimized

Cu Contact Control;

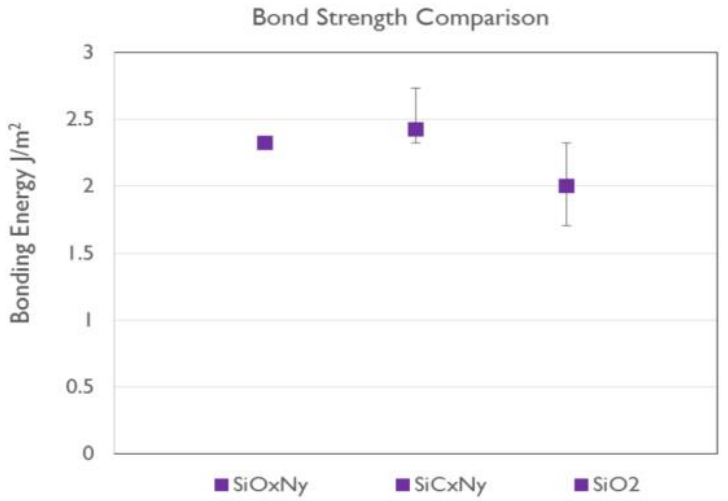
Cu expands more than the dielectric (1nm/μm/50°C)

- Cu gets into direct contact (no void)
- Cu thermal expansion depends on;
  - Cu height, Coefficient of Thermal Expansion (CTE) mismatch, annealing temperature [directly]
  - Cu film quality, film homogeneity (purity, grade, grain size) [indirectly]

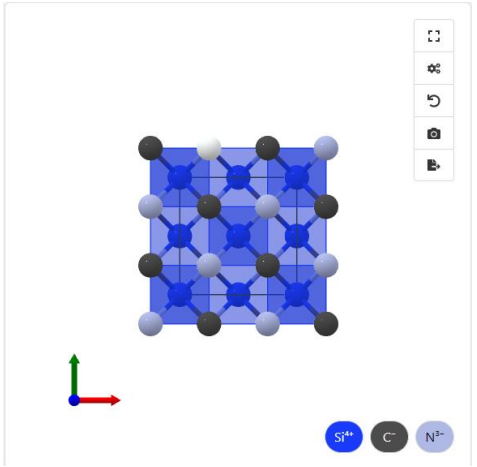
SiCN Surface Roughness



Post-CMP RMS roughness of (a) SiO2 (b) SiOxNy (c) SiCxNy SAM images of 300mm dielectric bonds (d) SiO2 (e) SiOxNy (f) SiCxNy



Bond energy of SiO_2, SiO_xN_y and SiC_xN_y with post- bond anneal of 250°C- 2hour.



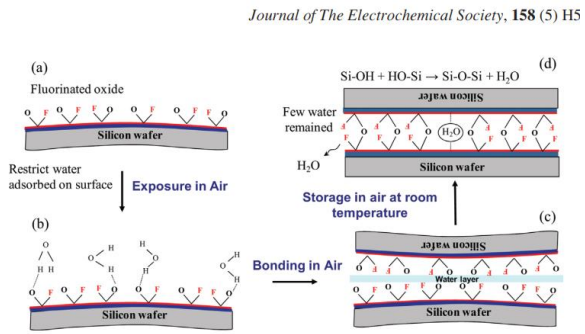


Figure 11. (Color online) Schematic illustration of room-temperature bonding of Si wafers after fluorine containing plasma activation.
Journal of The Electrochemical Society, **158** (5) H525-H529 (2011)

- CMP roughness can be directly linked to final bond strength.
- SiCxNy is the most promising dielectric with respect to surface roughness and bond strength in addition to its H storage capability.

ST Microelectronics & LETI: S. Lhostis, A. Farcy, E. Deloffre, F. Lorut et al., presented at Electronic Components and Technology Conference ECTC in Las Vegas (2016) .

Cu Dishing Control

Void in the Dielectric Interface

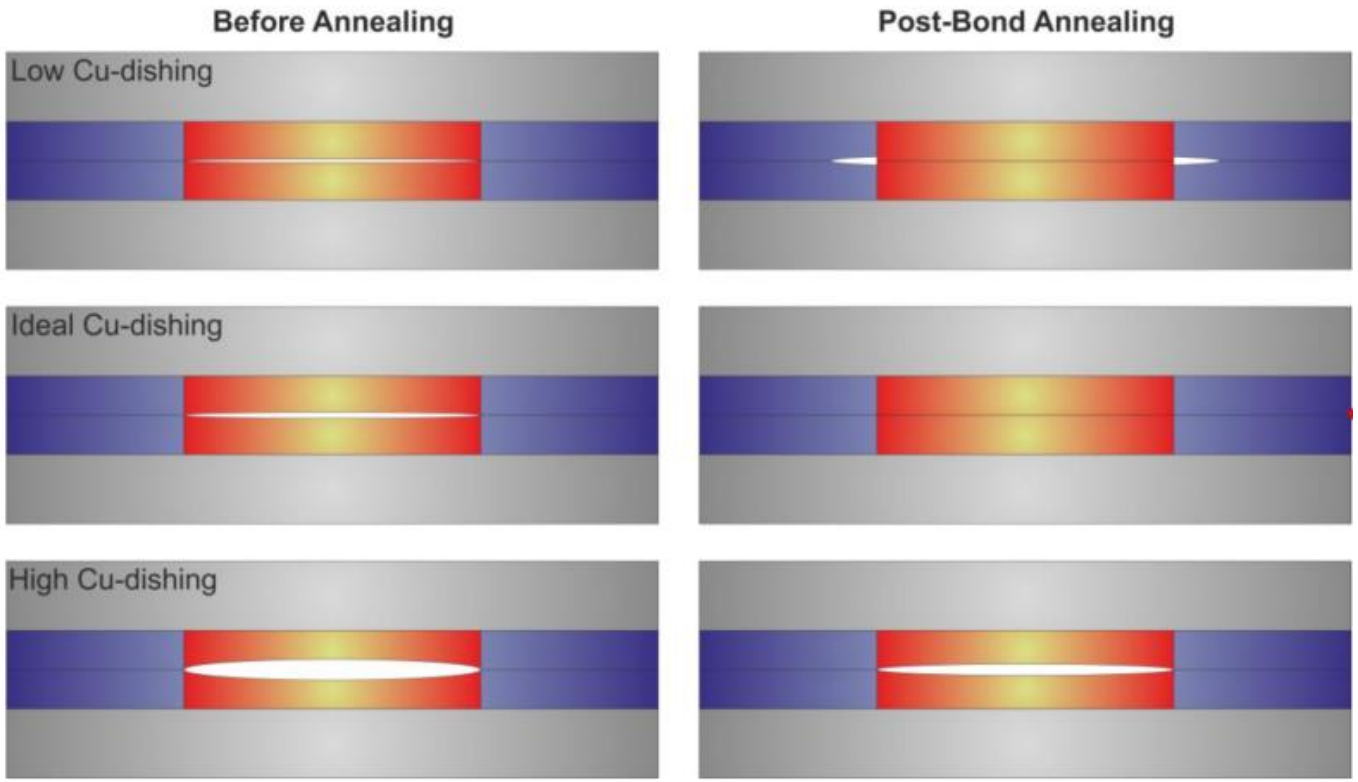
Too little dishing, too high anneal temperature

Ideal Contact

Dishing is filled by thermal expansion through anneal (~ 300/400 ° C anneal).

Void in the Cu Interface

Too much dishing, too low anneal temperature



- CMP dishing control is needed within a few nm (1-5 nm) range with adequate (~400 ° C) anneal temperature [1].
- A close loop metrology can be set up to tune the annealing temperature by the dishing gap.
- Lower Cu surface roughness leads to more efficient contact area formation [2].

J. P. Mudrick at al., "Sub-11:11tm Pitch Hybrid Direct Bond Interconnect Development for Die-to-Die Hybridization" SAND2019-2384C (2019).

Cu Dishing Control

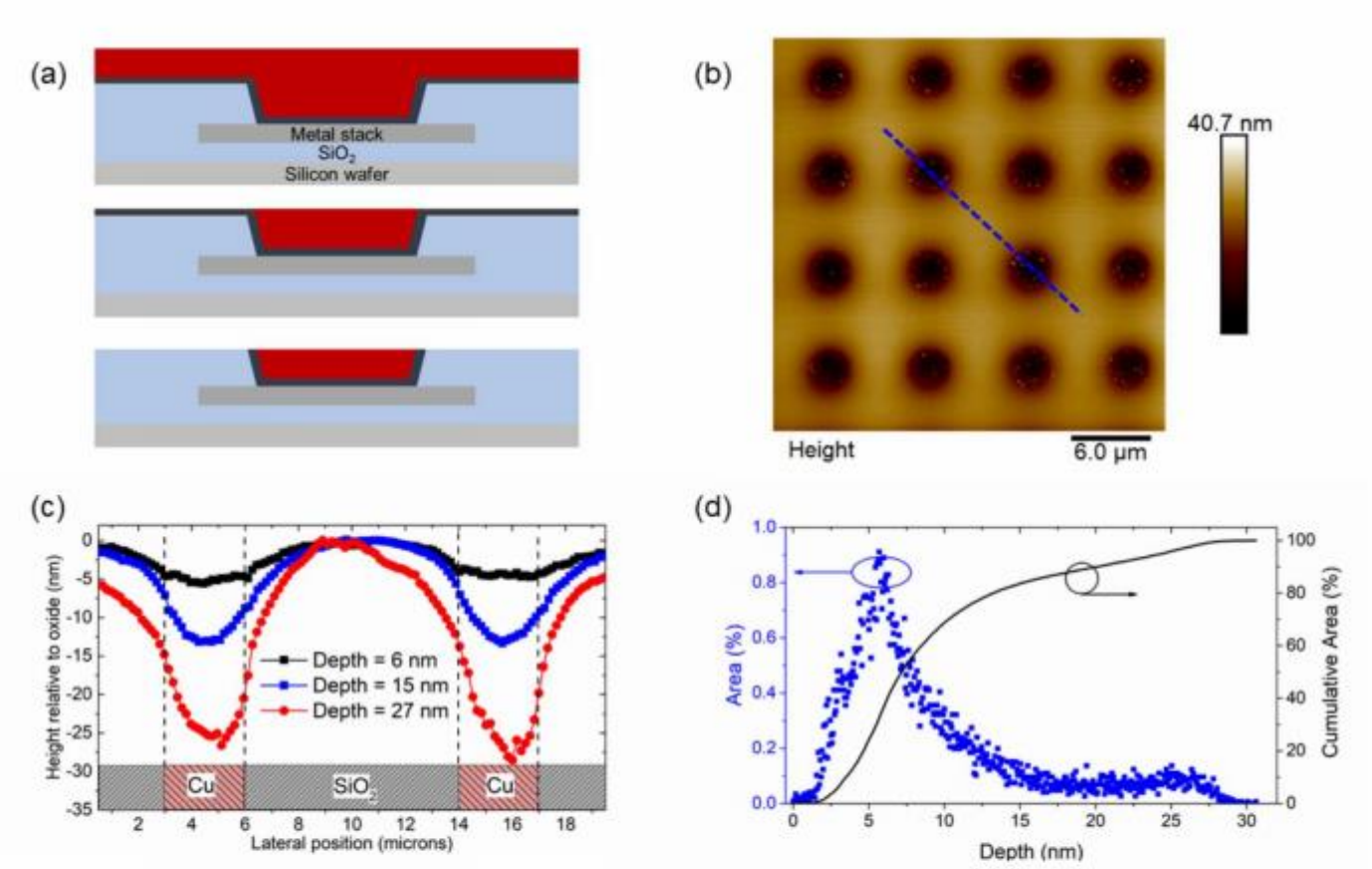


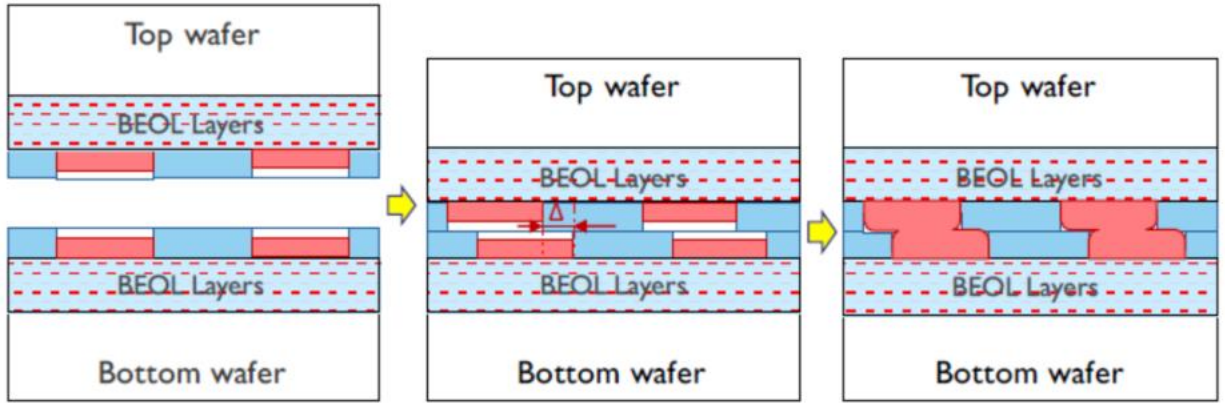
Figure 2. Hybrid bonding surface preparation and characterization. (a) Evolution of surface during CMP process; Ta is shown in gray, and Cu is shown in red. (b) Typical AFM topography scan showing recessed Cu plugs. (c) Line profiles of three wafers with different recess depths corresponding to the blue dashed line in (b). (d) Depth histogram of a 15 x 15 µm scan area consisting of 4 Cu plugs surrounded by SiO_2.

- Two-step CMP process to control the Cu recess depth.
- Bulk Cu removed on single platen selectively over Ta.
- High selectivity to Cu allows for the platen motor current to be utilized in determining the polish endpoint.
- Over-polish is empirically determined to synergize with the effective removal during the Ta barrier CMP stage.
- The Ta barrier layer is removed on a secondary platen leaving Cu recessed relative to the dielectric field.
- Cu recess depths between 5 and 25 nm are achieved after the first pass or after a single rework step.
- Pre-anneal Cu-Cu gap ranging from 9 to 47 nm.

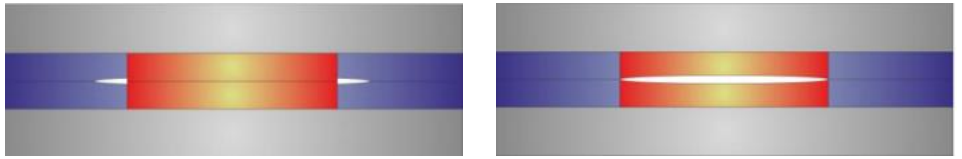
J. P. Mudrick at al., "Sub-11:11tm Pitch Hybrid Direct Bond Interconnect Development for Die-to-Die Hybridization" SAND2019-2384C (2019).

Cu Pad Design Consideration

Equal Pad Size

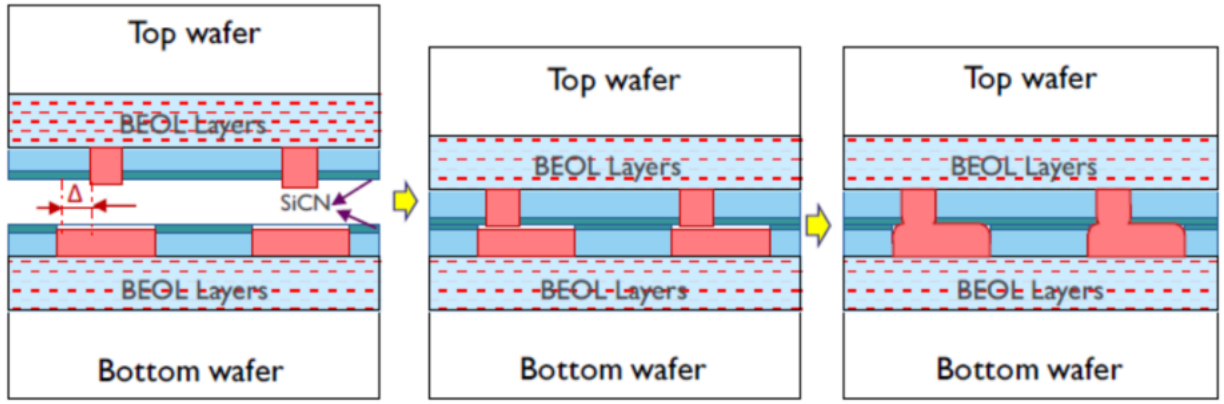


- Misalignment problem in bonding.
- Equivalent thermal expansion requiring more precise dishing and annealing control.



Dielectric void *Cu void*

Different Pad Size



- Misalignment can be compensated.
- Inequivalent dishing and thermal expansion can allow flexibility for dishing and annealing control.

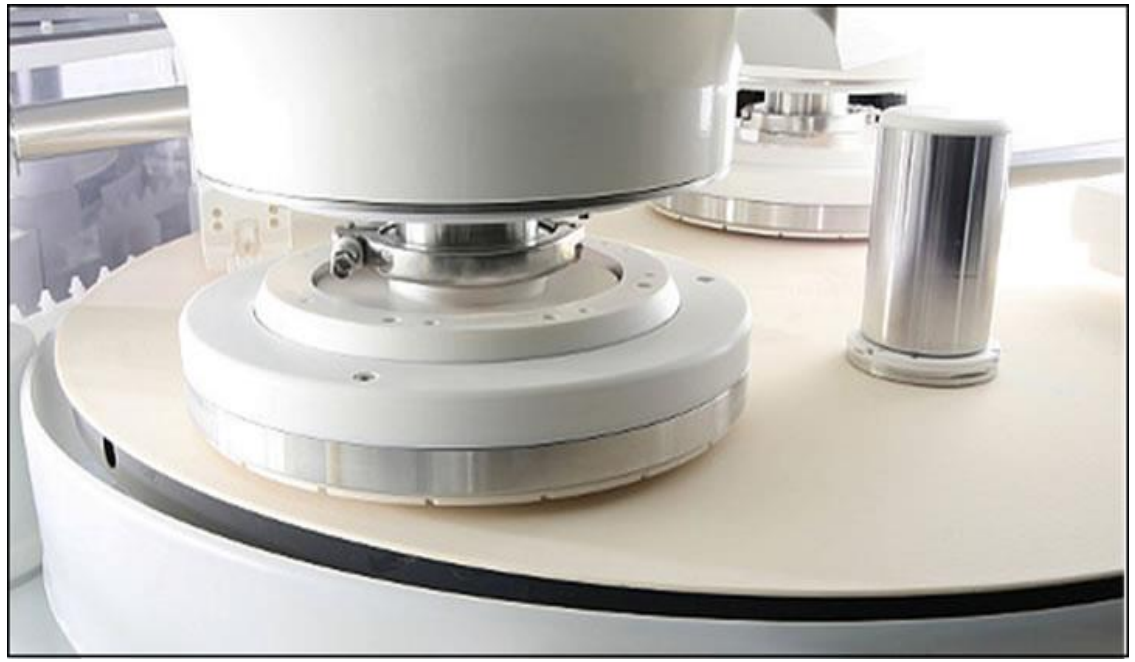
Dish less/ expand more in z-dimension. *Dish more/ expand less in z-dimension.*

- Different Cu pad size can help with CMP process margins and alignment flexibility.

CMP Hardware Options

Wafer CMP (Scrubs/cleans/metrology)

Equipment	Supplier	Comments
Wafer CMP (Scrubs/cleans/Metrology)	AMAT LK Reflection	Baseline Tool Enablement



Outline

- Introduction
- Bonding surface CMP
  - Hybrid Bonding CMP Challenges
    - SiCN Surface Roughness
    - Cu Surface Dishing
  - Cu Pad Design Consideration
- Backside Grind/Thinning and Edge Trim
  - Edge Trim
  - Backside Grinding
  - Backside CMP
- Backside Metallization
  - TSV first/ TSV last comparison and challenges
  - TSV last CMP integration

Si Backside Thinning (Edge Trim/ Grind/ Lap /CMP)]

- Technology Drivers
  - HWB improves CMOS performance with thermal budget reduction and reduces cost due to separate process flows.
  - 3D Structures address the lithography challenges with the bottleneck shifted to etch process.
  - Hybrid bonding can be used to produce many stacks reliably by reducing the demands on the etch process.
  - TSV first, TSV last as well as TSV middle processes are available.

- Key Challenges/Opportunities/Trends/Areas for Bonding Surface CMP
  - Challenge#1 Edge trim: Improves chipping of silicon.
  - Challenge#2 Wafer back grind
    - *Mechanical grinding resulting in residual stresses (CMOS wafer on top).*
    - *In situ metrology available for thickness measurement and control to compensate for any bow issues.*
  - Challenge#3 Wafer back lapping and CMP
    - *Single silicon polishing with standard DISCO/CMP toolset.*
  - Opportunity#1 Standard edge and backside trim tools are available.
- Cost
  - Edge Trim DISCO DFD6860, Wafer Backside Grind/Thinning DISCO DGP8761 HC
- Supplier Landscape
  - Current Suppliers: DISCO

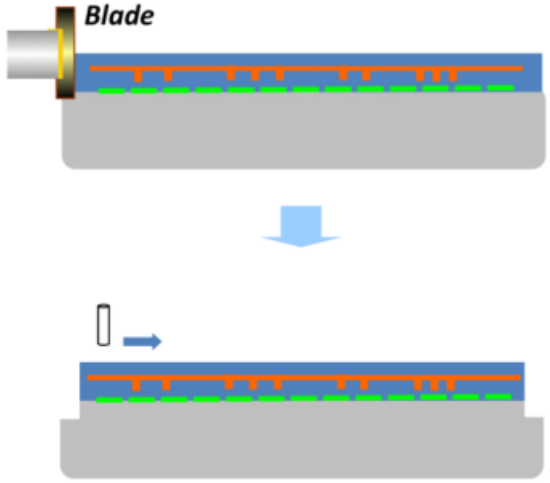
Planarization

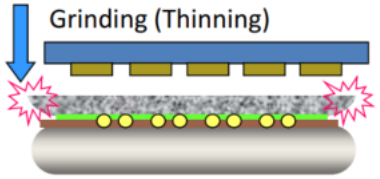
Polishing

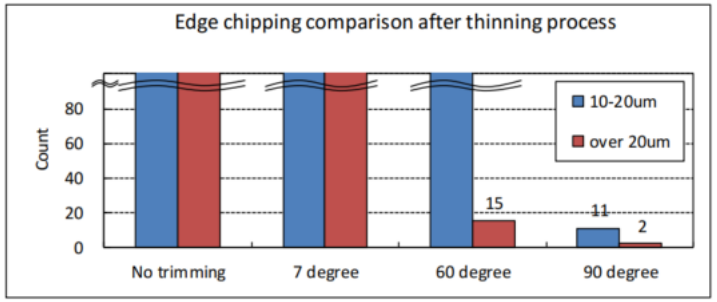
Edge Trim

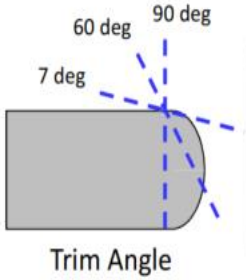
Equipment	Supplier	Comments
Edge Trim	DISCO	DFD6860

Trimming (single or multi pass)









Cleaning

- Particle (Atomizer nozzle)
- Metal cleaning (O3/Dilute HF)

- Edge trimming can improve wafer chipping after grinding (90 degrees trim angle performing the best).
- Wafer surface needs to keep in clean condition after trimming for bonding process.
- DFD6860 is capable to process edge trimming with high clean spec with Edge Trim Measurement Unit (ETMU).

Edge Trim

Manufacturer: DISCO
Model: DFD 6860
Category: SCRIBING / DICING
Vintage: 2015
Wafer Size: 12"
Equipment Details:
Dicing saw, 12"
2015 vintage.

No Edge Trimming

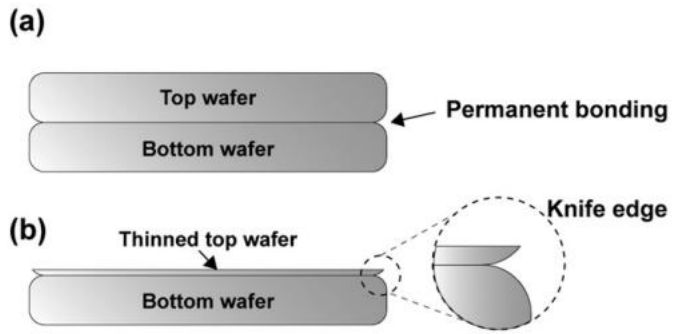


Fig. 1. Schematic images of dielectric bonding without edge trimming (a) post dielectric bonding (b) post grinding.

Edge Trimming Pre/Post Backgrind

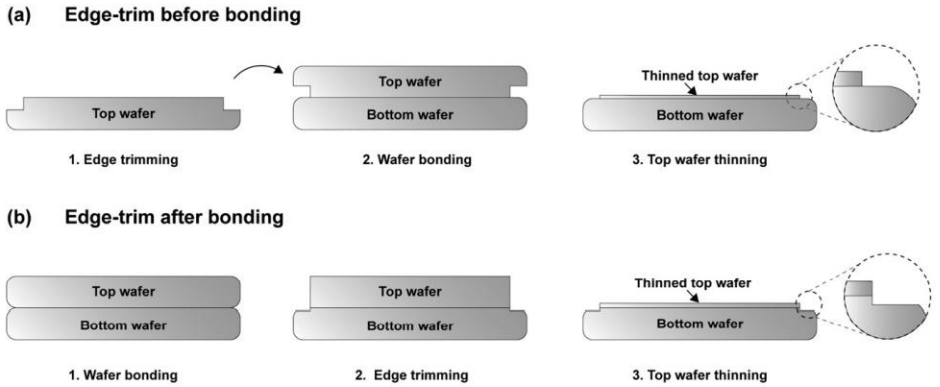


Fig. 3. Schematic illustration of edge trimming process flow (a) Edge-trim before bonding (b) Edge-trim after bonding.

Edge Trim: Blade sawing process applied on the Si wafer edge and bevel, removing the fragile edge of the wafer prior to grinding.

- *Edge-trim before bonding:* Post edge trimming wafer surface clean is important
  - *A combination of functional water cleaning such as ozone dissolved in water and ammonia scrub cleaning shows a significant effect to remove Si residues, enabling void free dielectric bonding.*

- *Edge-trim after bonding:* Utilizing a small grit diamond blade shows no mechanical failures into the dielectric bonding interface.
  - *There is no need to optimize the post cleaning.*

These processes are very promising for the fabrication of extreme thinned Si (Si < 5 μm) without mechanical failure at wafer edge.

Fumihiro Inoue at al. "Edge trimming for surface activated dielectric bonded wafers." Microelectronic Engineering, Volume 167, 2017, Pages 10-16, ISSN 0167-9317, https://doi.org/10.1016/j.mee.2016.10.014.
Edge trimming for surface activated dielectric bonded wafers - ScienceDirect

Edge Trim

Result after grinding of permanent bonded wafer without edge preparation.

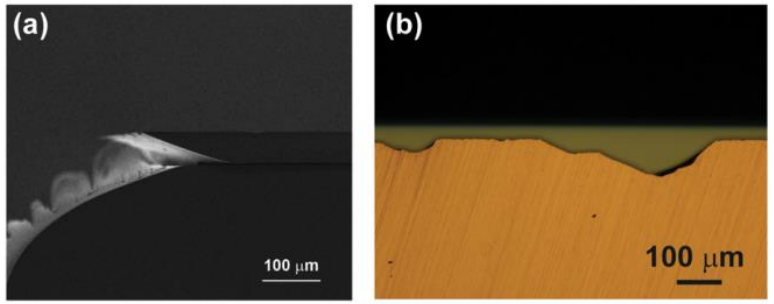


Fig. 2. (a) Cross-sectional SEM image of bonded wafer edge after top wafer grinding towards 50 µm thickness without edge trimming (b) Top OM view of wafer edge after grinding without edge trimming.

Particle count post edge trim before bonding.

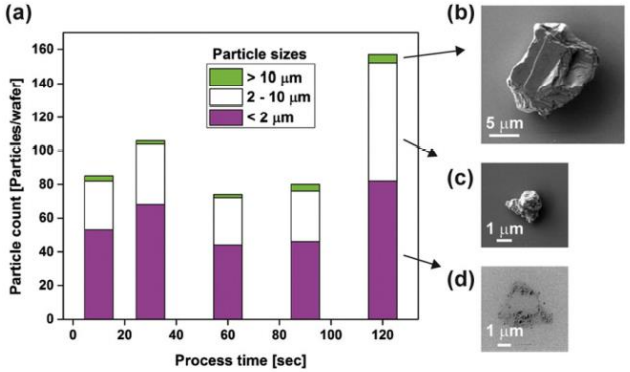


Fig. 5. (a) Particle count on blanket Si wafers after edge-trim before bonding for different process times of atomizing water. Top view SEM image of typical particles at (b) > 10 µm range (c) 2–10 µm range (d) 0.5–2 µm range.

Effect of blade grit size.

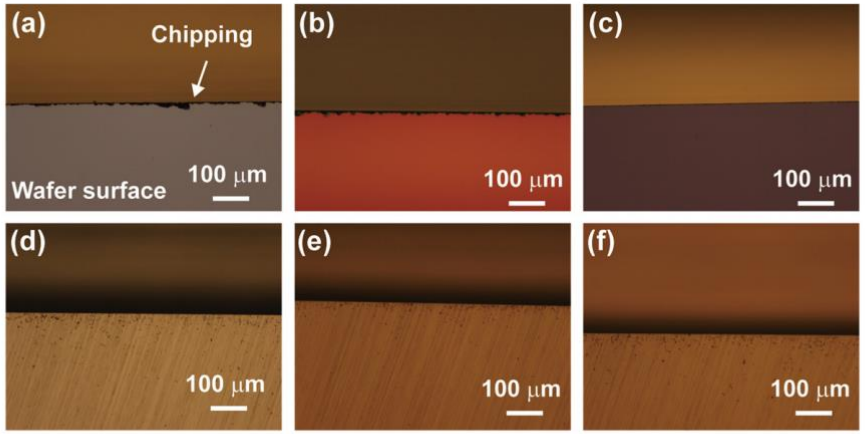


Fig. 9. Top view of OM images at wafer edge (a)–(c) after edge trimming and (d)–(f) after grinding towards 50 µm. (a) and (d) #400 blade was used for edge trimming, (b) and (e) #1000, (c) and (f) #1500 blade. The grinding conditions are exactly the same for all wafers.

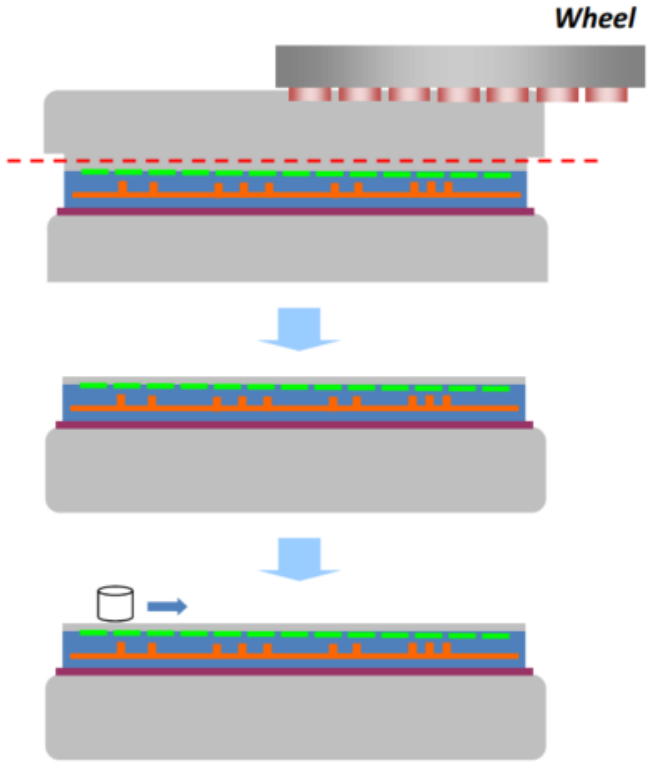
Recommendations;

- Post bonding edge trimming to prevent particle defects
- Use small grit size blade for smoother surface and better interface.
- Defects formed on the sidewall by edge trimming are similar to the ones formed by grinding on the Si surface**.

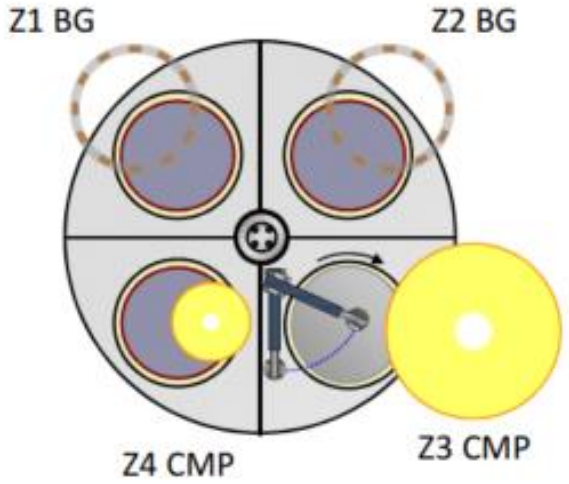
Fumihiro Inoue at al. "Edge trimming for surface activated dielectric bonded wafers." Microelectronic Engineering, Volume 167, 2017, Pages 10-16, ISSN 0167-9317, https://doi.org/10.1016/j.mee.2016.10.014.
Edge trimming for surface activated dielectric bonded wafers – ScienceDirect
Fumihiro Inoue at al. "Edge Trimming Induced Defects on Direct Bonded Wafers." Transactions of the ASME, Vol. 140, SEPTEMBER 2018.

Wafer Grind/Thinning

Equipment	Supplier	Comments
Wafer Grind/Thinning	DISCO/ Lasertec	DGP8761 HC/BGM300



- Grinding process
  - *Rough grinding*
  - *Fine grinding (40um removal)*
- CMP process
  - *Main polishing (3um polish)*
  - *Final polishing (Buff/ particle removal)*
- Cleaning process
  - *Particle removal (PVA brush)*
  - *Metal cleaning （O3/Diluted HF)*



Z1: Rough grinding
Z2: Fine grinding
Z3: Main polish (CMP)
Z4: Final polish (CMP)

https://www.bing.com/videos/search?q=Backgrinding+silicon+wafers&docid=607999337222720036&mid=2EC9C2D55960C5C02CF32EC9C2D55960C5C02CF3&view=detail&FORM=VIRE

Wafer Grind/Thinning

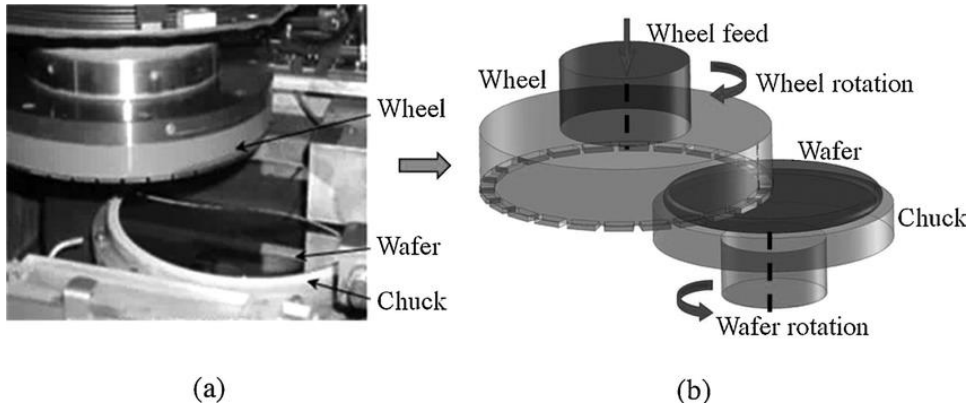
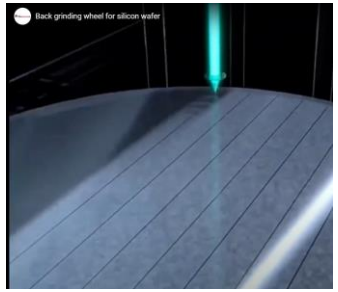
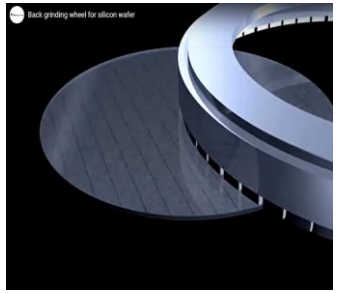


Fig. 1. Schematic of self-rotating grinding mechanism: (a) Experimental set up of wafer grinding; (b) Illustration of the rotating wafer and wheel*

Source: *Pei Chen et al. "Modelling and experimental study of roughness in silicon wafer self-rotating grinding." November 2017Precision Engineering 51, DOI:10.1016/j.precisioneng.





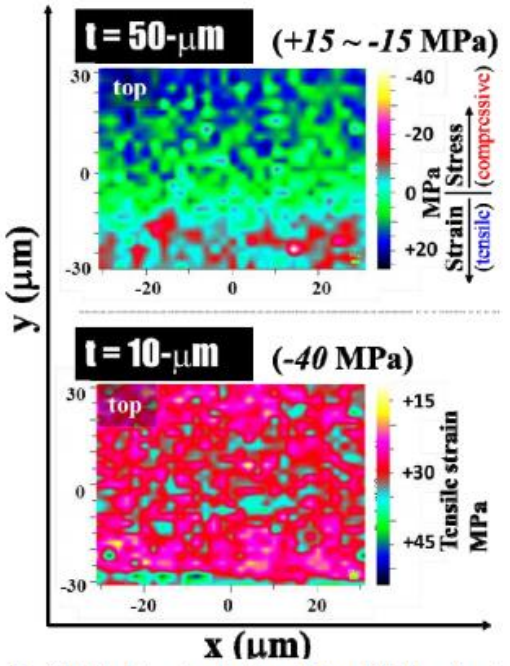


Fig. 2 Residual stress in ultra-thinned down LSI chips after stress relieved by chemical mechanical polishing.

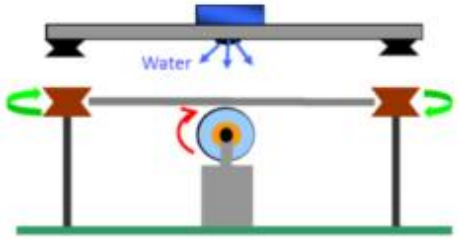
- 50 μm-thick Si chips, the residual stress after CMP process is same as the dry-polishing (DP) processed samples.
- Dry polishing is known to produce lot of sub surface damages, the relatively robust bulk mechanical strength of Si allowed the Si chips to withstand.
- Further thinning down to 10 μm leads to introduction of remnant stress of up to +40 MPa of tensile stress even in the CMP processed chip.
- This observation reveals that ultra-thinned LSI wafers are under severe stress, which may lead to chipping and cracking.**

Source: *Mariappan et al. "Yield Enhancement and Mitigating the Si-Chipping and Wafer Cracking in Ultra-Thin 20μm-Thick 8-and 12-Inch LSI Wafer." May 2015, DOI:10.1109/ASMC.2015.7164435 Conference: ASMC2015

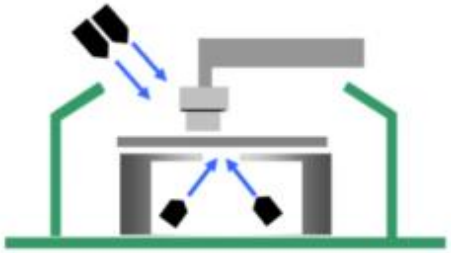
https://www.bing.com/videos/search?q=Backgrinding+silicon+wafers&docid=607999337222720036&mid=2EC9C2D55960C5C02CF32EC9C2D55960C5C02CF3&view=detail&FORM=VIRE

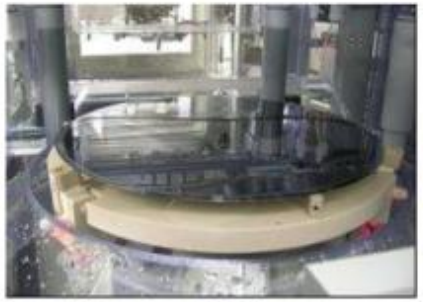
Backside Clean

- Backside cleaning
  - PVA roll brush cleaning with DIW
  - Edge cleaning available as option



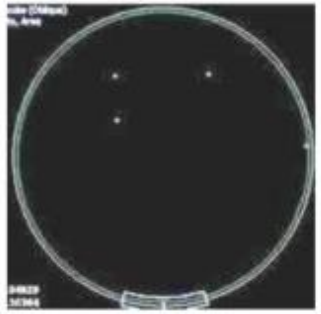
- Spinner cleaning with chemical cleaning options
  - O3
  - DHF
  - SC-1 (NH3)
  - Atomizing Nozzle for DFD6860
  - PVA Scrub for DGP8761HC





	DGP8761HC	DFD6860
Defect level	0.2um↑: < 10 pcs with Z4	0.2um↑: < 10 pcs adders
Metal level	5E+10 atoms/cm2 >	5E+10 atoms/cm2 >

Results based on DISCO recommended cleaning conditions. Wafer frontside.



https://www.disco.co.jp/eg/products/polisher_etcher/dgp8761.html

CMP Hardware Options

Equipment	Supplier	Comments
Edge Trim	DISCO	DFD6860
Wafer Grind/Thinning	DISCO/ Lasertech	DGP8761 HC/ BGM300
Wafer CMP (Scrubs/cleans/Metrology)	DISCO/AMAT	DISCO/Baseline Tool Enablement

Outline

- Introduction
- Bonding surface CMP
  - Hybrid Bonding CMP Challenges
    - SiCN Surface Roughness
    - Cu Surface Dishing
  - Cu Pad Design Consideration
- Backside Grind/Thinning and Edge Trim
  - Edge Trim
  - Backside Grinding
  - Backside CMP
- Backside Metallization
  - TSV first/ TSV last comparison and challenges
  - TSV last CMP integration

Backside Metallization

- Technology Drivers
  - HWB improves CMOS performance with thermal budget reduction and reduces cost due to separate process flows.
  - 3D Structures address the lithography challenges with the bottleneck shifted to etch process.
  - Hybrid bonding can be used to produce many stacks reliably by reducing the demands on the etch process.
  - TSV first, TSV last as well as TSV middle processes are available.

- Key Challenges/Opportunities/Trends/Areas for Bonding Surface CMP
  - Challenge#1 TSV first/middle/ last can be suitable depending on the integration scheme
    - POR metallization can be utilized as possible.
  - Opportunity#1 The POR CMP set-up can be used by selection of suitable consumable set.
- Cost
  - CMP tools are readily available (no fixed cost). Cost will depend on consumable sets (operational costs to be similar to any CMP application).
- Supplier Landscape
  - Current Suppliers: Standard CMP Tools by AMAT, Ebara.

TSV First Integration

1. Via Formation

- TSV Etch
- Isolation layer
- Plating (Cu, W, Poly)
- Via CMP

2. Font Side Metallization

- Front side MLM
- CMP POR

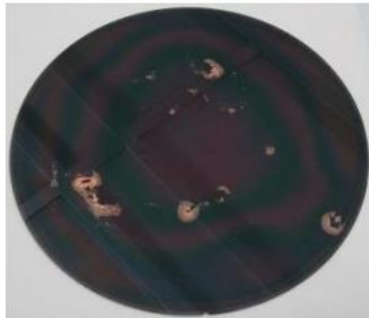
3. TSV Reveal

- Wafer backside thinning
- TSV revealed

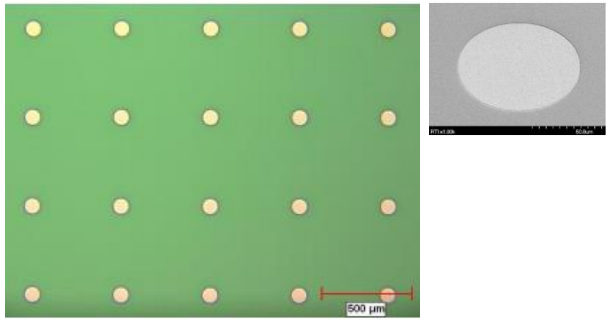
4. Back Side Metallization

- Backside metallization

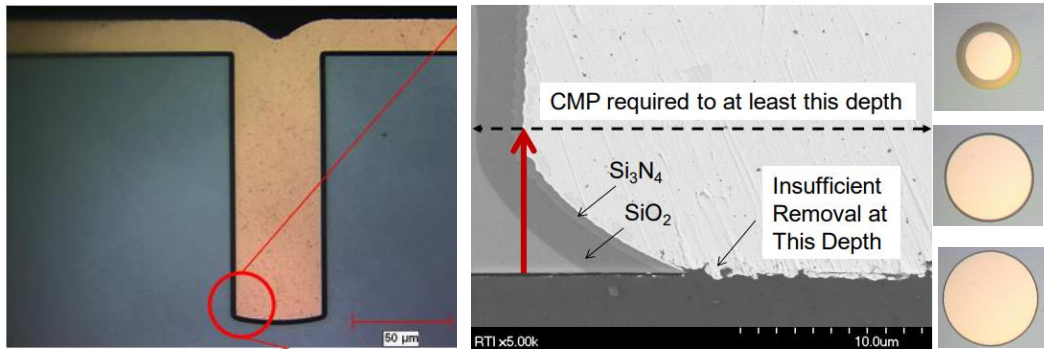
Residue



Via CMP



Backside TSV Reveal



RTI International, Inc. https://www.rti.org/publication/process-integration-and-testing-tsv-si-interposers-3d-integration-applications-2

TSV First Integration

1. Via Formation

- TSV Etch
- Isolation layer
- Plating (Cu, W, Poly)
- Via CMP

CMP Challenges:

Large via (~50-100μm)
Thick metal overburden
- *High-rate Metal Slurry (POR Cu CMP takes >20 min)*
- *Metal Residue**
- *Selective to nitride/liner post barrier clear*
- *Metal Dishing (~ 1 μm across 80 μm via)*
- *Good surface finish on both metal and dielectric.*

2. Font Side Metallization

- Front side MLM
- CMP POR

3. TSV Reveal

- Wafer backside thinning
- TSV revealed
- Protect via

CMP Challenges:

Backgrind silicon
- *Stop 3-15μm before hitting TSV*
- *Single crystalline silicon*

CMP
- *Reveal TSV & polish/smoothen Si post grinding*
- *Planarize silicon, barrier, liner and metal*
- *Selective to metal/barrier/silicon*
- *Metal Dishing (~ 1 μm across 80 μm via)*
- *Polish far enough to remove rounded profile**

4. Back Side Metallization

- Backside metallization
- SiCN/BLOK Dep
- Oxide Dep TEOS
- Oxide buff CMP?
- Via Pattern
- Via Etch
- Cu metallization

RTI International, Inc. https://www.rti.org/publication/process-integration-and-testing-tsv-si-interposers-3d-integration-applications-2

TSV First and Last Comparison

TSV First

Approach

- TSV can be integrated with final via formation.
- Backgrind + silicon CMP (reveals TSV)
- Backside grind/CMP has dual action => smoothens the background silicon and reveals the via simultaneously.

Challenges

- Etch variation can make TSV reveal difficult (where to stop?)
- Incomplete TSV reveal can cause opens.
- Defects/scratches.

TSV Last

Approach

- Front side process remains POR.
- Backside etch will be independent of the silicon thickness profile (WIW).
- Si Backgrind/CMP is stop in film and no selectivity needed.
- TSV etch+ Liner + Metal Dep+ Metal CMP.

Challenges

- Photo alignment is needed.
- Post silicon backgrind, silicon planarization and surface roughness is important for photo process/TSV etch.

CMP Hardware Options

Wafer CMP (Scrubs/cleans/metrology)

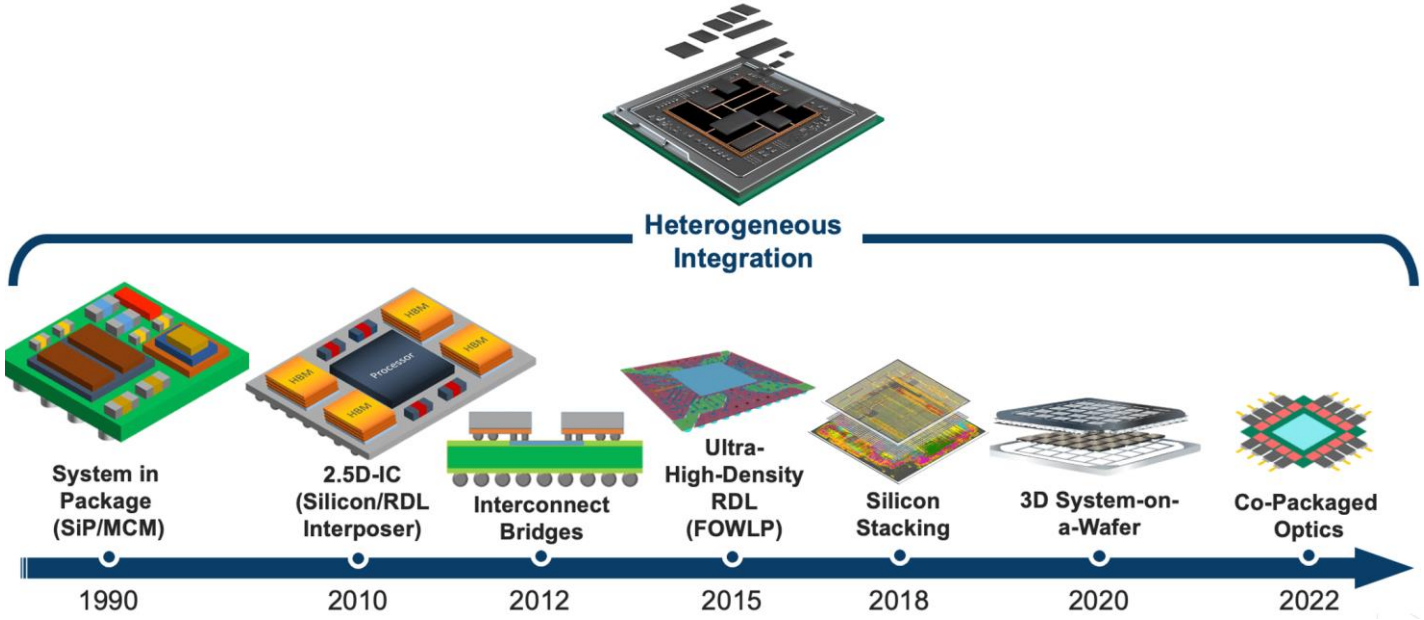
Equipment	Supplier	Comments
Wafer CMP (Scrubs/cleans/Metrology)	EBARA/AMAT	Baseline Tool Enablement

CMP BKMs on HWB

- Bonding surface Cu pad mismatch is preferred for dishing control flexibility.
- TSV to be on the CMOS wafer (to minimize pressure on the array from backgrinding).
- CMP can be tuned for TSV first or TSV last application. Will follow TSV last as per PI inputs.
- Post bonding edge trimming is suggested to prevent particle defects.
- Use small grit size blade for smoother surface and better interface.
- Integrated metrology to control edge trimming and backgrind total thickness variation for backside grinding (or to measure TSV reveal in case TSV first).
- Toolset alternatives maybe needed.

What is Forthcoming?

Heterogeneous Integration



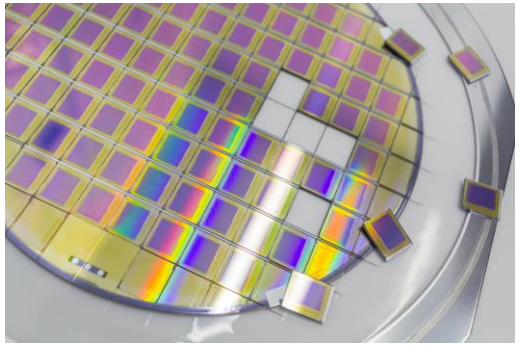
- On-die: Si with optical devices (InP/ Ge)
- In Interposer: Devices of various materials and nodes integrated
- Complex: MEMS, biosensors, chemistry, optics

https://semiengineering.com/mechanical-challenges-increase-with-chiplet-integration/
https://www.youtube.com/watch?v=6eQ7P2TD7is

https://www.anandtech.com/show/16823/intel-accelerated-offensive-process-roadmap-updates-to-10nm-7nm-4nm-3nm-20a-18a-packaging-foundry-emib-foveros

Thin Silicon

Conventional



Ultrathin Silicon

- Double side polished 8-12um and single side polished 90um available by VSI.
- Improved surface micro-roughness and total thickness variations.
- Specifications can not presently match those of standard Double Side Polished or Haze-Free Wafers.
- Surface cleanness and handling needs attention (wafers float away).
- Suitable for sensor manufacturing (100-150mm diameters available)

https://www.virginiasemi.com/?cont_uid=18

The Electrochemical Society
Advancing solid state & electrochemical science & technology

DONATE

ABOUT ECS | MEMBERSHIP | PUBLICATIONS | PROGRAMS | MEETINGS

245TH ECS MEETING

- GENERAL INFORMATION >
- SUBMIT ABSTRACTS
- REGISTRATION INFO
- AUTHOR INFORMATION
- HOTEL RESERVATIONS
- VISA & TRAVEL
- CALL FOR PAPERS

EMAIL SIGN UP

HOME / MEETINGS / 245TH ECS MEETING

245th ECS Meeting

May 26-May 30, 2024 | San Francisco, CA

The 245th ECS Meeting takes place in San Francisco, CA, from May 26-May 30, 2024, at the San Francisco Marriott Marquis. This international conference brings together scientists, engineers, and researchers from academia, industry, and government laboratories to share results and discuss issues on related topics through a variety of formats such as oral presentations, poster sessions, panel discussions, tutorial sessions, short courses, professional development workshops, and exhibits. The meeting's unique blend of electrochemical and solid state science and technology provides an opportunity and forum to learn and exchange information on the latest scientific and technical developments in a variety of interdisciplinary areas.

IMPORTANT DATES

Deadlines:

Abstract submission opens | August 2023

Abstract deadline | December 1, 2023

Travel grant submission period | December 1, 2023-February 26, 2024

Registration and hotel block opens | February 2024

ECST submission site open | February 16-March 15, 2024

To exhibit | March 15, 2024

To sponsor | March 15, 2024

Early registration | May 6, 2024

D - DIELECTRIC SCIENCE AND MATERIALS

D01 - Chemical Mechanical Polishing 17

This symposium brings together engineers and scientists from around the world to address both fundamentals and current research topics in this vital planarization and surface finishing technology. The symposium also discusses particle synthesis, emerging applications, and other relevant issues of this enabling technology.

Abstracts are being solicited in the following areas:

- CMP fundamental science and technology
- Heterogeneous integrations enabled by CMP
- CMP surface reactions and electrochemical effects
- Novel abrasives and synthesis techniques
- CMP of SiC and other wide bandgap materials
- CMP of III-V and II-VI materials
- Post CMP cleaning
- Other emerging applications of CMP

Deadline for New Submissions: Friday, 1 December 2023

Begin a Submission

https://ecs.confex.com/ecs/245/cfp.cgi

Questions/Comments?