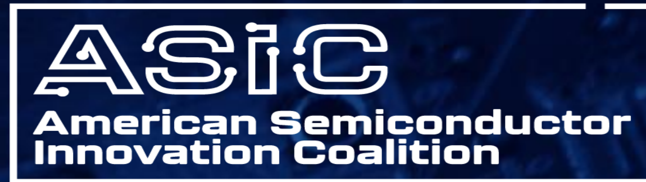

The CHIPS Act-related National Advanced Packaging Manufacturing Program (NAPMP)

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February 23, 2023
September 13, 2023 (update)

www.asicoalition.org

Acronyms

- **ASIC** – American Semiconductor Innovation Coalition
- **COE** – Coalition of Excellence
- **IAC** - Industry Advisory Committee (to CHIPS)
- **IDM** – Integrated Device Manufacturer
- **NAPMP** –National Advanced Packaging Manufacturing Program
- **NGMM –** Next Generation Microelectronics Manufacturing (DARPA)
- **NSTC** – National Semiconductor Technology Center
- **OSAT** – Outsourced Semiconductor Assembly and Test

Contents

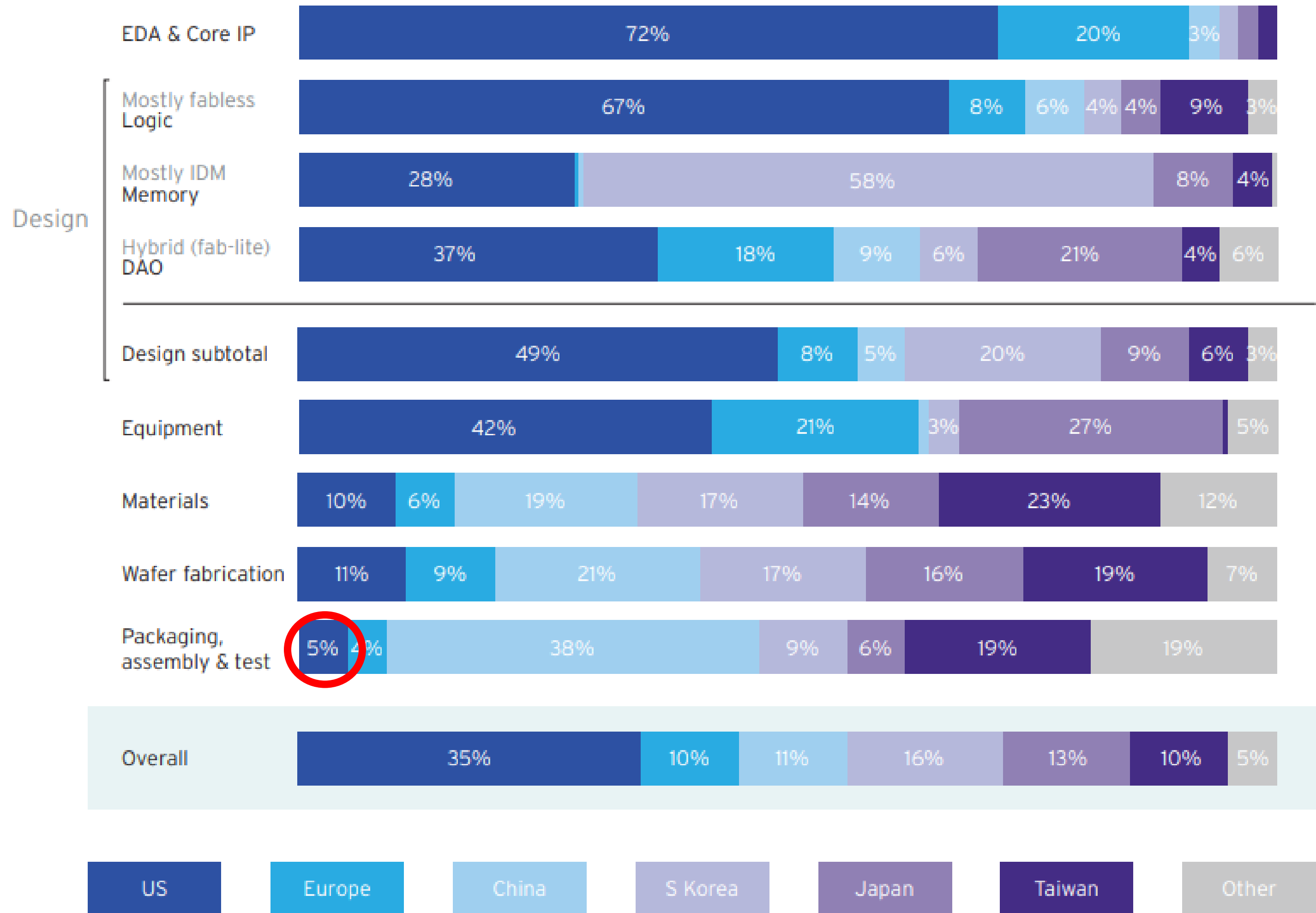
- **Problem Statement** – very limited US self-sufficiency in Semiconductor Packaging
- **Solution: CHIPS Act** – $52B over 5 years for Semiconductor and Packaging R&D
- **ASIC** – American Semiconductor Innovation Coalition
- **NAPMP** – Proposed ASIC Framework for the National Advanced Packaging Manufacturing Program

The US Houses only ~5% of the Packaging Industry (by Value Added)

Negative Implication:

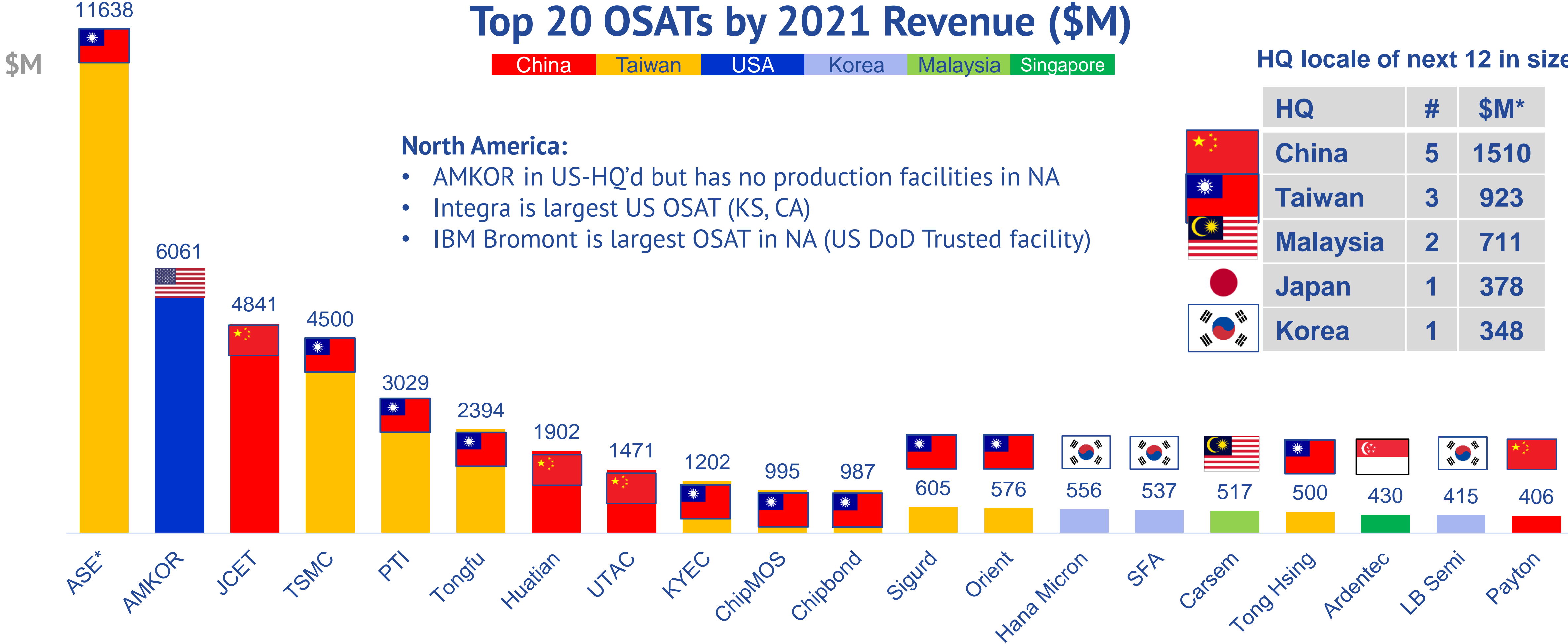
- Surety of Supply

Packaging Assembly & Test is the weakest link in the Supply Chain for the United States.



Source: SIA, State of the Industry report, Nov'22

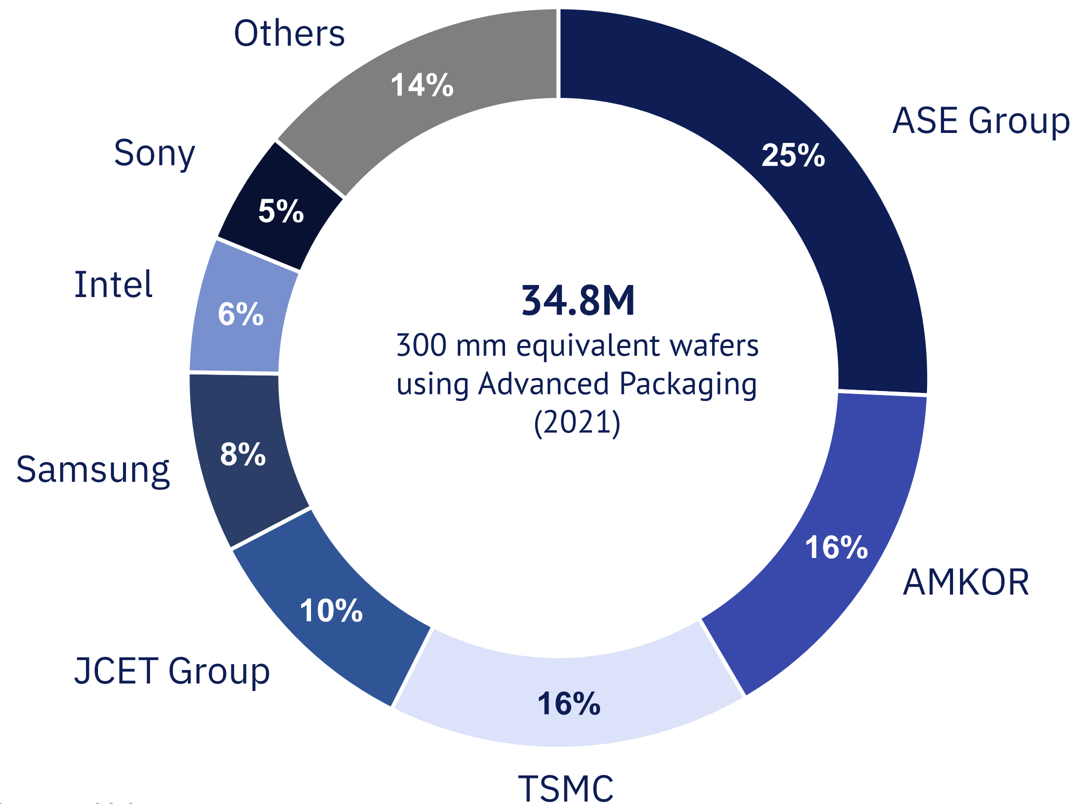
China & Taiwan Dominate the OSAT Landscape



HQ	#	$M*
China	5	1510
Taiwan	3	923
Malaysia	2	711
Japan	1	378
Korea	1	348

Source: Yole

6 Companies Package 80% of wafers using Advanced Packaging



Company	HQ	Advanced Packaging Main Factory Location(s)		
ASE Group	Taiwan	Taiwan	China	Korea
AMKOR	USA	Korea	China	Taiwan
TSMC	Taiwan		Taiwan	
JCET Group	China	Korea	China	Singapore
Samsung	Korea		Korea	
Intel	USA	Vietnam	China	Malaysia

Advanced Packaging includes: all flip chip, all wafer level packaging technologies, and all 2.x and 3D technologies.

>50% of the World’s Packaging Facilities are in China + Taiwan

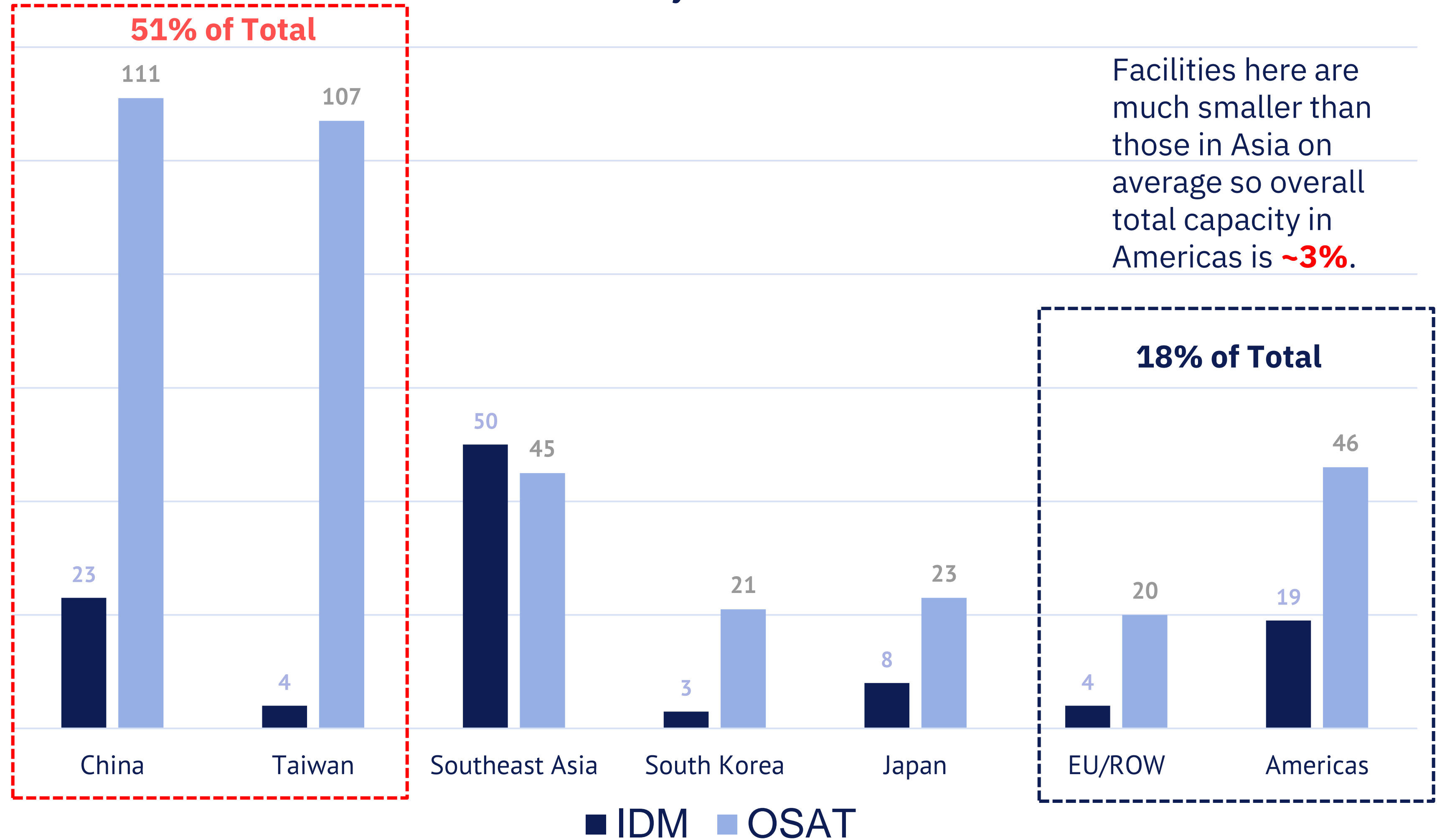
Implied Capacity is even higher

Global Packaging Facilities:

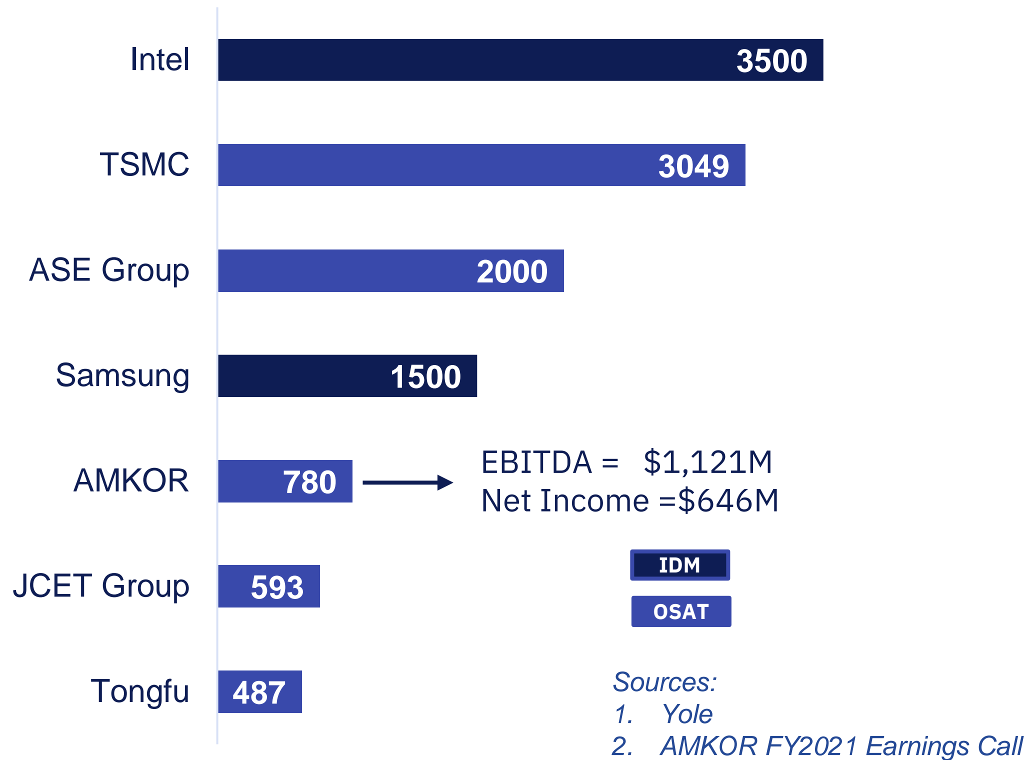
- 373 OSAT (77%)
- 111 IDM (23%)

The majority are focused on legacy packaging technology (e.g. >100 facilities offering QFN)

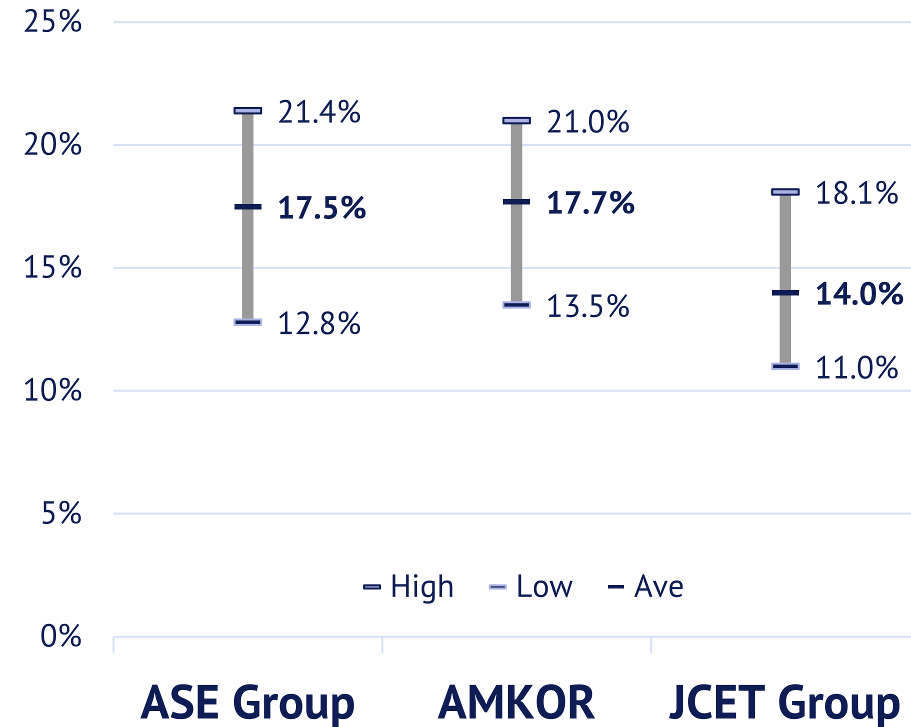
Source: SEMI, OSAT Database



OSAT Manufacturing in US has two Major Barriers to Entry



Sources:
1. Yole
2. AMKOR FY2021 Earnings Call



...and this with all major manufacturing operations being in Asia.

Financial sustainability is a problem even if you have the initial CAPEX to launch.

CHIPS Act Overview

Background

- Called for by DPAA of 2021
- Approved by Congress and signed into law in August 2022 with $52.7B of funding over 5 years as part of the larger CHIPS and Science Act ($280B total)
- Section 9906 b calls for creation of an Industrial Advisory Committee (IAC)
- Section 9908 calls for the President to investigate applications of the Defense Production Act (DPA) of 1950 to enhance US capabilities in these areas within 180 days of the CHIPS Act enactment

All amounts in US$B

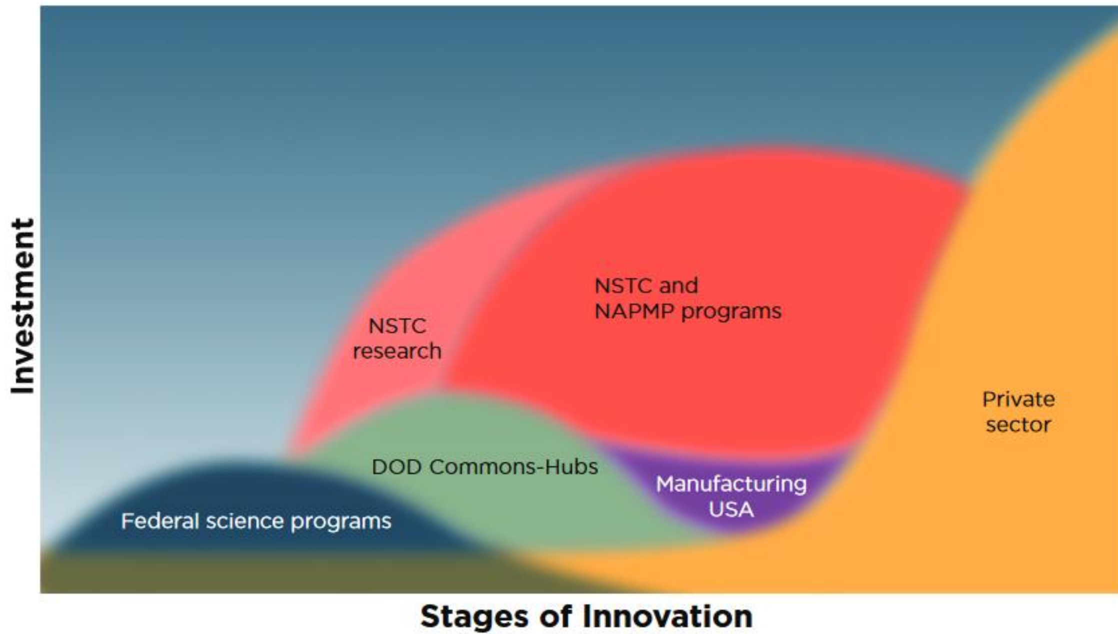
Section	Subject Matter	FY2023	FY2024	FY2025	FY2026	FY2027	TOTAL
9902	Incentives Program	19	5	5	5	5	**39**
9903	ME Commons	0.4	0.4	0.4	0.4	0.4	**2**
9905	Security	0.1	0.1	0.1	0.1	0.1	**0.5**
9906 c	NSTC	2	2	1.3	1.1	1.6	**11**
9906 d	NAPAMP	2.5					
9906 e	Microelectronics Research at NIST	0.5					
9906 f	Manufacturing USA Institutes						
	Workforce and Education Fund*	0.025	0.025	0.05	0.05	0.05	**0.2**
							52.7

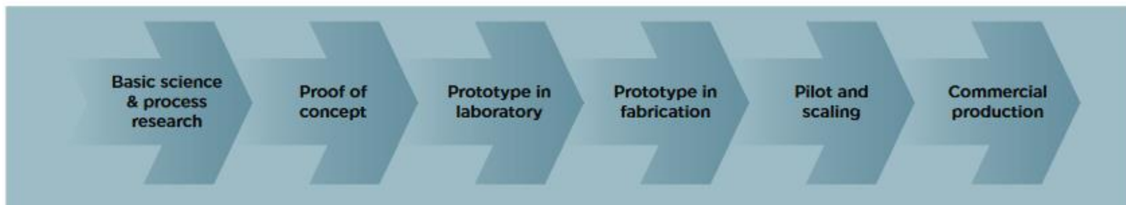
*to be administered through NSF

Source: Information derived from https://www.bennet.senate.gov/public/_cache/files/4/0/40919cb4-ff63-4434-8ae2-897a4a026b30/7BCDD84F555A6B85BEC800514F1D3AFD.chips-and-science-act-of-2022-section-by-section.pdf

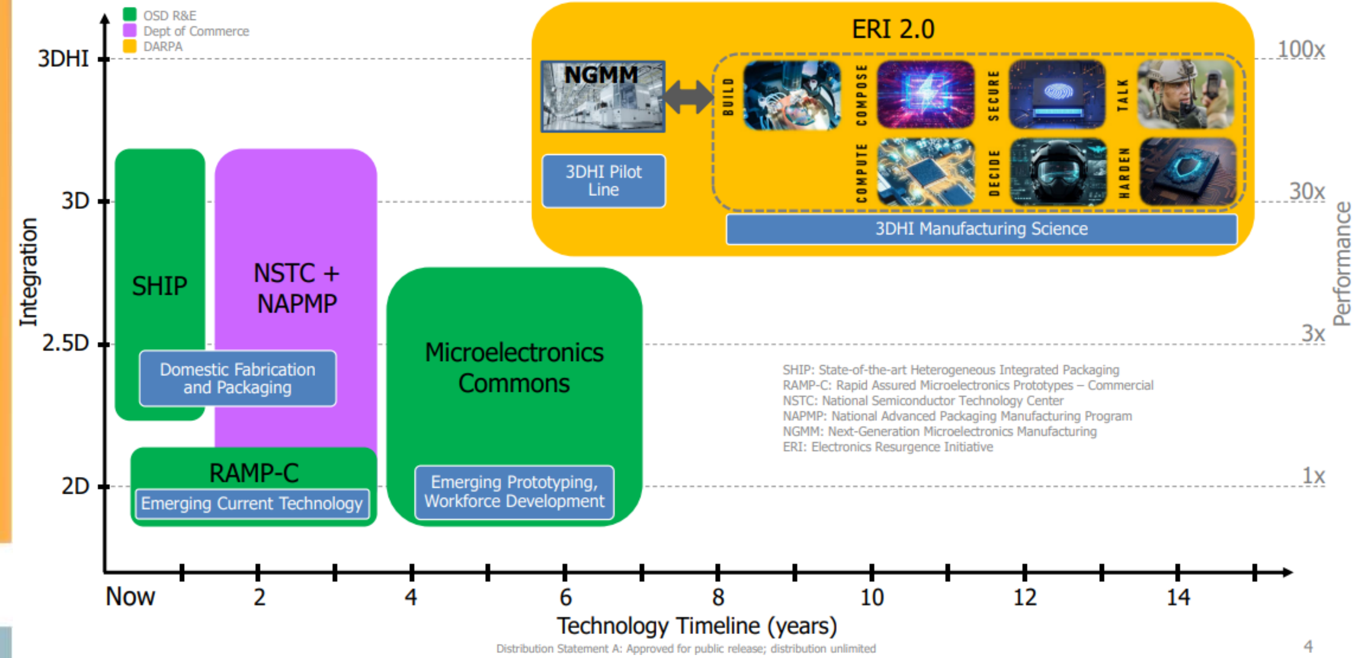
Two Government Agency Views of Program Positioning

Dept of Commerce View





DARPA View

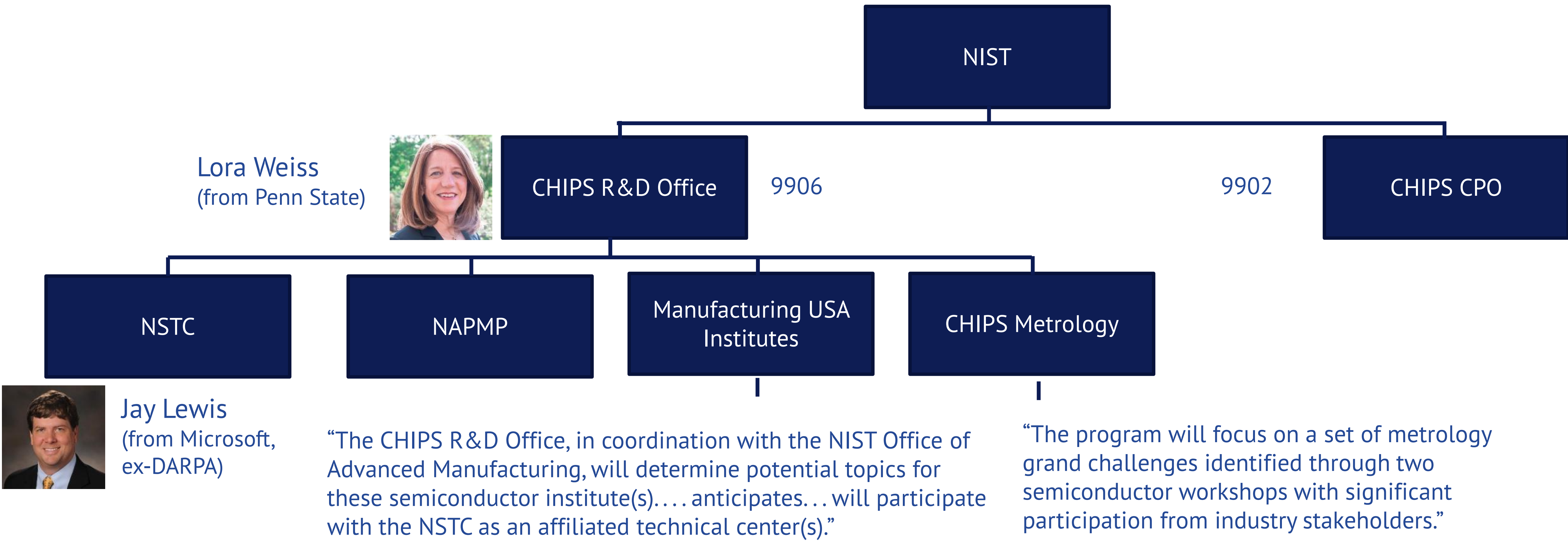


Reasonably consistent views . . .

Source: DoC/NIST White Paper on NSTC

CHIPS R&D Office

- Led by R&D Director, reporting to the Under Secretary of Commerce for Standards and Technology
- Will manage the development of NSTC, NAPMP, Manufacturing USA Institutes, and CHIPS Metrology Program [all of 9906]
- “Separate from but coordinated with CHIPS Incentive Program” [9902]

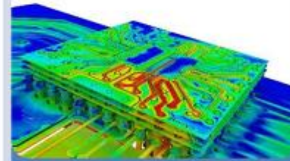


Source: ”CHIPS for AMERICA: A Vision and Strategy for the National Semiconductor Technology Center, CHIPS R&D Office, April 25, 2023

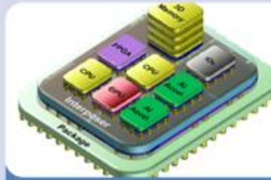
National Advanced Packaging Manufacturing Program (NAPMP)

NIST

Technology innovation	Create an R&D environment advancing the state-of-the art in advanced packaging.
Ecosystem support	Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.



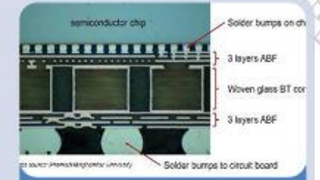
Co-design and simulation



Chiplets

Pilot packaging facilities

Tooling and automation



Materials and substrates

- The NAPMP will utilize the NSTC to support (a) packaging facility(ies) that enables R&D efforts
- **Prototype and pilot scale integration** of components fabricated in NSTC facilities or 3rd party sources
- Baseline packaging flows to support a goal of **established package proven IP**

Source: "CHIPS for America Research and Development Update," E. Lin, presented at the June 6, 2023 IAC Meeting

- The facility should have **sufficient tool redundancy** to allow **groundbreaking research** on new materials and processes while still **maintaining baseline capacity**
- **Partnerships with domestic OSATs** and electronics manufacturing services (EMS) to facilitate migration of successful prototypes to a production manufacturing environment

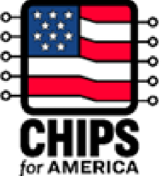
Chip R&D Dept. Mandate to Create a Chiplet Program

"**Chiplets:** Developments on chiplets cut across many core NSTC and NAPMP activities: standards, roadmaps, technical centers, and the multi-project wafer program. The Department expects the NSTC to work with the NAPMP to **create a chiplet program** that plays a leading role in **driving standards** in **2D and 2.5D heterogenous integration**, as well as establishing a **long-term vision in 3D integration** of memory and logic beyond existing standards in stacked memory. NSTC-sponsored multi-project wafer programs could be used to grow an expansive library of interoperable chiplets that can be integrated with custom chiplets to demonstrate innovations with reduced investment and time. **The technical center for heterogenous integration described earlier, combined with an open chiplet platform, could play a central role in prototyping** new and emerging complex systems for transition into commercial production. Private sector companies could be created or expanded to participate in a chiplet ecosystem. In brief, the NSTC, in coordination with the NAPMP, should establish a robust chiplet program to **enable an open chiplet marketplace** and maintain U.S. leadership in a broad spectrum of silicon and non-silicon technologies."

Source: "CHIPS for AMERICA: A Vision and Strategy for the National Semiconductor Technology Center, CHIPS R&D Office, April 25, 2023

CHIP Act 9906 Gameplan by DoC Element

Program Development Timeline



	SUMMER 2023	FALL 2023	WINTER 2023
National Semiconductor Technology Center	IAC Meeting June 6th	Selection Committee identifies Board of Trustees	Establish NSTC
National Advanced Packaging Manufacturing Program		NAPMP vision and strategy paper	
Manufacturing USA institute(s)	RFI Summary Published	Select topic(s); begin proposal process	
Metrology Program (NIST)	Metrology Gaps Report Published	Select programs to begin	

NSTC Whitepaper April 25th

HINT: Sign-up for updates at CHIPS.gov

Source: "CHIPS for America Research and Development Update," E. Lin, presented at the June 6, 2023 IAC Meeting

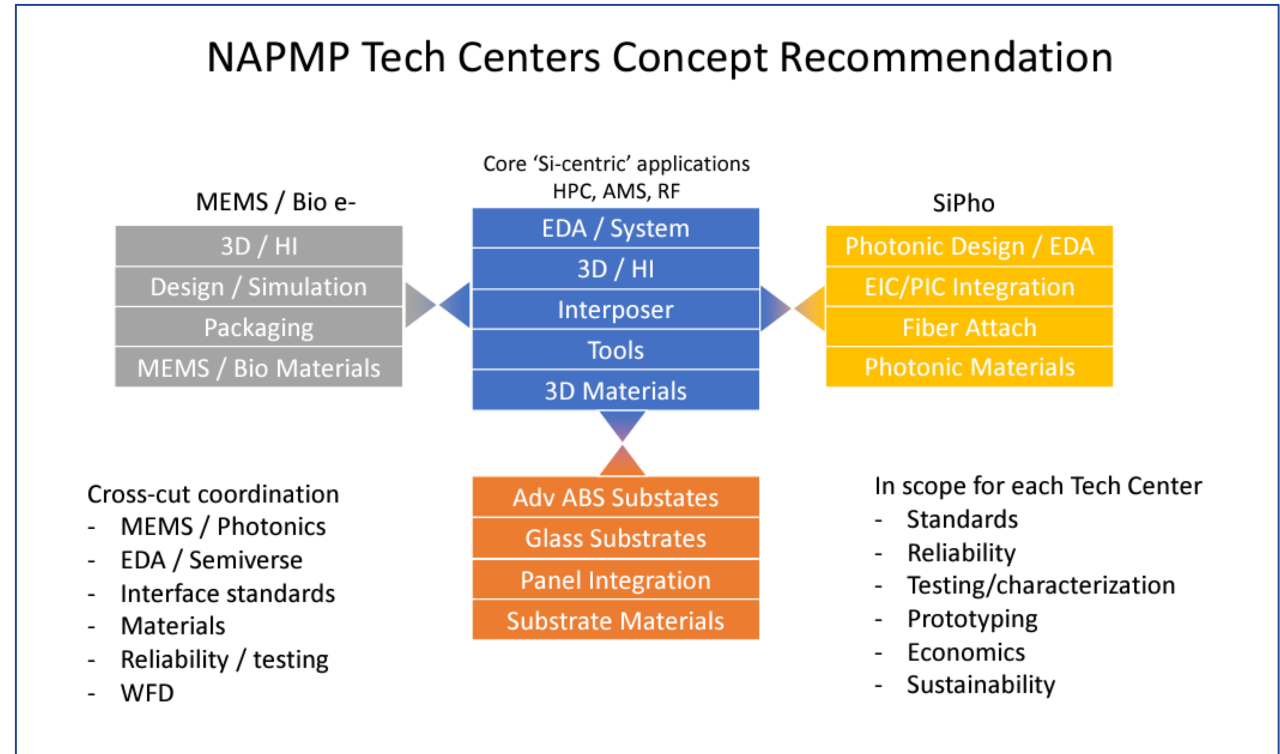
IAC Working Group Recommendations (June 6th, 2023)
Implications to both NSTC and NAPMP

Source: https://www.nist.gov/chips/industrial-advisory-committee/industrial-advisory-committee-meetings

IAC R&D Gaps Working Group Output on NAPMP

Approach (90 days)

- Reviewed 16 relevant R&D, roadmap, and ecosystem landscape reports
- Rolled up "Top 5 Focus Areas" from each working group member
- Identified key R&D gaps categories to be addressed
- Recorded perspectives from 22 experts relevant to these categories
- Prepared 10 recommendations for June 6 IAC meeting



IAC R&D Working Group recommends 4-5 NAPMP "Tech Centers"

Source: "IAC R&D Gaps Working Group," presented at the June 6, 2023 IAC Meeting

IAC R&D Gaps Working Group Recommendations

1) Ensure an **independent budget and a dedicated executive leader** for NAPMP, reporting to NSTC CEO and NSTC fiduciary board
2) Incentivize (9902) an existing **wafer- and panel-based manufacturer** to **create prototyping capabilities** in the US by establishing a pilot and initial manufacturing line, including expansion capabilities (annex) for R&D
3) Incentivize (9902) at least one existing **substrate manufacturer** to create a US pilot and initial manufacturing line and with a R&D annex to **explore advance substrate options** (including glass)
4) Ensure a robust set of programs that **establish and extend enabling processes and capabilities** such as bump and line pitches sub-5 um line/space, processing for TSVs (silicon and substrate), hybrid bonding (Wf-Wf, Die-Wf, Die-Die), etc. across multiple technologies and materials (i.e., not just silicon)
5) Identify **EDA** advanced packaging and system gaps and create pathfinding and ultimately EDA tools that can effectively co-design and system optimize all elements of **2.5 and 3D heterogeneous integration** (especially photonics, memory, RF, power, etc.) **including multi-physics capabilities**
6) Create a community of stakeholders to **build a digital twin capability from the R&D stage through manufacturing** with a **tight integration to EDA/simulation** as well as for **workforce development support and training**
7) Set grand challenges of **achieving 10x increase in productivity and 10x decrease in environmental/energy footprint** for mainstream advanced packaging capabilities, including eco-benign semiconductor manufacturing
8) Double the **U.S. advanced packaging university footprint** (from ~5 to ~10) and faculty, expand existing advanced packaging university programs by at least 50%, and build a virtual university-wide curriculum with increased funding for research and education
9) If the IAC were to call out one emerging technology to receive special attention, we believe **silicon photonics** is a rare general-purpose technology that should merit CHIPS Act investments in R&D, prototyping, and manufacturing
10) Complete a **landscape survey and gap analysis of the advanced packaging** of both supply and demand in the US (and North America) leveraging recent reports including prototyping gaps in key specialty packaging capabilities - including MEMS, photonics, power electronics, analog, and RF.

Source: "IAC R&D Gaps Working Group," presented at the June 6, 2023 IAC Meeting

Sample of Participants

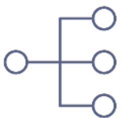
Built a Diverse Coalition - 220+ member entities including industry companies, innovation start-ups, univerisities, U.S. National Labs, key industry groups, and non-profit/consortia

Answered the NSTC/NAPMP RFI and the Manufacturing USA RFI from the US Department of Commerce - Over 90 members of the ASIC team collaborated to produce a 120-page NSTC/NAPMP response and over 25 members teamed to produce the Manufacutring USA response

NAPMP Whitepaper - Over 25 members created a 15-page whitepaper providing guidance on how the NAPMP should be organizaed and executed https://asicoalition.org/news/advancing-semiconductor-leadership-in-america-whitepaper

Social Media Channels - ASIC launched accounts on Twitter and LinkedIn

Website Launch - https://asicoalition.org/



Organization - ASIC formed working committees in the areas of Governance, IP Management, Work Force Development, Start-ups, and Technology Agenda to advise U.S. Government stakeholers

ASIC Advanced Packaging Team

Who are we? 138* members from across 79* entities

19 Universities
37 members

BU
Cornell
GaTech
MIT
Penn State
Princeton
Purdue
RPI
SUNY
U Binghamton
U Delaware
U Illinois
U Michigan
U Minnesota
U Puerto Rico
U Vermont
UCLA
UIUC
USC(ISI)

48 Companies
87 members

3D Glass
ADI
Advantest
AMAT
AMD
Analog Photonics
ASPDL
AT&S
Atomica
Canon Nano
DECA
Dupont
FormFactor
GE Research
Global Foundries
Green Source
Hyperion
i3 Micro
IBM
Integra
Jabil
Resonac
JSR Micro
Keysight
KLA
LAM
Marvell
Mercury
Mosaic
NANTERO
nepes
NGC
Nhanced
WDC
Novami
NXP
Siemens
Skywater
Sunray
TEL
Teledyne
TI
TTM
UI Corp
ULVAC
Veeco
WDC

3 Industry Assoc
3 members

iNEMI
IPC
SEMI

2 MIIs
4 members

AIM Photonics
NextFlex

3 Analysts
3 members

TechCet
TechSearch
Yole Dev

3 National Labs
3 members

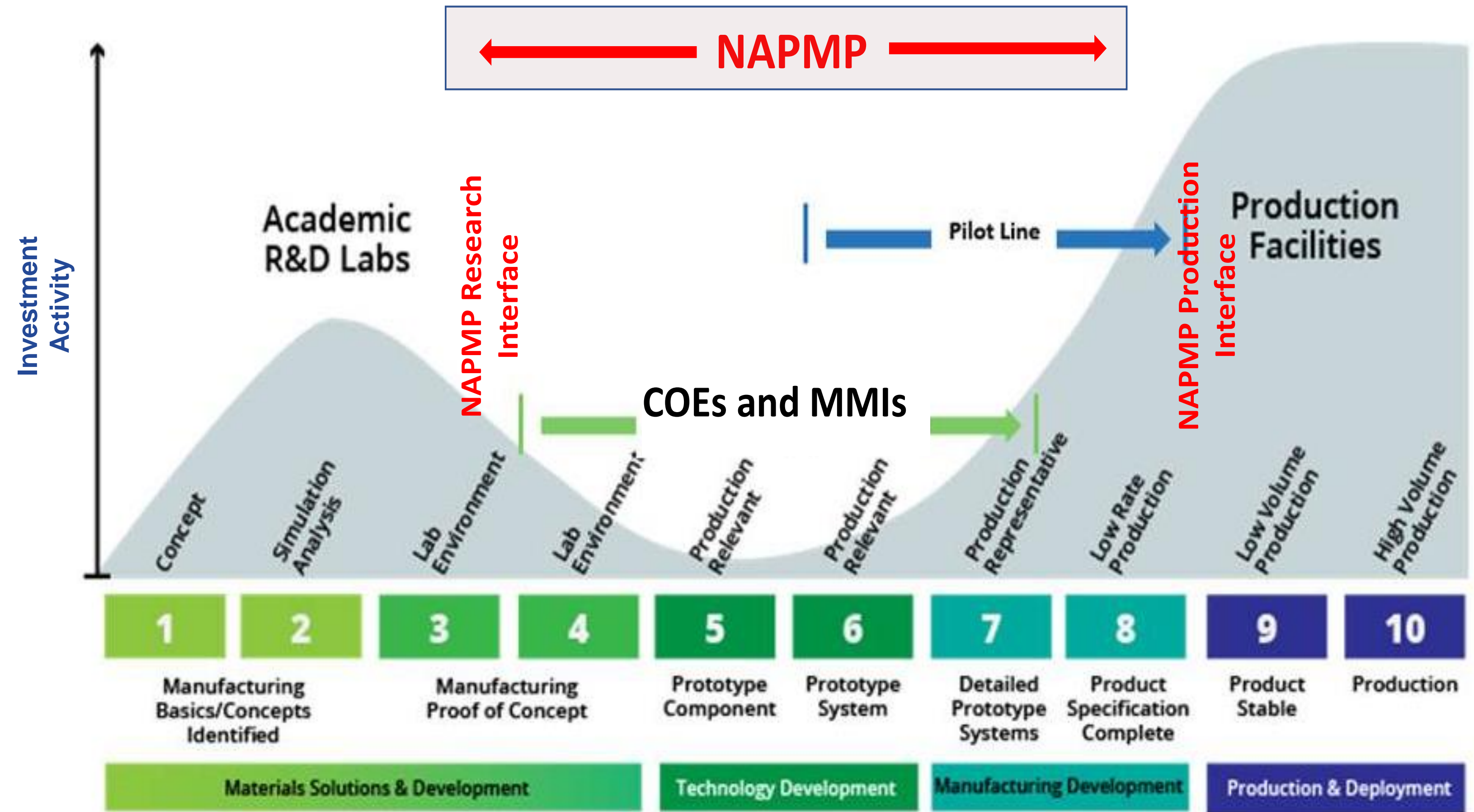
ANL
CEA-LETI
Fraunhofer

NYCreates

*from Feb'23 – more now

ASIC Interpretation of NAPMP Objectives

- Encourage and support advanced research to create totally new technologies, designs and products.
- Accelerate technology development
- Transfer new technology to US commercial production
- Support workforce development
- Maintain close links with the NSTC

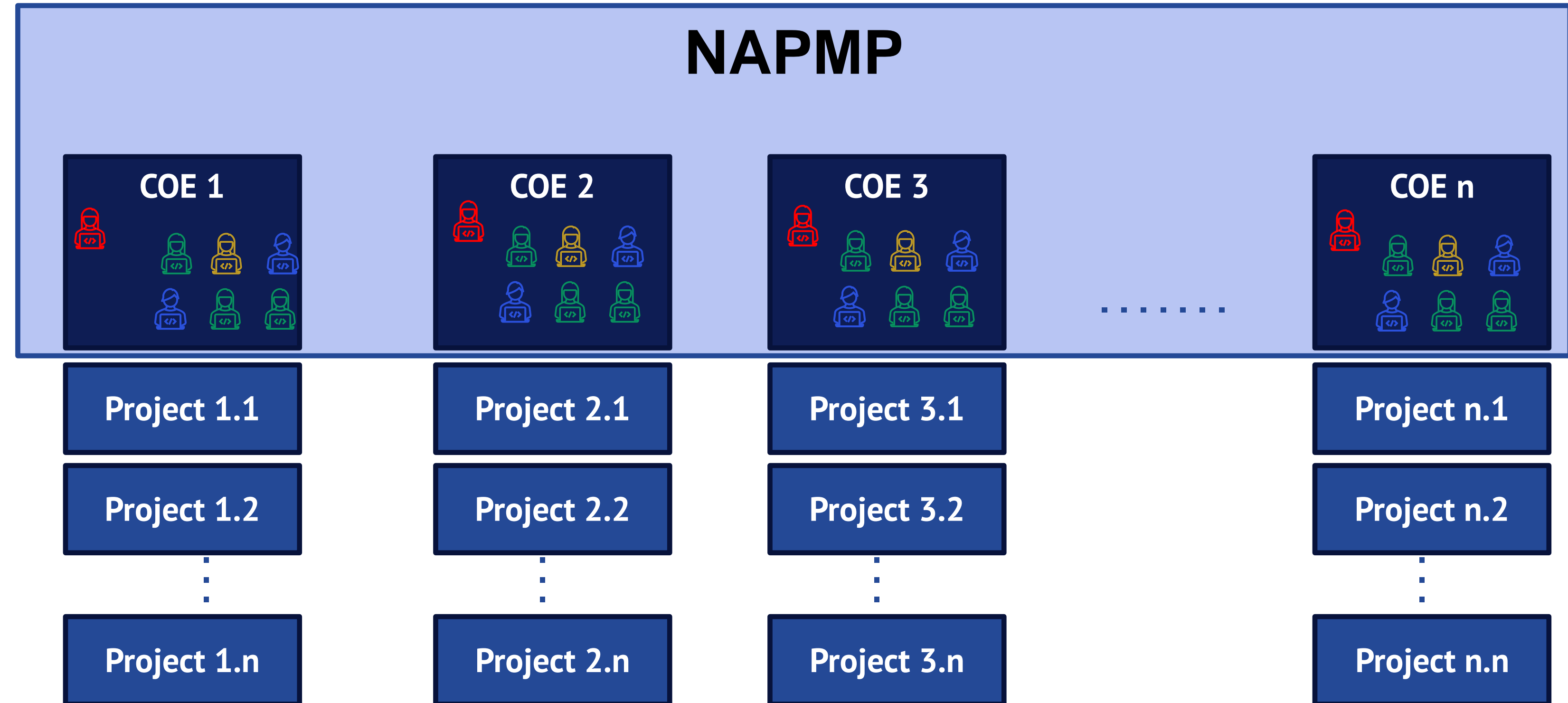


NAPMP COE Structure Proposed by ASIC

As a "Manufacturing Program", we assume the NAPMP COEs will be program focused and will not typically have their own facilities

Major tasks would be;

- Research interface
- Road mapping
- Program selection, funding, objectives, monitoring to accelerate technology development
- Transfer of technology to pilot lines



- Each COE has a specific technology theme
- COE should have industry/university inputs, along with NIST inputs, into decision making

NAPMP Coalitions of Excellence (COEs)

The COEs would focus on accelerating technology development in the NAPMP, each with a particular technology theme. Ten proposed:

- 3D heterogeneous integration
- Copackaged optics (CPO)
- Advanced SIP
- High voltage/high power
- FO-WLP (reconstituted)
- Interposers/Bridges
- Substrates
- MEMS
- Flexible Hybrid & Additive
- Cross cutting (eg thermal, reliability, DFM, etc)

Each COE would have sub-COEs to drive subsets of the technology.

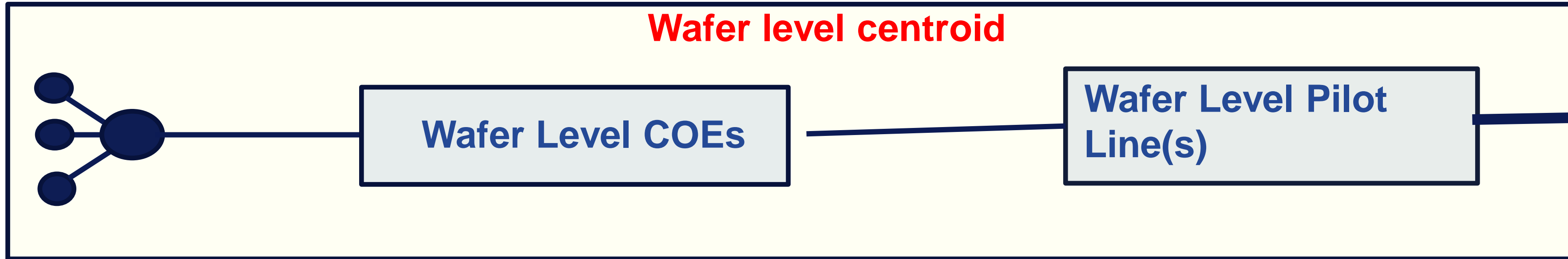
Example: 3D HI

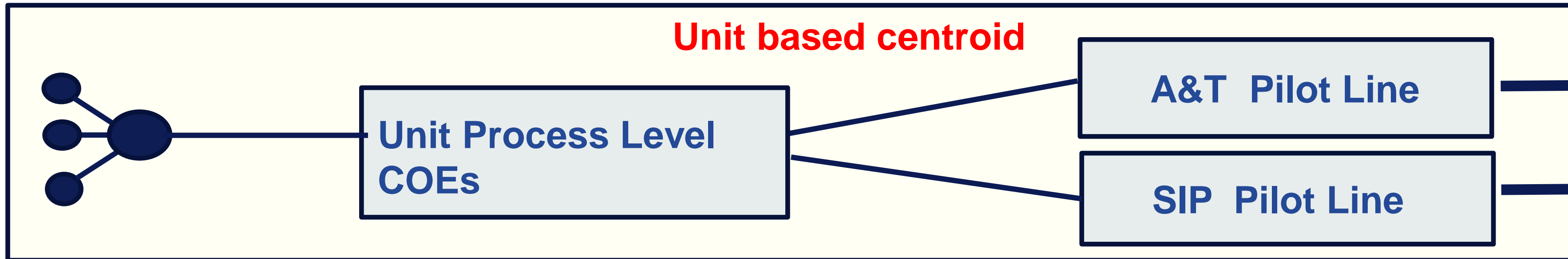
- Co-design EDA for design and test
- Hybrid bonding *[example Projects]*
  - *Bonding down to 2um bond pitch plus improved wafer finishing*
  - *Alignment to 100nm*
  - *Higher throughput tools with die speed binning capability*
  - *New materials to reduce anneal temperature*
  - *Data management for increased yield and traceability*
- Thermal dissipation
- Below surface metrology
- Reliability

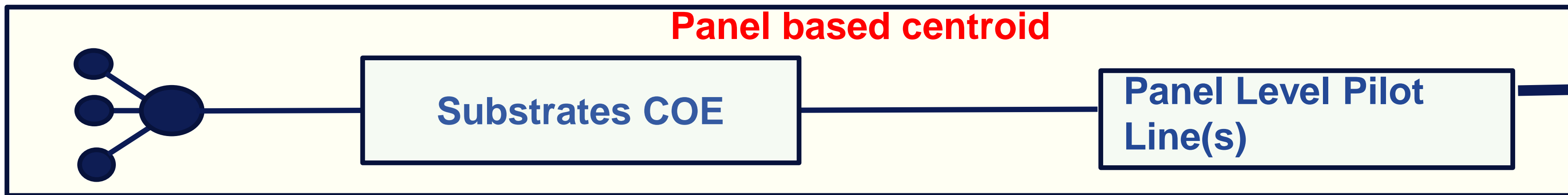
ASIC Proposed COE/Pilot Line Approach

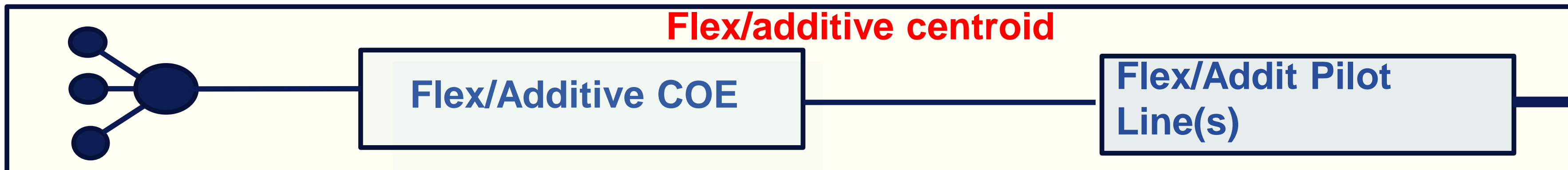
Research hub and spokes

NAPMP Activities









Manufacturing

Domestic US Manufacturing Facilities / Partners

ASIC Proposed NAPMP Success Metrics

The NAPMP needs to monitor a broad set of success metrics, both leading and trailing, covering four areas:

- Operations
- Technical
- Economic
- Workforce Development

Area	ASIC Proposed NAPMP Metrics	
Operations	▪ # of NAPMP projects taken to production in USA ▪ # of members and dues paid ▪ # of projects delivered on schedule ▪ # of projects transfer to manufacturing	▪ Budget control ▪ # of research partnerships (academic and commercial) ▪ Progress towards industry self sufficiency for the NAPMP ▪ Assess performance of each NAPMP COE
Technical	▪ Roadmap acceleration versus prior expectations ▪ US technical leadership ▪ # of technologies/processes/products transferred to manufacturing ▪ Reduced environmental footprint for packaging technologies	▪ # of breakthrough challenges supported by NAPMP developed technologies ▪ # of projects terminated for technical reasons ▪ # of patents and license revenue ▪ # of peer reviewed papers and conference presentations
Economic	▪ US production market share in semi packaging (advanced and mature) ▪ # of new jobs created in US packaging facilities ▪ Growth of new industries supported by the NAPMP (eg EV, medical etc) ▪ Growth of US based packaging foundry	▪ # of start-up companies supported by NAPMP ▪ # of packaging related start-ups reaching successful exit ▪ National security support ▪ # of projects terminated for market reasons ▪ Improved supply chain resilience (less dependence on Taiwan)
Workforce	▪ # of students in training versus goals (AA, BS, MS, PhD) ▪ % minority and retrained students (eg military) ▪ # of students hired by semiconductor packaging industry ▪ # of semi packaging centric locations, courses and programs ▪ Geographic diversity of training	▪ % students graduating in 2 years (CC) and 4 years (BS) ▪ # students hired by semi-industry ▪ Number of CCs, colleges, and universities offering courses. ▪ # of student internships (at multiple levels: 2-year, 4-year, post-grad)

Summary

- The ASIC NAPMP team has developed an organization and structure for the NAPMP built around:
  - Ten Coalitions of Excellence for accelerated technology development
  - Five Pilot Lines for economic and sustainable manufacturing hardening
  - University Focus Centers leading the university research efforts

See White Paper for details

- The NAPMP objectives are:
  - Support research activities in advanced packaging
  - Accelerate technology development
  - Develop and harden economically and sustainable manufacturable processes
  - Transfer technology for manufacture to support multiple new market opportunities
- The NAPMP will collaborate with multiple organizations including the NSTC, companies, universities and other government programs (eg NGMM, ME Commons)

To Learn more about ASIC

- Website: https://asicoalition.org/about
- Twitter: https://twitter.com/asicoalition
- Linkedin: https://www.linkedin.com/company/american-semiconductor-innovation-coalition/

www.asicoalition.org