The CHIPS Act-related National Advanced Packaging Manufacturing Program (NAPMP)

Scott Sikorski, PhD
IBM Research

February 23, 2023
September 13, 2023 (update)
Acronyms

- **ASIC** – American Semiconductor Innovation Coalition
- **COE** – Coalition of Excellence
- **IAC** – Industry Advisory Committee (to CHIPS)
- **IDM** – Integrated Device Manufacturer
- **NAPMP** – National Advanced Packaging Manufacturing Program
- **NGMM** – Next Generation Microelectronics Manufacturing (DARPA)
- **NSTC** – National Semiconductor Technology Center
- **OSAT** – Outsourced Semiconductor Assembly and Test
Contents

- **Problem Statement** – very limited US self-sufficiency in Semiconductor Packaging
- **Solution: CHIPS Act** – $52B over 5 years for Semiconductor and Packaging R&D
- **ASIC** – American Semiconductor Innovation Coalition
- **NAPMP** – Proposed ASIC Framework for the National Advanced Packaging Manufacturing Program
The US Houses only ~5% of the Packaging Industry (by Value Added)

Negative Implication:
• Surety of Supply

Packaging Assembly & Test is the weakest link in the Supply Chain for the United States.

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**SEMICONDUCTOR INDUSTRY VALUE ADDED BY ACTIVITY AND REGION 2021 (%)**

<table>
<thead>
<tr>
<th>Activity</th>
<th>US</th>
<th>Europe</th>
<th>China</th>
<th>S Korea</th>
<th>Japan</th>
<th>Taiwan</th>
<th>Other</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDA &amp; Core IP</td>
<td>72%</td>
<td>20%</td>
<td>8%</td>
<td>6%</td>
<td>4%</td>
<td>4%</td>
<td>3%</td>
</tr>
<tr>
<td>Mostly fabless Logic</td>
<td>67%</td>
<td>58%</td>
<td>58%</td>
<td>4%</td>
<td>4%</td>
<td>9%</td>
<td>4%</td>
</tr>
<tr>
<td>Mostly IDM Memory</td>
<td>28%</td>
<td>8%</td>
<td>8%</td>
<td>4%</td>
<td>4%</td>
<td>9%</td>
<td>3%</td>
</tr>
<tr>
<td>Hybrid (fabless) DAO</td>
<td>37%</td>
<td>18%</td>
<td>18%</td>
<td>9%</td>
<td>6%</td>
<td>21%</td>
<td>4%</td>
</tr>
<tr>
<td>Design Subtotal</td>
<td>49%</td>
<td>20%</td>
<td>8%</td>
<td>5%</td>
<td>20%</td>
<td>9%</td>
<td>6%</td>
</tr>
<tr>
<td>Equipment</td>
<td>42%</td>
<td>21%</td>
<td>3%</td>
<td>27%</td>
<td>6%</td>
<td>3%</td>
<td>9%</td>
</tr>
<tr>
<td>Materials</td>
<td>10%</td>
<td>6%</td>
<td>19%</td>
<td>17%</td>
<td>14%</td>
<td>23%</td>
<td>12%</td>
</tr>
<tr>
<td>Wafer Fabrication</td>
<td>11%</td>
<td>9%</td>
<td>21%</td>
<td>17%</td>
<td>16%</td>
<td>19%</td>
<td>7%</td>
</tr>
<tr>
<td>Packaging, assembly &amp; test</td>
<td>5%</td>
<td>39%</td>
<td>9%</td>
<td>6%</td>
<td>19%</td>
<td>19%</td>
<td>19%</td>
</tr>
<tr>
<td>Overall</td>
<td>35%</td>
<td>10%</td>
<td>11%</td>
<td>16%</td>
<td>13%</td>
<td>10%</td>
<td>5%</td>
</tr>
</tbody>
</table>

Source: SIA, State of the Industry report, Nov’22
China & Taiwan Dominate the OSAT Landscape

Top 20 OSATs by 2021 Revenue ($M)

<table>
<thead>
<tr>
<th>HQ locale</th>
<th>#</th>
<th>$M*</th>
</tr>
</thead>
<tbody>
<tr>
<td>China</td>
<td>5</td>
<td>1510</td>
</tr>
<tr>
<td>Taiwan</td>
<td>3</td>
<td>923</td>
</tr>
<tr>
<td>Malaysia</td>
<td>2</td>
<td>711</td>
</tr>
<tr>
<td>Japan</td>
<td>1</td>
<td>378</td>
</tr>
<tr>
<td>Korea</td>
<td>1</td>
<td>348</td>
</tr>
</tbody>
</table>

North America:
- AMKOR in US-HQ’d but has no production facilities in NA
- Integra is largest US OSAT (KS, CA)
- IBM Bromont is largest OSAT in NA (US DoD Trusted facility)

Source: Yole
6 Companies Package 80% of wafers using Advanced Packaging

Top Providers of Advanced Packaging*

<table>
<thead>
<tr>
<th>Company</th>
<th>HQ</th>
<th>Advanced Packaging Main Factory Location(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASE Group</td>
<td></td>
<td><img src="image" alt="ASE Group Flags" /></td>
</tr>
<tr>
<td>AMKOR</td>
<td></td>
<td><img src="image" alt="AMKOR Flags" /></td>
</tr>
<tr>
<td>TSMC</td>
<td></td>
<td><img src="image" alt="TSMC Flags" /></td>
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<tr>
<td>JCET Group</td>
<td></td>
<td><img src="image" alt="JCET Group Flags" /></td>
</tr>
<tr>
<td>Samsung</td>
<td></td>
<td><img src="image" alt="Samsung Flags" /></td>
</tr>
<tr>
<td>Intel</td>
<td></td>
<td><img src="image" alt="Intel Flags" /></td>
</tr>
</tbody>
</table>

Source: Yole

Advanced Packaging includes: all flip chip, all wafer level packaging technologies, and all 2.x and 3D technologies.
>50% of the World’s Packaging Facilities are in China + Taiwan
Implied Capacity is even higher

Global Packaging Facilities:
- 373 OSAT (77%)
- 111 IDM (23%)

The majority are focused on legacy packaging technology (e.g. >100 facilities offering QFN)

Facilities here are much smaller than those in Asia on average so overall total capacity in Americas is ~3%.

Source: SEMI, OSAT Database
OSAT Manufacturing in US has two Major Barriers to Entry

Financial sustainability is a problem even if you have the initial CAPEX to launch.

Estimated 2021 CapEx spend for Packaging Activity

<table>
<thead>
<tr>
<th>Company</th>
<th>CapEx Spend</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>3500</td>
</tr>
<tr>
<td>TSMC</td>
<td>3049</td>
</tr>
<tr>
<td>ASE Group</td>
<td>2000</td>
</tr>
<tr>
<td>Samsung</td>
<td>1500</td>
</tr>
<tr>
<td>AMKOR</td>
<td>780</td>
</tr>
<tr>
<td>JCET Group</td>
<td>593</td>
</tr>
<tr>
<td>Tongfu</td>
<td>487</td>
</tr>
</tbody>
</table>

EBITDA = $1,121M
Net Income =$646M

5 Year GM% for Top 3 OSATs

<table>
<thead>
<tr>
<th>OSAT</th>
<th>High</th>
<th>Low</th>
<th>Ave</th>
</tr>
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<tbody>
<tr>
<td>ASE Group</td>
<td>21.4%</td>
<td>21.0%</td>
<td>21.2%</td>
</tr>
<tr>
<td>AMKOR</td>
<td>17.5%</td>
<td>17.7%</td>
<td>17.6%</td>
</tr>
<tr>
<td>JCET Group</td>
<td>12.8%</td>
<td>13.5%</td>
<td>13.2%</td>
</tr>
</tbody>
</table>

Sources:
1. Yole
2. AMKOR FY2021 Earnings Call

... and this with all major manufacturing operations being in Asia.
CHIPS Act Overview

Background

- Called for by DPAA of 2021
- Approved by Congress and signed into law in August 2022 with $52.7B of funding over 5 years as part of the larger CHIPS and Science Act ($280B total)
- Section 9906 b calls for creation of an Industrial Advisory Committee (IAC)
- Section 9908 calls for the President to investigate applications of the Defense Production Act (DPA) of 1950 to enhance US capabilities in these areas within 180 days of the CHIPS Act enactment

### Table

<table>
<thead>
<tr>
<th>Section</th>
<th>Subject Matter</th>
<th>FY2023</th>
<th>FY2024</th>
<th>FY2025</th>
<th>FY2026</th>
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<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>39</td>
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<tr>
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<td>9905</td>
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<td>0.1</td>
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<td>0.5</td>
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<tr>
<td>9906 c</td>
<td>NSTC</td>
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<td></td>
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</tr>
<tr>
<td>9906 d</td>
<td>NAPAMP</td>
<td>2.5</td>
<td></td>
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<td>1.3</td>
<td>1.1</td>
<td>1.6</td>
<td>11</td>
</tr>
<tr>
<td>9906 f</td>
<td>Manufacturing USA Institutes</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Workforce and Education Fund*</td>
<td>0.025</td>
<td>0.025</td>
<td>0.05</td>
<td>0.05</td>
<td>0.05</td>
<td>0.2</td>
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</tbody>
</table>

*to be administered through NSF

All amounts in US$B

Two Government Agency Views of Program Positioning

Dept of Commerce View

DARPA View

Reasonably consistent views...

Source: DoC/NIST White Paper on NSTC
CHIPS R&D Office

- Led by R&D Director, reporting to the Under Secretary of Commerce for Standards and Technology
- Will manage the development of NSTC, NAPMP, Manufacturing USA Institutes, and CHIPS Metrology Program [all of 9906]
- “Separate from but coordinated with CHIPS Incentive Program” [9902]

Source: “CHIPS for AMERICA: A Vision and Strategy for the National Semiconductor Technology Center, CHIPS R&D Office, April 25, 2023"
The NAPMP will utilize the NSTC to support (a) packaging facility(ies) that enables R&D efforts.

- **Prototype and pilot scale integration** of components fabricated in NSTC facilities or 3rd party sources.
- Baseline packaging flows to support a goal of **established package proven IP**.

The facility should have **sufficient tool redundancy** to allow **groundbreaking research** on new materials and processes while still **maintaining baseline capacity**.

- **Partnerships with domestic OSATs** and electronics manufacturing services (EMS) to facilitate migration of successful prototypes to a production manufacturing environment.

“Chiplets:” Developments on chiplets cut across many core NSTC and NAPMP activities: standards, roadmaps, technical centers, and the multi-project wafer program. The Department expects the NSTC to work with the NAPMP to create a chiplet program that plays a leading role in driving standards in 2D and 2.5D heterogenous integration, as well as establishing a long-term vision in 3D integration of memory and logic beyond existing standards in stacked memory. NSTC-sponsored multi-project wafer programs could be used to grow an expansive library of interoperable chiplets that can be integrated with custom chiplets to demonstrate innovations with reduced investment and time. The technical center for heterogenous integration described earlier, combined with an open chiplet platform, could play a central role in prototyping new and emerging complex systems for transition into commercial production. Private sector companies could be created or expanded to participate in a chiplet ecosystem. In brief, the NSTC, in coordination with the NAPMP, should establish a robust chiplet program to enable an open chiplet marketplace and maintain U.S. leadership in a broad spectrum of silicon and non-silicon technologies.”

Source: “CHIPS for AMERICA: A Vision and Strategy for the National Semiconductor Technology Center, CHIPS R&D Office, April 25, 2023"
# CHIP Act 9906 Gameplan by DoC Element

## Program Development Timeline

**SUMMER 2023**
- National Semiconductor Technology Center
  - IAC Meeting June 6th

**FALL 2023**
- Selection Committee identifies Board of Trustees
  - NAPMP vision and strategy paper

**WINTER 2023**
- Establish NSTC
  - RFI Summary Published
  - Select topic(s); begin proposal process
  - Metrology Gaps Report Published
  - Select programs to begin

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**NSTC Whitepaper April 25th**

**HINT:** Sign-up for updates at CHIPS.gov

Source: "CHIPS for America Research and Development Update," E. Lin, presented at the June 6, 2023 IAC Meeting
IAC Working Group Recommendations (June 6th, 2023)
Implications to both NSTC and NAPMP

Source: https://www.nist.gov/chips/industrial-advisory-committee/industrial-advisory-committee-meetings
Approach (90 days)

- Reviewed 16 relevant R&D, roadmap, and ecosystem landscape reports
- Rolled up “Top 5 Focus Areas” from each working group member
- Identified key R&D gaps categories to be addressed
- Recorded perspectives from 22 experts relevant to these categories
- Prepared 10 recommendations for June 6 IAC meeting

R&D Gaps Working Group

- Daniel Armbrust, Intel
- Rajarao Kompella, IBM
- Om Nalamasu, Applied Materials
- Todd Youngren, SRC
- Vitor Meireles, GlobalFoundries
- Andrew Fursen, Texas Instruments
- Ahmad Bahai, Texas Instruments
- Carol Handwerker, Purdue University
- James Ang, National Institute for Science and Technology
- Susie Armstrong, Qualcomm
- Debo Oloso-Olikana, Applied Materials
- H.S. Philip Wong, Stanford University
- Gregg Bartlett, GlobalFoundries
- Ken Joyce, Brewer Science
- Ann Kelleher, Intel Corporation
- Charles Gray, Ford Motor Company
- James Choi, GlobalFoundries

NAPMP Tech Centers Concept Recommendation

Core "Si-centric" applications
- HPC, AMS, RF
- EDA / System
- Design / Simulation
- Packaging
- MEMS / Bio Materials
- Interposer
- Tools
- 3D Materials
- Adv ABS Substrates
- Glass Substrates
- Panel Integration
- Substrate Materials
- SiPho
- Photonic Design / EDA
- EIC/PIC Integration
- Fiber Attach
- Photonic Materials

Cross-cut coordination
- MEMS / Photonics
- EDA / Semiverse
- Interface standards
- Materials
- Reliability / testing
- WFD

IAC R&D Working Group recommends 4-5 NAPMP “Tech Centers”

Source: "IAC R&D Gaps Working Group," presented at the June 6, 2023 IAC Meeting
IAC R&D Gaps Working Group Recommendations

1) Ensure an independent budget and a dedicated executive leader for NAPMP, reporting to NSTC CEO and NSTC fiduciary board

2) Incentivize (9902) an existing wafer- and panel-based manufacturer to create prototyping capabilities in the US by establishing a pilot and initial manufacturing line, including expansion capabilities (annex) for R&D

3) Incentivize (9902) at least one existing substrate manufacturer to create a US pilot and initial manufacturing line and with a R&D annex to explore advance substrate options (including glass)

4) Ensure a robust set of programs that establish and extend enabling processes and capabilities such as bump and line pitches sub-5 μm line/space, processing for TSVs (silicon and substrate), hybrid bonding (Wf-Wf, Die-Wf, Die-Die), etc. across multiple technologies and materials (i.e., not just silicon)

5) Identify EDA advanced packaging and system gaps and create pathfinding and ultimately EDA tools that can effectively co-design and system optimize all elements of 2.5 and 3D heterogeneous integration (especially photonics, memory, RF, power, etc.) including multi-physics capabilities

6) Create a community of stakeholders to build a digital twin capability from the R&D stage through manufacturing with a tight integration to EDA/simulation as well as for workforce development support and training

7) Set grand challenges of achieving 10x increase in productivity and 10x decrease in environmental/energy footprint for mainstream advanced packaging capabilities, including eco-benign semiconductor manufacturing

8) Double the U.S. advanced packaging university footprint (from ~5 to ~10) and faculty, expand existing advanced packaging university programs by at least 50%, and build a virtual university-wide curriculum with increased funding for research and education

9) If the IAC were to call out one emerging technology to receive special attention, we believe silicon photonics is a rare general-purpose technology that should merit CHIPS Act investments in R&D, prototyping, and manufacturing

10) Complete a landscape survey and gap analysis of the advanced packaging of both supply and demand in the US (and North America) leveraging recent reports including prototyping gaps in key specialty packaging capabilities - including MEMS, photonics, power electronics, analog, and RF.

Source: “IAC R&D Gaps Working Group,” presented at the June 6, 2023 IAC Meeting
Built a Diverse Coalition - 220+ member entities including industry companies, innovation start-ups, universities, U.S. National Labs, key industry groups, and non-profit/consortia.

Answered the NSTC/NAPMP RFI and the Manufacturing USA RFI from the US Department of Commerce - Over 90 members of the ASIC team collaborated to produce a 120-page NSTC/NAPMP response and over 25 members teamed to produce the Manufacturing USA response.


Social Media Channels - ASIC launched accounts on Twitter and LinkedIn.

Website Launch - [https://asicoalition.org/](https://asicoalition.org/)


Sample of Participants

- American Semiconductor Innovation Coalition (ASIC)
- IBM
- Intel
- Qualcomm
- NVIDIA
- Texas Instruments
- Analog Devices
- Intel Corporation
- Synopsys
- Cadence Design Systems
- Advantest
- Ambrute
- ASML
- Applied Materials
- Albany Nanotech Complex
- Argonne
- Ansys
- Anadigics
- Alliance of Automobile Manufacturers
- i3 Microsystems
- IBM
- microcontroller
- MIT
- Mythic
- Neologic
- NXP
- NEUreate
- NY Creates
- New York University
- MIT
- Rensselaer Polytechnic Institute
- Siemens
- Silviasoft
- Synopsys
- Thermo Fisher Scientific
- TEL
- ULVAC
- Western Digital
ASIC Advanced Packaging Team

Who are we?  138* members from across 79* entities

19 Universities  37 members
BU
Cornell
GaTech
MIT
Penn State
Princeton
Purdue
RPI
SUNY
U Binghamton
U Delaware
U Illinois
U Michigan
U Minnesota
U Puerto Rico
U Vermont
UCLA
UIUC
USC(ISI)

3 Analysts  3 members
TechCet
TechSearch
Yole Dev

3 National Labs  3 members
ANL
CEA-LETI
Fraunhofer

3 Industry Assoc  3 members
iNEMI
IPC
SEMI

2 Mlls  4 members
AIM Photonics
NextFlex

48 Companies  87 members
3D Glass
ADI
Advantest
AMAT
AMD
Analog Photonics
ASPDPL
AT&S
Atomica
Canon Nano
DECA
Dupont
FormFactor
GE Research
Global Foundries
Green Source
Hyperion
i3 Micro
IBM
Integra
Jabil
Resonac
JSR Micro
Keysight
KLA
LAM
Marvell
Mercury
Mosaic
NANTERO
tenes
NGC
Nhanced
WDC
Novami
NXP
Siemens
Skywater
Sunny
TEL
Teledyne
TI
TTM
UI Corp
ULVAC
Veeco
WDC

*from Feb’23 – more now
ASIC Interpretation of NAPMP Objectives

- Encourage and support advanced research to create totally new technologies, designs and products.
- Accelerate technology development
- Transfer new technology to US commercial production
- Support workforce development
- Maintain close links with the NSTC
As a “Manufacturing Program”, we assume the NAPMP COEs will be program focused and will not typically have their own facilities.

Major tasks would be:

- Research interface
- Road mapping
- Program selection, funding, objectives, monitoring to accelerate technology development
- Transfer of technology to pilot lines

- Each COE has a specific technology theme
- COE should have industry/university inputs, along with NIST inputs, into decision making
NAPMP Coalitions of Excellence (COEs)

The COEs would focus on accelerating technology development in the NAPMP, each with a particular technology theme. Ten proposed:

- 3D heterogeneous integration
- Copackaged optics (CPO)
- Advanced SIP
- High voltage/high power
- FO-WLP (reconstituted)
- Interposers/Bridges
- Substrates
- MEMS
- Flexible Hybrid & Additive
- Cross cutting (eg thermal, reliability, DFM, etc)

Each COE would have sub-COEs to drive subsets of the technology.

Example: 3D HI

- Co-design EDA for design and test
- Hybrid bonding  
  [example Projects]
  - Bonding down to 2um bond pitch plus improved wafer finishing
  - Alignment to 100nm
  - Higher throughput tools with die speed binning capability
  - New materials to reduce anneal temperature
  - Data management for increased yield and traceability
- Thermal dissipation
- Below surface metrology
- Reliability
ASIC Proposed COE/Pilot Line Approach

Research hub and spokes

NAPMP Activities

- Wafer level centroid
  - Wafer Level COEs ➔ Wafer Level Pilot Line(s)

- Unit based centroid
  - Unit Process Level COEs ➔ A&T Pilot Line ➔ Domestic US Manufacturing Facilities / Partners
  - Unit Process Level COEs ➔ SIP Pilot Line

- Panel based centroid
  - Substrates COE ➔ Panel Level Pilot Line(s)

- Flex/additive centroid
  - Flex/Additive COE ➔ Flex/Addit Pilot Line(s)

Manufacturing
The NAPMP needs to monitor a broad set of success metrics, both leading and trailing, covering four areas:

- Operations
- Technical
- Economic
- Workforce Development

## ASIC Proposed NAPMP Success Metrics

<table>
<thead>
<tr>
<th>Area</th>
<th>ASIC Proposed NAPMP Metrics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operations</td>
<td>• # of NAPMP projects taken to production in USA&lt;br&gt;• # of members and dues paid&lt;br&gt;• # of projects delivered on schedule&lt;br&gt;• # of projects transfer to manufacturing</td>
</tr>
<tr>
<td>Technical</td>
<td>• Roadmap acceleration versus prior expectations&lt;br&gt;• US technical leadership&lt;br&gt;• # of technologies/processes/products transferred to manufacturing&lt;br&gt;• Reduced environmental footprint for packaging technologies</td>
</tr>
<tr>
<td>Economic</td>
<td>• US production market share in semi packaging (advanced and mature)&lt;br&gt;• # of new jobs created in US packaging facilities&lt;br&gt;• Growth of new industries supported by the NAPMP (eg EV, medical etc)&lt;br&gt;• Growth of US based packaging foundry</td>
</tr>
<tr>
<td>Workforce</td>
<td>• # of students in training versus goals (AA, BS, MS, PhD)&lt;br&gt;• % minority and retrained students (eg military)&lt;br&gt;• # of students hired by semiconductor packaging industry&lt;br&gt;• # of semi packaging centric locations, courses and programs&lt;br&gt;• Geographic diversity of training</td>
</tr>
</tbody>
</table>
Summary

- The ASIC NAPMP team has developed an organization and structure for the NAPMP built around:
  - Ten Coalitions of Excellence for accelerated technology development
  - Five Pilot Lines for economic and sustainable manufacturing hardening
  - University Focus Centers leading the university research efforts

- The NAPMP objectives are:
  - Support research activities in advanced packaging
  - Accelerate technology development
  - Develop and harden economically and sustainable manufacturable processes
  - Transfer technology for manufacture to support multiple new market opportunities

- The NAPMP will collaborate with multiple organizations including the NSTC, companies, universities and other government programs (eg NGMM, ME Commons)

See White Paper for details
To Learn more about ASIC

→ **Website:** [https://asicoalition.org/about](https://asicoalition.org/about)

→ **Twitter:** [https://twitter.com/asicoalition](https://twitter.com/asicoalition)

→ **Linkedin:** [https://www.linkedin.com/company/american-semiconductor-innovation-coalition/](https://www.linkedin.com/company/american-semiconductor-innovation-coalition/)