Joint User Group Meeting

Waferbonding and CMP – A Perfect Couple!

Fraunhofer ENAS & Center for Microtechnolgies @ Chemnitz University, Technology Campus 3, 09126 Chemnitz, Germany
Fraunhofer IZM-ASSID, Ringstrasse 12, 01468 Moritzburg, Germany
ErzM-Technologies UG, Technology Campus 1, 09126 Chemnitz, Germany

Dr. Knut Gottfried

Content

- Wafer bonding technologies
- What CMP can do
- Metrology

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Bonding in semiconductor fabrication

Bonding has different meanings in semiconductor manufacturing

Wire bonding

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Die (chip) bonding for single device packaging

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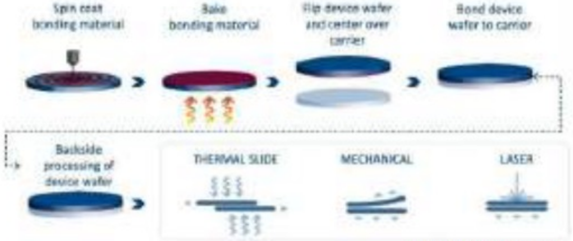
Temporary wafer to wafer bonding



© Brewer Science

Permanent wafer to wafer bonding

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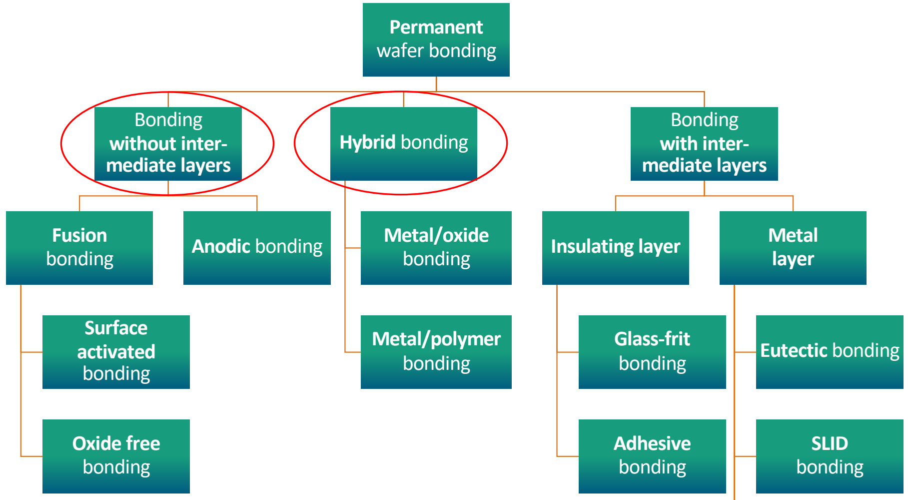
Wafer bonding technologies

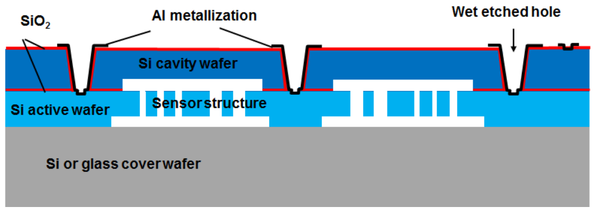
<u>Permanent</u> wafer bonding?

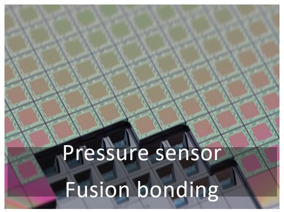
Wafer bonding techniques are used in microelectronics and MEMS / µ-systems to join wafers together on their entire surface – with or without additional intermediate layers.

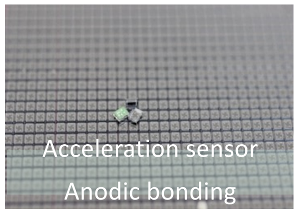


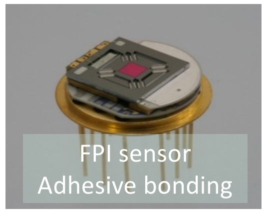
General requirements

- Material compatibility
- Mechanical stability
- Temperatures
- Hermetic sealing
- Bonding area
- Electrical contact









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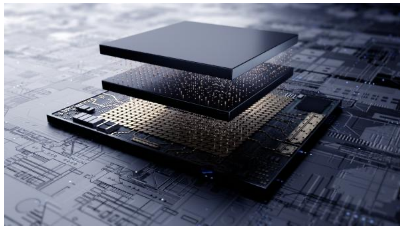
Wafer bonding – typical applications

Device Fabrication or Packaging???

Wafer Bonding technologies

3D-stacked devices

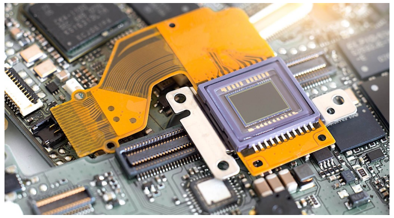
- **Hybrid** bonding



Source: Samsung 3D stacked memory at 7nm

CIS / µ-Displays

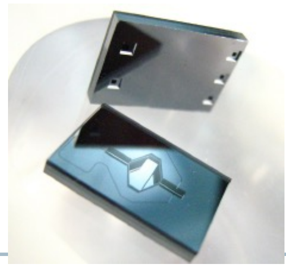
- **Fusion** bonding
- **Hybrid** bonding
- **Adhesive** bonding



Source: global tcad solution CMOS Image Sensors

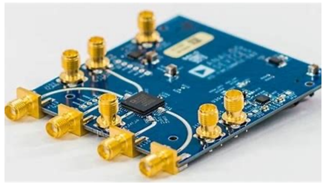
MEMS

- **Fusion** bonding
- **Anodic** bonding
- **Surface activated** bonding
- **Glass-frit** bonding
- **Eutectic** bonding
- **Adhesive** bonding
- **SLID** bonding
- **TC** bonding



RF Devices

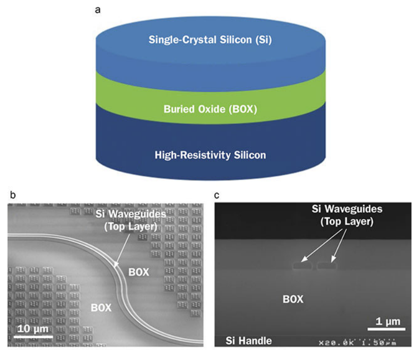
- **Fusion** bonding
- **Adhesive** bonding
- **Surface activated** bonding
- **SLID** bonding
- **Eutectic** bonding
- **Atomic Diffusion bonding**
- **TC** bonding



Source: Analog Devices RF Transceivers

SOI & SEMI finished bonded substrate

- **Fusion** bonding
- **Atomic Diffusion bonding**



Source: SOI Technology Lights Up the Next Wave of Photonics Solutions

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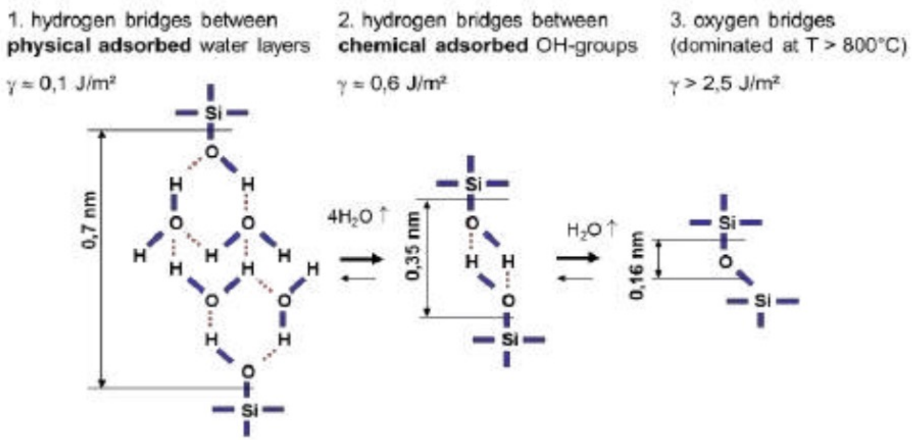
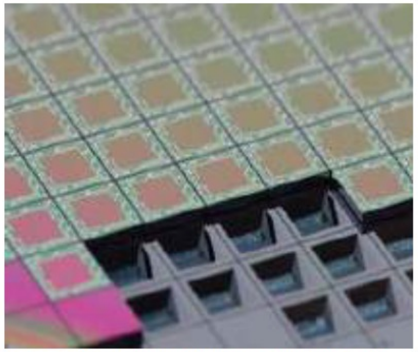
Direct bonding mechanism




Sensors fabricated from a 3-wafer stack

- Direct bonding between silicon wafers is based on hydroxyl groups (OH-groups)
- Can be initiated at room temperature just by close mechanical contact of the surfaces which should be bonded together (formation of hydrogen bridges based on van-der-Waals attractions)
- Conversion into covalent bonds at elevated temperatures (<u>typically 300°C or less</u>)
- In most cases PECVD-oxides or low temperature oxides are the bonding layers; thus, also other materials than silicon can be bonded
- Works also for patterned wafers, e.g., MEMS → bonding applies in frame areas only

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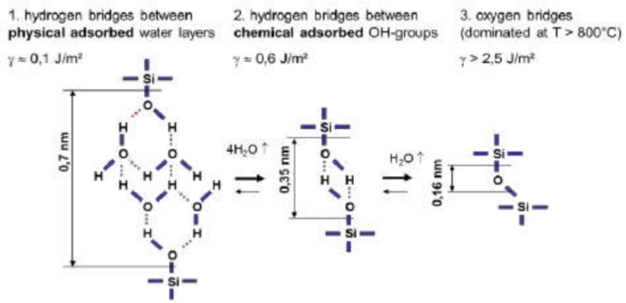
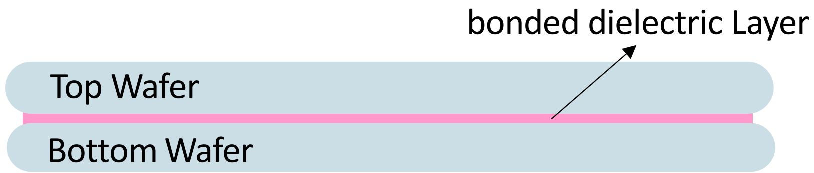
Direct bonding – what CMP can do?

- Surface geometry / surface properties of the wafers
  - Flatness, warp, bow
  - Roughness
- Rules of thumb
  - Flatness, warp, bow < 50µm
  - Roughness < 1nm … better < 0.5 nm
- What's the job of **CMP** here?
  - Adjust the desired roughness
  - Generate dangling bonds – touch polish / buffing!

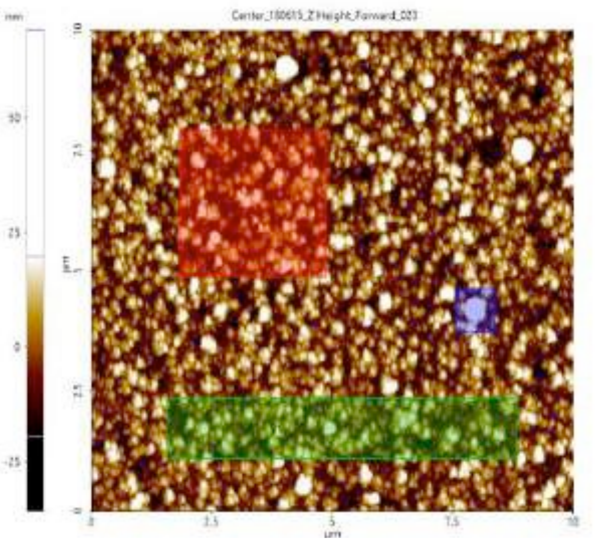




- Let's keep in mind:
  - The bond strength of direct bonds significantly increases with temperature! In contrast, we have clear temperature limits given by the devices and substrates.
  - We will never have perfect surfaces in a way that each atom of wafer 1 is bonded to a counterpart atom on wafer 2! But we need as much as possible bonding pairs! This is usually achieved by plasma activation right before bonding and can be supported / enhanced by CMP prior the plasma activation.

CVD-oxide direct bonding

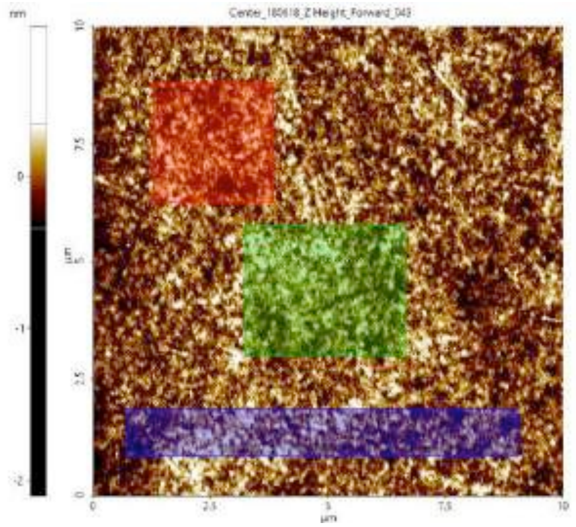
CVD-oxide layer - pre CMP



Statistics

Region	Min(nm)	Max(nm)	Mid(nm)	Mean(nm)	Rpv(nm)	Rq(nm)	Ra(nm)	Rz(nm)	Rsk	Rku
Red	-28.193	33.849	1.828	-1.786	64.042	8.830	7.878	62.766	-0.318	2.946
Green	-31.075	40.282	4.654	-0.265	71.450	8.320	7.262	68.225	-0.222	2.978
Blue	-24.423	67.882	21.734	8.846	92.314	11.802	15.838	85.517	-1.079	5.879

CVD-oxide layer - post CMP



Statistics

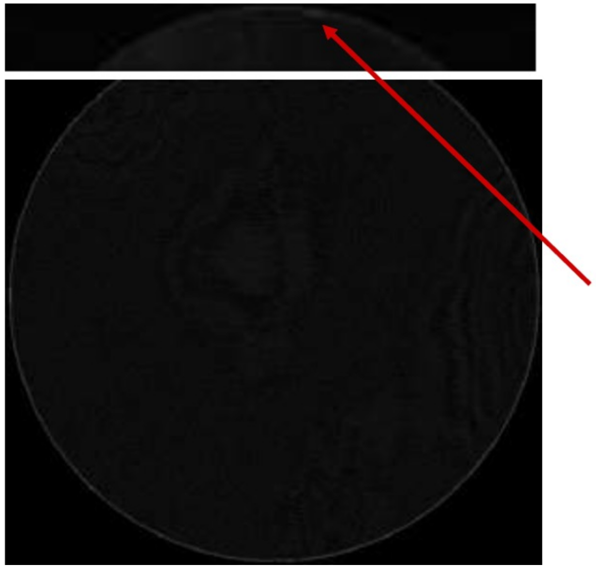
Region	Min(nm)	Max(nm)	Mid(nm)	Mean(nm)	Rpv(nm)	Rq(nm)	Ra(nm)	Rz(nm)	Rsk	Rku
Red	-0.654	0.592	-0.031	0.013	1.246	0.166	0.132	1.172	0.075	2.979
Green	-0.571	0.981	0.205	0.055	1.552	0.168	0.134	1.281	0.023	3.016
Blue	-0.717	0.733	0.008	0.014	1.450	0.170	0.136	1.252	0.074	2.911

Typical roughness improvement after a standard oxide CMP process

- Polisher: AMAT-Reflexion / AMAT-Mirra / AXUS-SURFACE / AXUS-IPEC / …
- Consumables: Klebosol 1508, IC1000 pad

CVD oxide direct bonding

- TEOS deposited at 125°C onto two 300mm Si-wafers
- TEOS surface polished
- Pre-bond cleaning in CMP tool
- Bonder: EVG Gemini
- Bond anneal at 200°C
- CSAM data:



small defect visible from bond energy test

✓ No other defects from particles or outgassing visible

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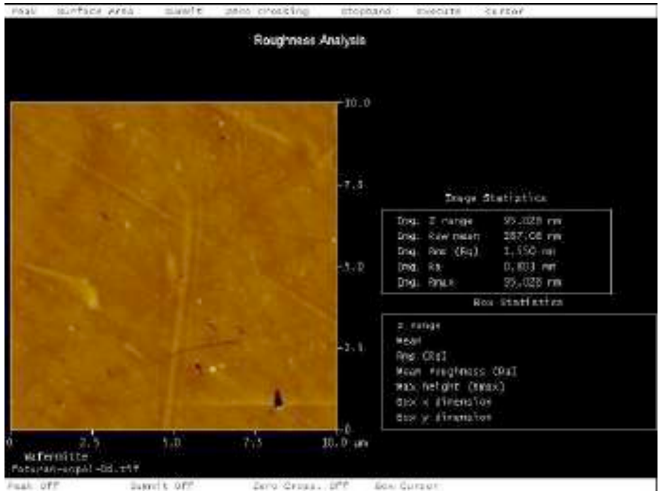
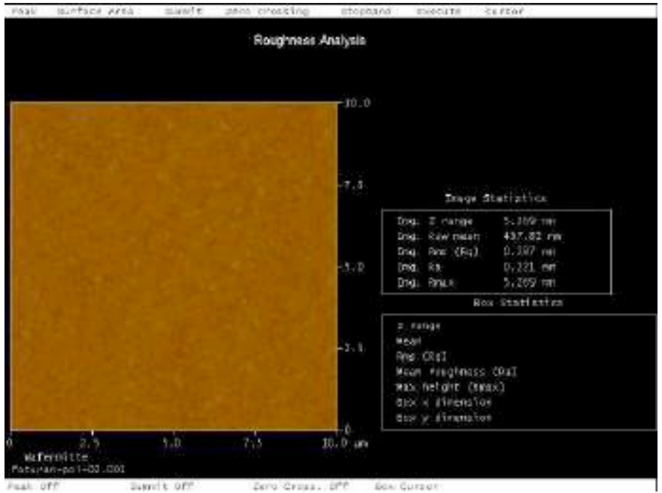
Glass direct bonding



Foturan glass – pre-CMP



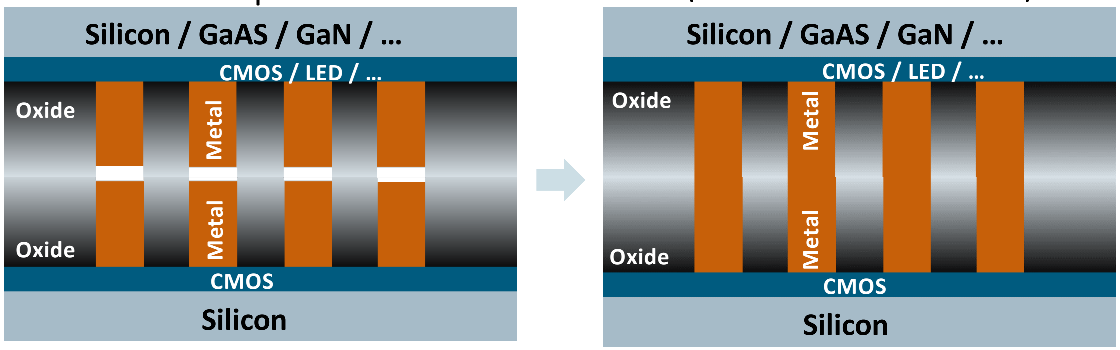
Foturan glass – post-CMP

	Platen 1	Platen 2
Polish pad	IC 1000	Politex
Slurry	Klebosol 1508	DI water
Down force	2 psi	1 psi
Polish time	up to 90 s	up to 60 s
Head/platen speed	64 rpm / 60 rpm	20 rpm / 20 rpm

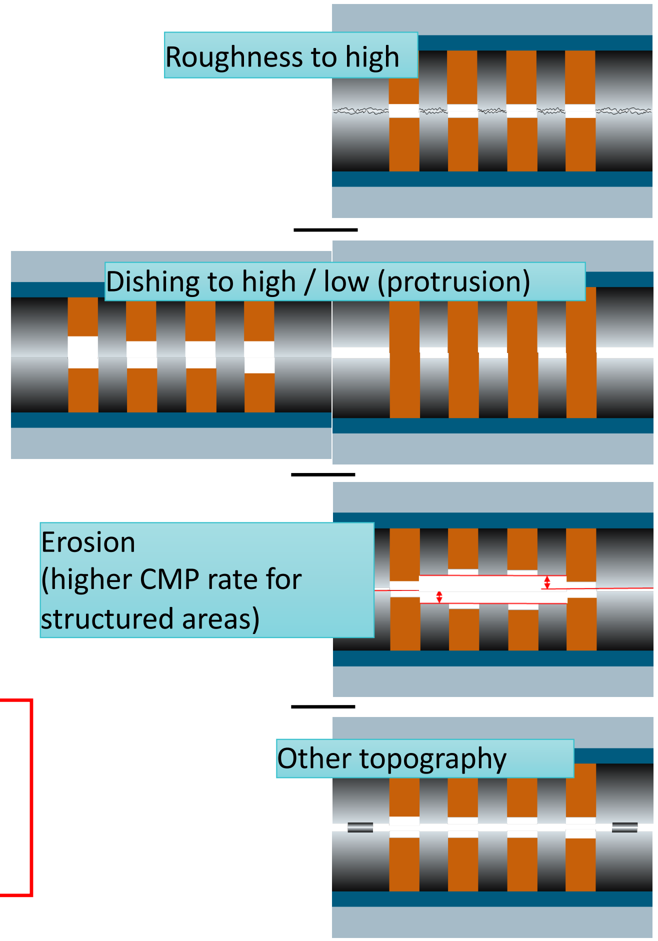
Hybrid Bonding

Oxide to Oxide bond at room temperature

Heat closes dishing gap (metal CTE > Oxide CTE)



Failure modes, which prevent bonding



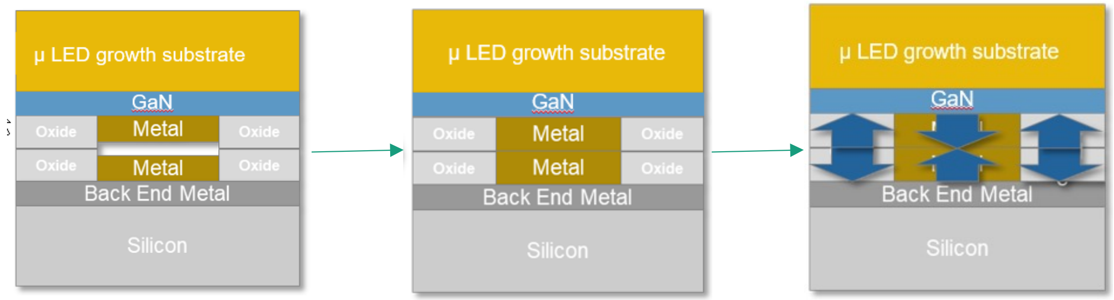
Critical parameters for bonding

- Roughness Oxide
- Dishing
- Erosion
- Topography (from underlying layers)

These parameters have to be measured during processing in an adequate way to increase homogeneity, quality, yield, ...

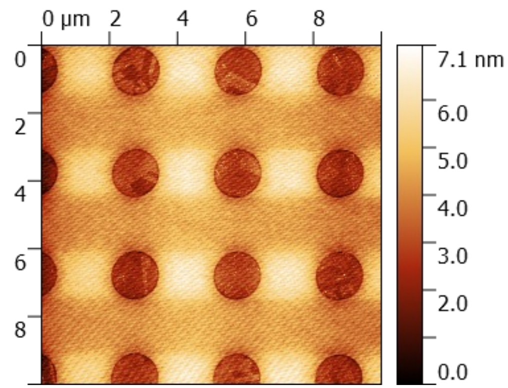
Hybrid bonding - process requirements

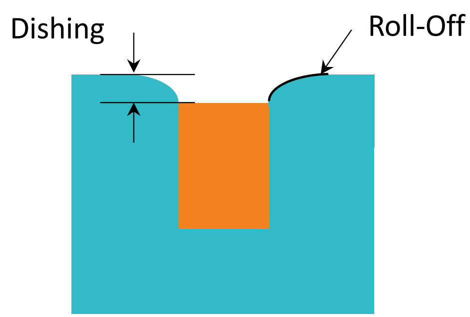
- Good uniformity: within die, within wafer, wtw
- Low remaining topography
- Low roughness



Specific to hybrid bonding applications

- Oxide roughness: same as direct bonding < 0.5 nm
- Oxide rounding: < 1 nm / µm
- Cu roughness in lower nm range
- Dishing: no rule of thumb, depends on via size and temperature budget (typ. 1 nm … 10 nm)
- Low remaining long-range topography (typ. less than 10 nm)
- Trenching: as low as possible (undesired effect)





Sketch of Dishing & Roll-Off of one via

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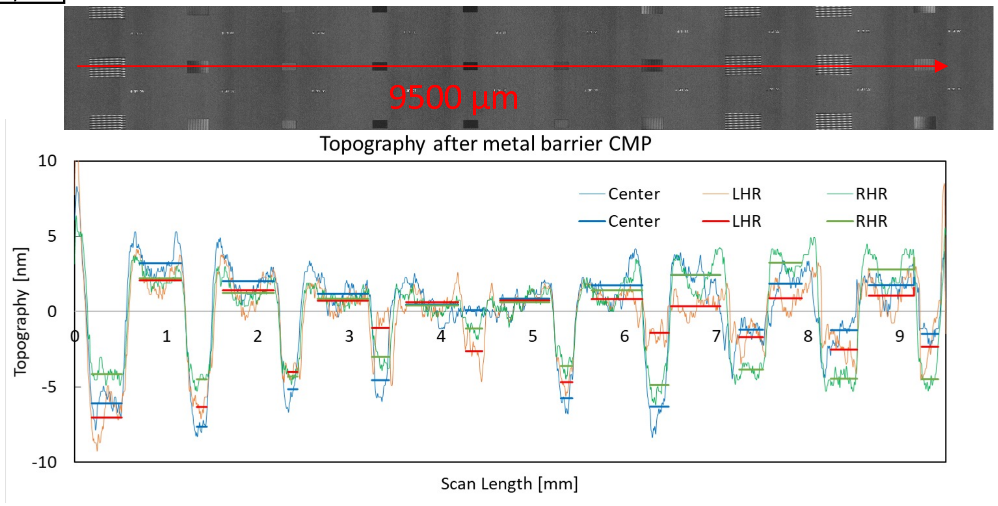
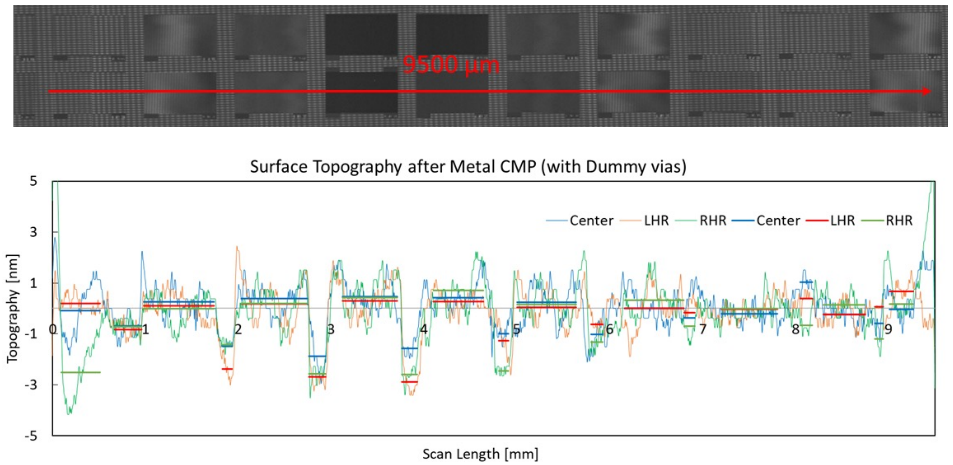
Hybrid bonding - Impact of Via Diameter & Density

Topography – Via Array and Without Dummy Vias

	15.90 % Cu				12.57 % Cu				15.90 % Cu	
Via Pitch (µm)	5	3	2	1	1	2	3	5	5	3



15.90 % Cu				12.57 % Cu				15.90 % Cu	
5	3	2	1	1	2	3	5	5	3



- Via pitch and density have an impact on the topography of the structures.
- The peaks slope are low and the overall topography is < 10nm for isolated via arrays.
- With the surrounding dummy vias, with a density of 16.62% the topography further decreases to < 5nm.

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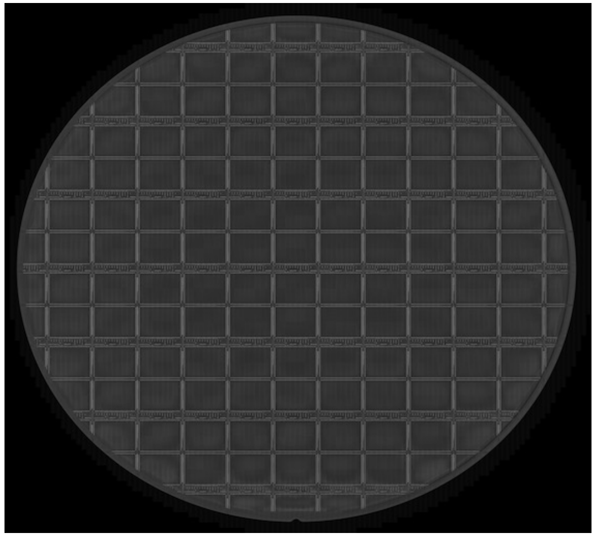
What’s the conclusion for CMP?

➢ **CMP will create bondable surfaces!**

- Perfect process control
  - Process parameters / process window
  - Endpoint
  - Consumables
- Process strategy
  - Over polish
  - Selective / non-selective
  - Dishing – protrusion – dishing

- **Fast and reliable inline metrology**

- Layout adaption / optimization
  - Design for functionality
  - Design for fabrication



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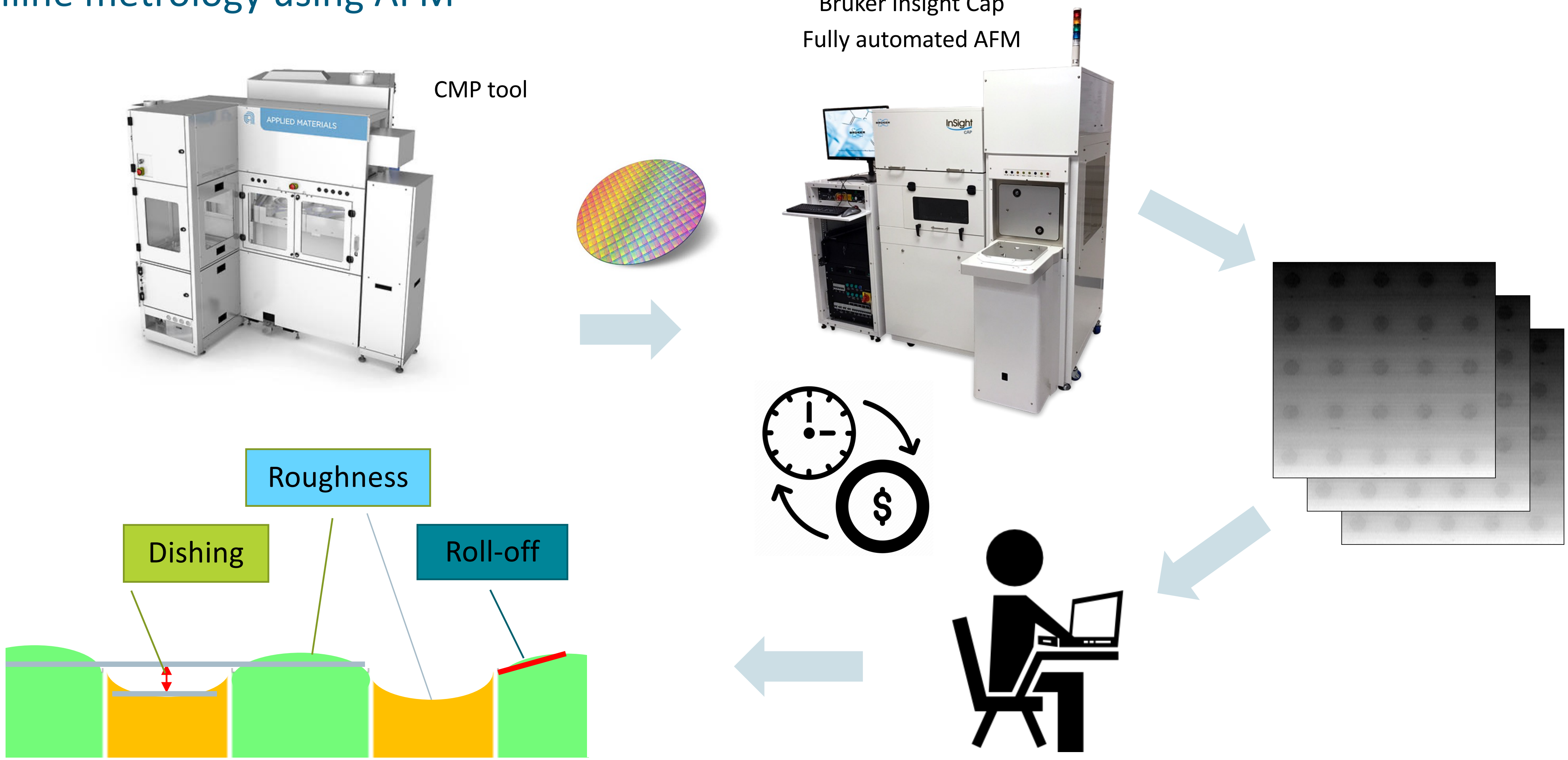
Inline metrology using AFM



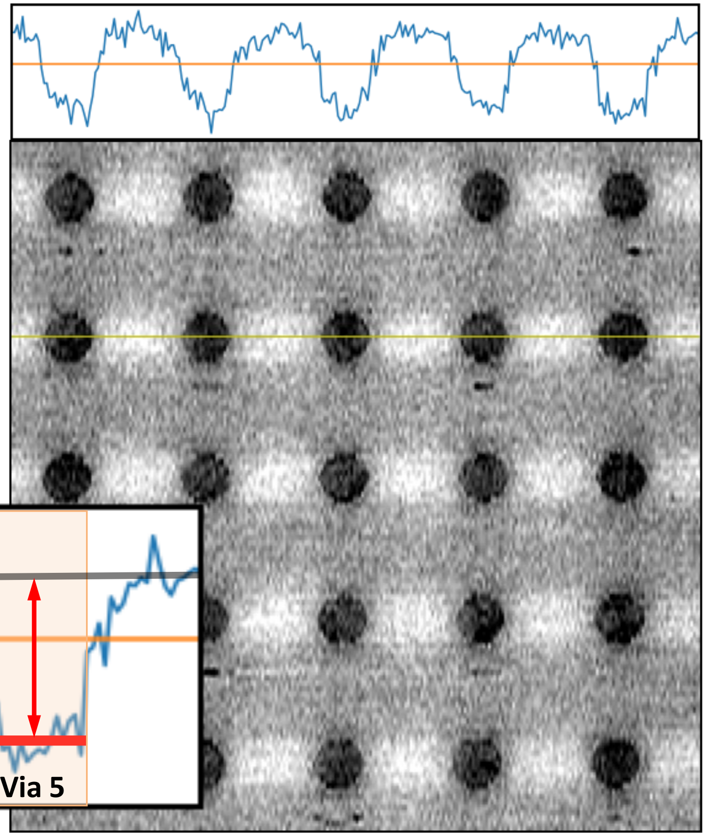
Manual Via Analysis

Using existing commercial software / free ware:

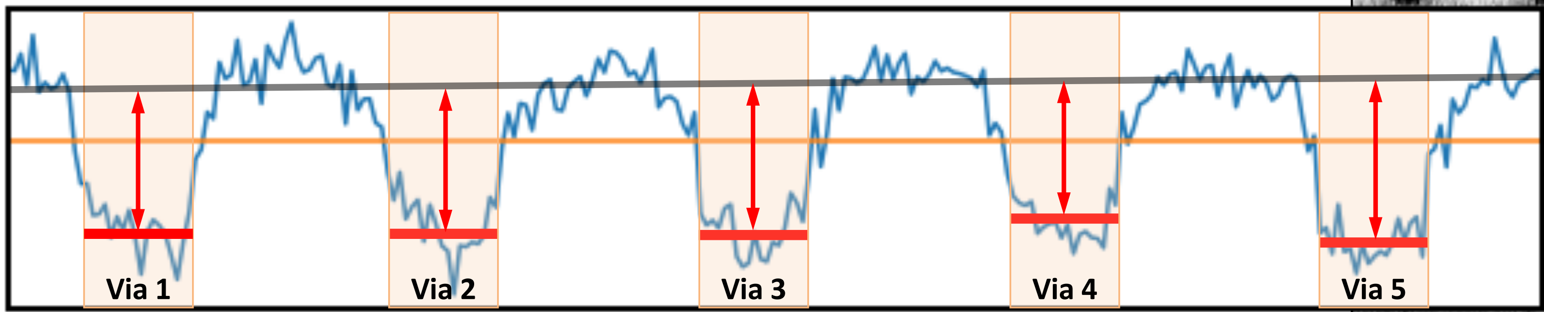
→ Manual placing of horizontal lines in the middle of each row

→ Manual placing of via boundaries in each line

→ Compute dishing in 1D line segment



Manually placed via boundaries



Very time consuming and fragile → Automatic analysis desirable

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Problem Statement

PROBLEM

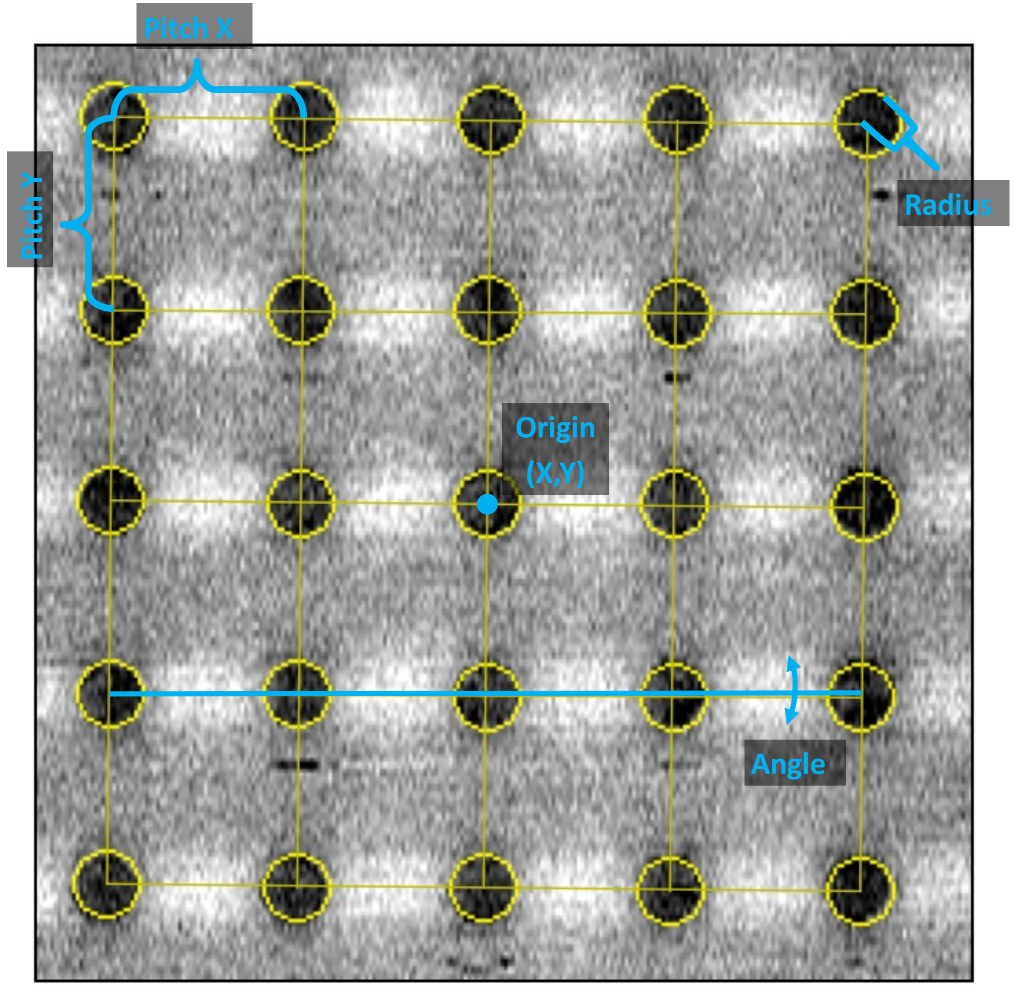
- Finding individual patterns for an automated analysis

SOLUTION

- Define a six-dimensional parameter space
- Efficient search for a parameterized grid of NxN circles

ENABLES

- Automatically compute dishing, roll-off, …, in 2D image instead 1D



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Sobel Edge Detection and Hough Transformation

Step 1: Standard Sobel edge detection filter

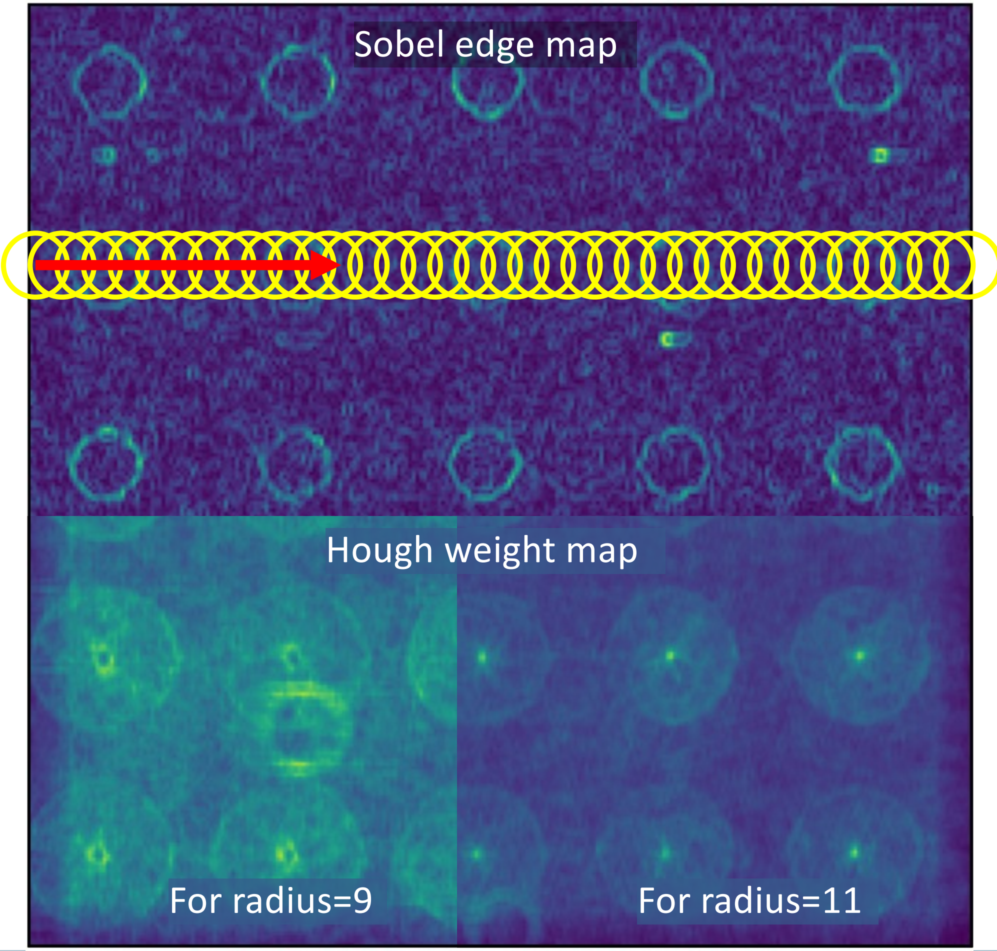
Step 2: Hough transformation

```
For every possible radius:
   For every possible center location:
      Accumulate all the pixels along the
      perimeter of the circle
```

Example runtime:

5 Radii, and image size 256x256 pixel

→ 1.49 s on a standard laptop (can be easily parallelized)



For more details see:

Zienert et al., Automatic Detection of Via Arrays in AFM Images for CMP Dishing Evaluation. Accepted for publication in IEEE Xplore.

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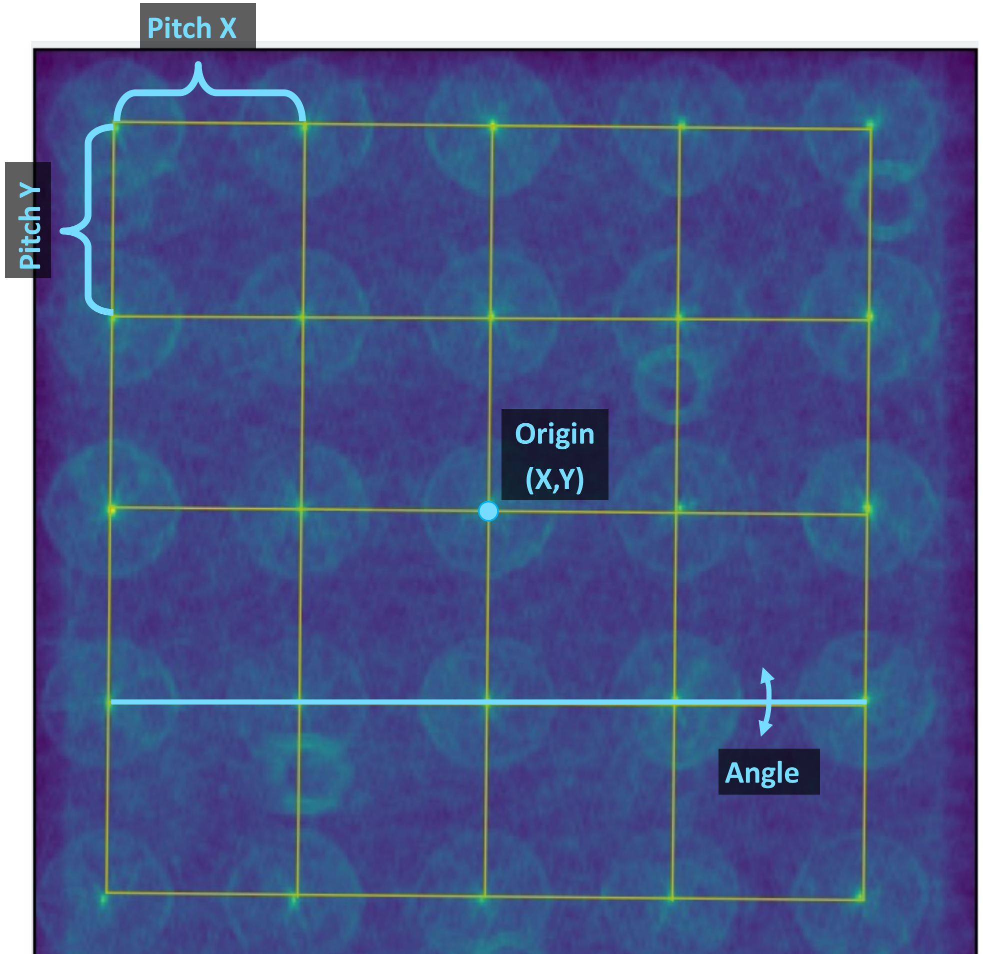
Brute Force Grid Search

Generate all possible grids and compute a weight indicating how well that grid fits

```
For every possible Radius:
   For every possible Pitch X:
      For every possible Pitch Y:
         For every possible grid location:
            For every possible Angle:
               Generate a NxN grid
               Accumulate all weights at
               the grid positions

Find best fitting grid parameters
```



Example:

- 21 pitch values, 5 angles, 5 radii and all origins
- 3,186,225 loop iterations
- 0.95 s on a normal laptop
- (can be easily parallelized)

Very efficient Python/NumPy implementation

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Topography analysis

Baseline:

Average height to determine zero level

Dishing:

Average height of all pixels inside a smaller circle

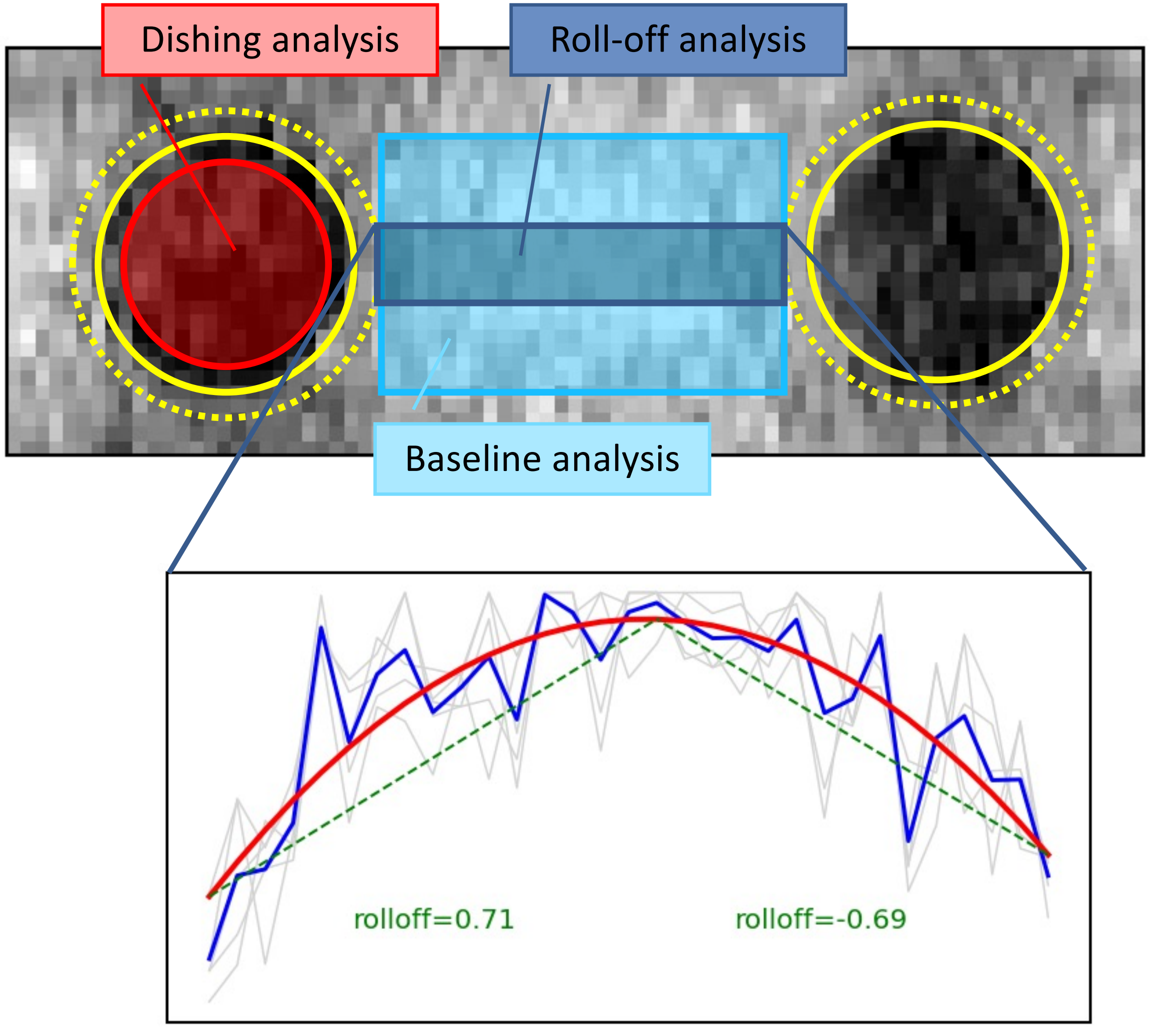
Standard deviation across all vias in the grid

Roll-off factor:

Vertically average all pixels inside rectangle

Fit 2nd order polynomial line

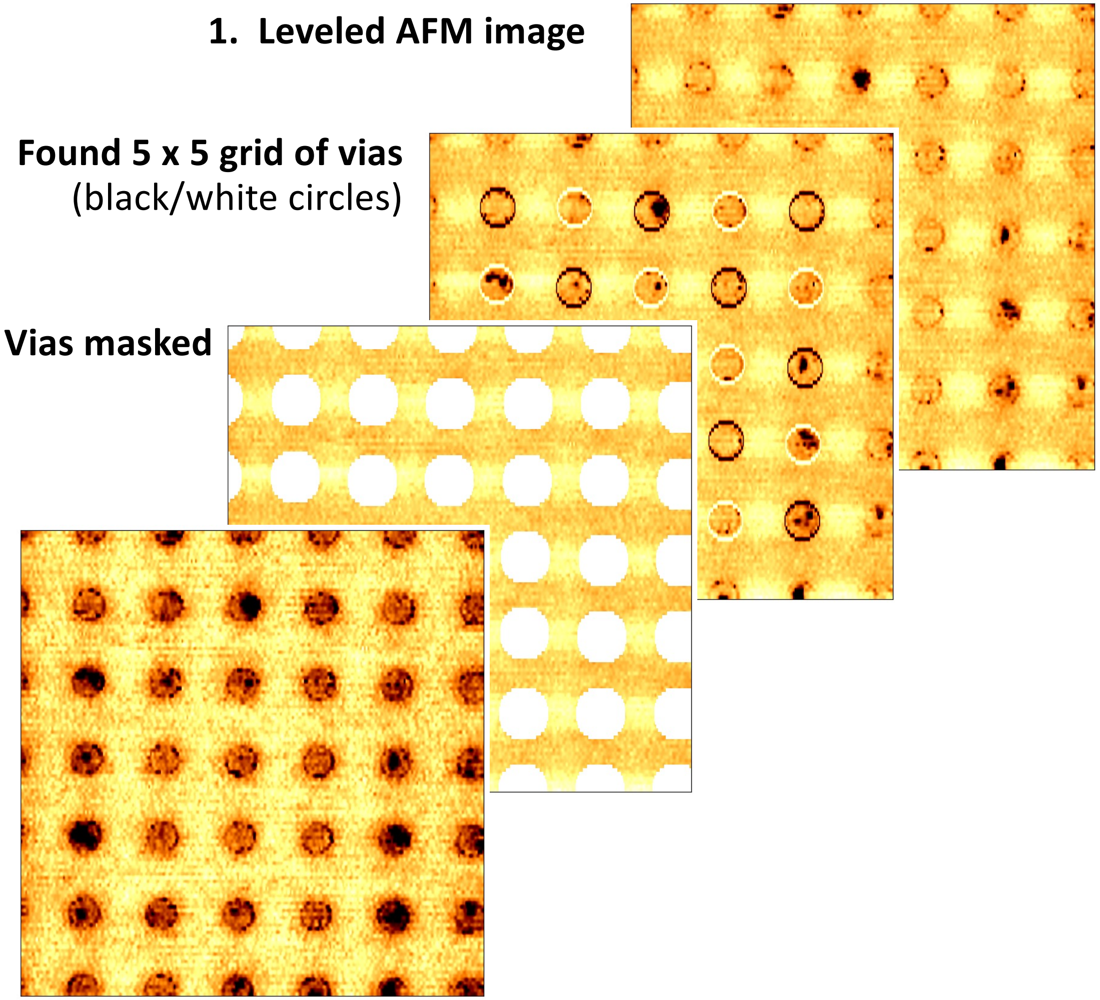
Determine slope from edge to maximum



Roughness analysis

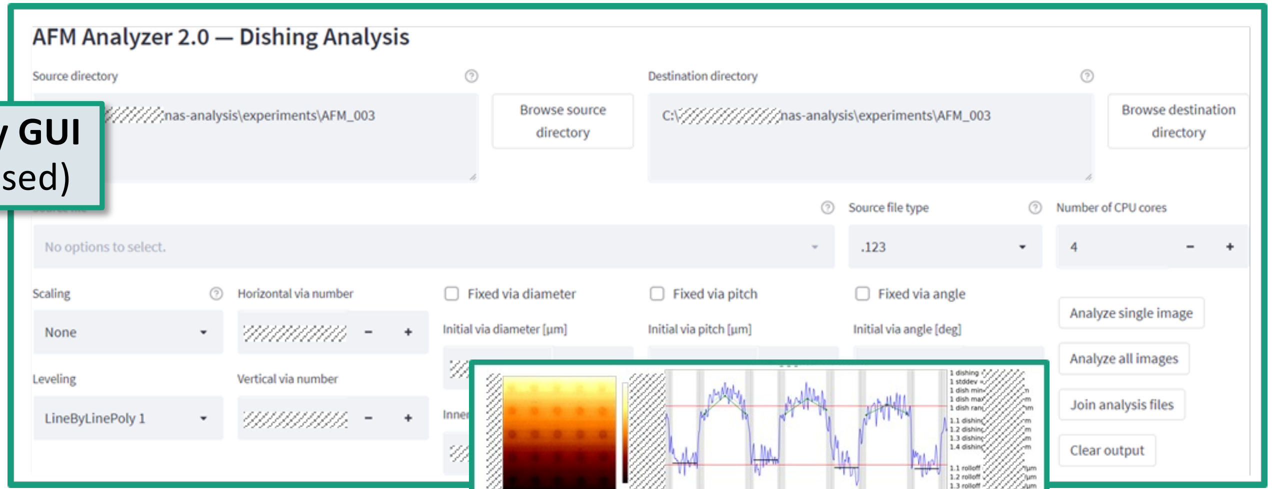
1. Leveled AFM image
2. Via search
3. Mask all vias
4. Level again without vias
   - Linear fits on area without vias
   - Applied to full image
   - Removes leveling artifacts (bright spots between vias)
5. Roughness analysis
   - E.g. arithmetic mean height $S_a = \frac{1}{A}\sum_{x,y}|z(x,y)|$
   - On area without vias
   - On areas inside vias (via bottoms)

→ Roughness values in agreement with commercial AFM software (manual analysis)



Current status

User friendly GUI (browser-based)

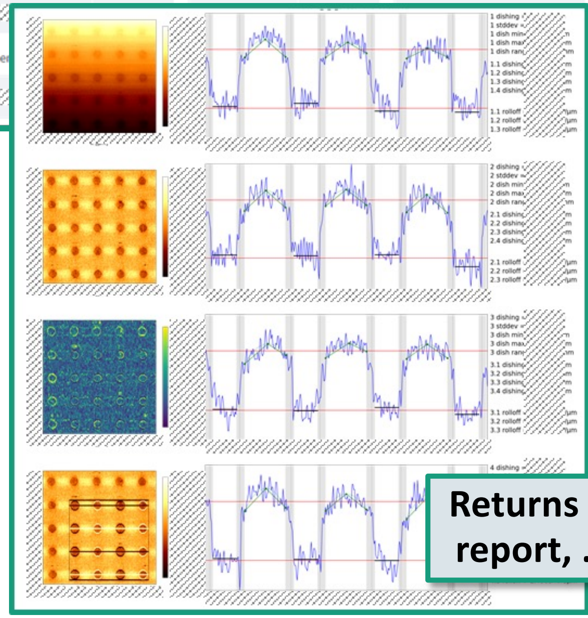


1. Implemented a fast algorithm to find regular grids of vias in AFM images (takes few tens of seconds per image, evaluates 20 images in parallel)

2. Replaced manual 1D dishing calculation by automatic 2D calculation reducing noise and increasing robustness and accuracy

3. Automatically generates reports (xlsx, csv, pdf, etc.)

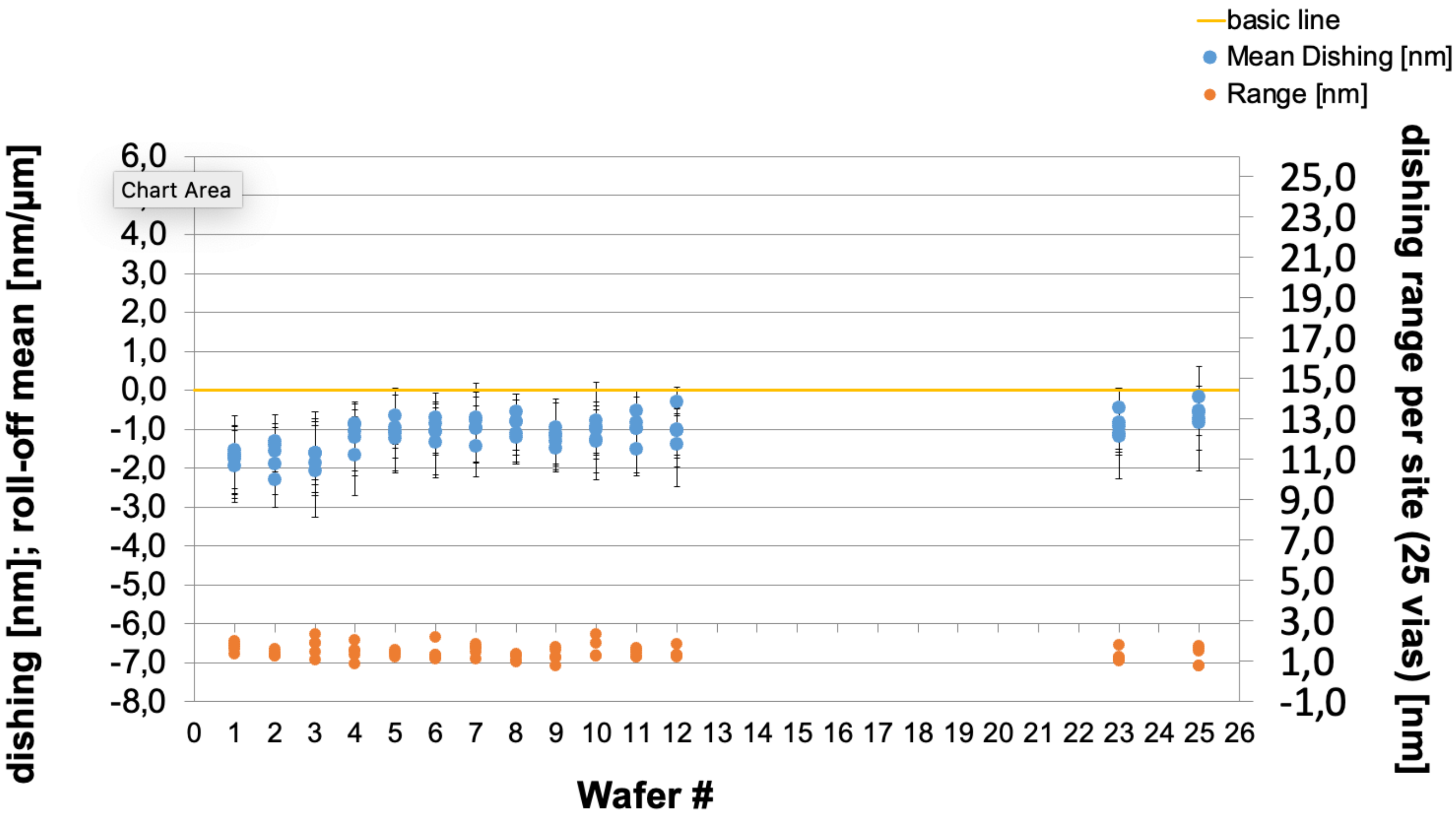
4. Created a browser-based graphical user interface to set parameters and automate the process



Returns graphical report, .csv, .xlsx

Reduced time for dishing analysis and report generation from hours to seconds

Example: dishing for µ-LED wafers with 1 µm via / 2 µm pitch



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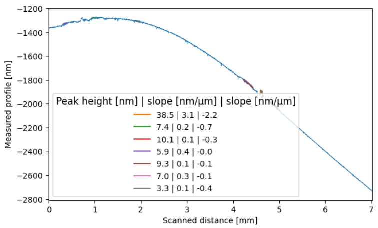
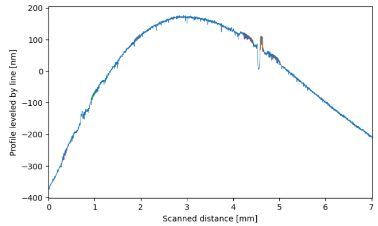
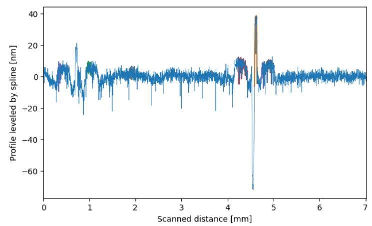
Long range topography inspection



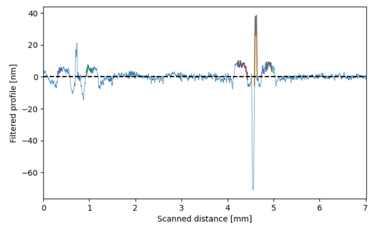
Raw data



Leveling



Smoothing



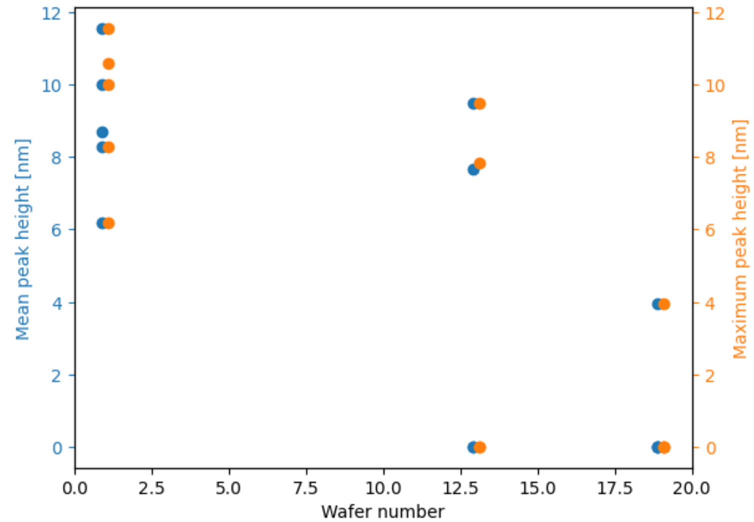
Result
→ evaluation of number of peaks, peak height, roll-off, …

Measurement parameter

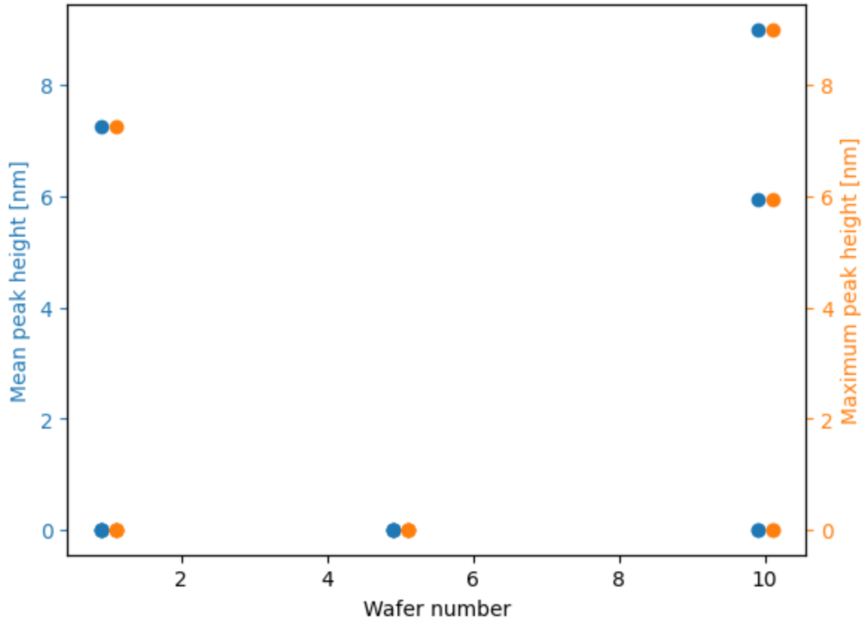
- 5 measurement points per wafer
- Scan length depending on layout (7 … 14 mm)

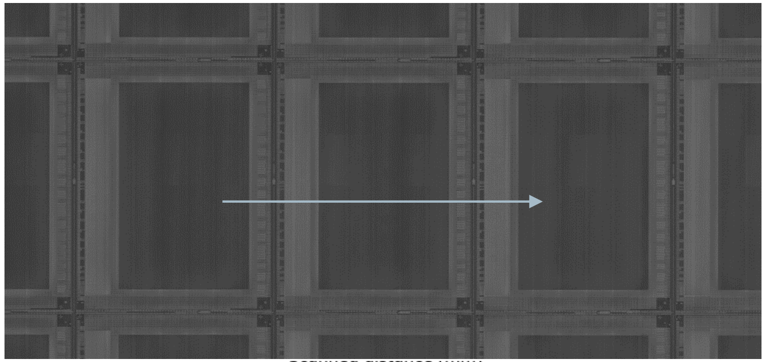
Explanation diagramm

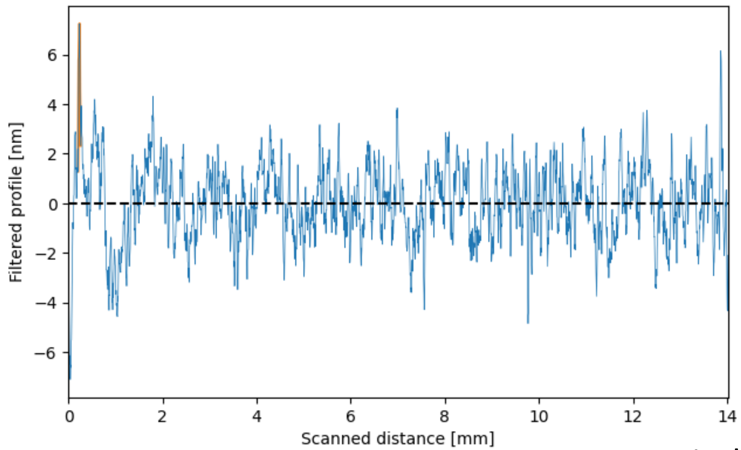
- Detected peaks per wafer
- plotting of
  - mean peak height and
  - maximum peak height per measurement point



Example: long range topography for µ-LED wafers with 1 µm via / 2 µm pitch



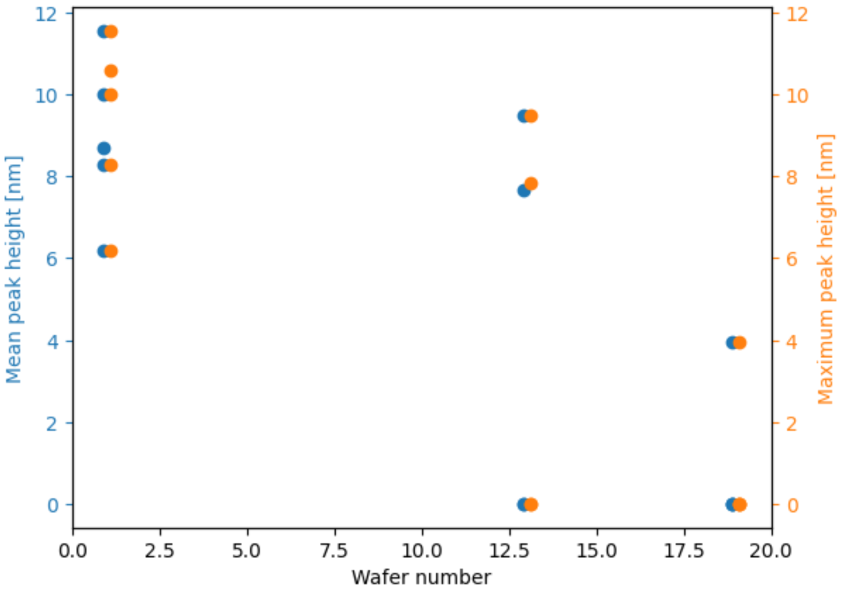


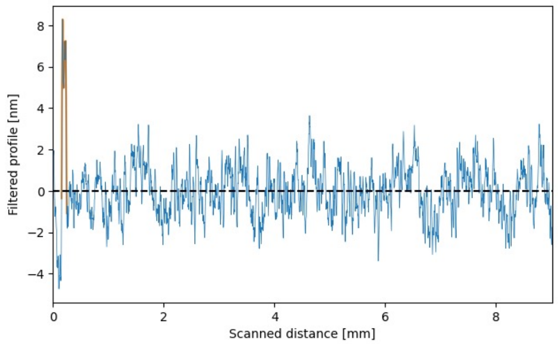


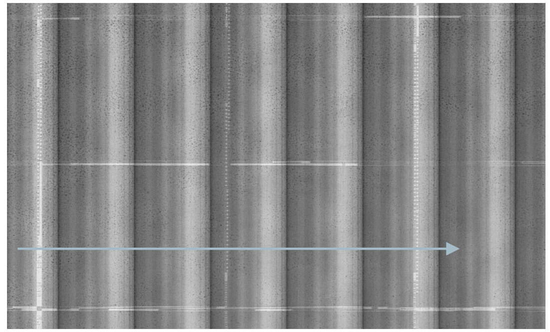
Typical profile

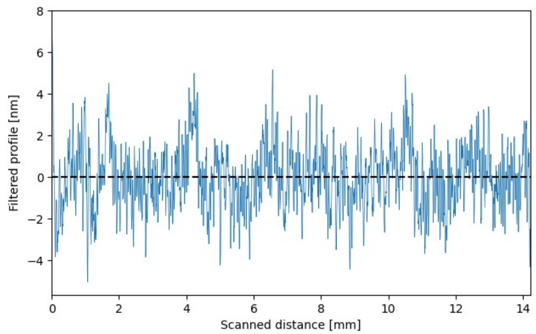
- No layout dependent topography
- Low number of peaks
- Peak height below 10 nm

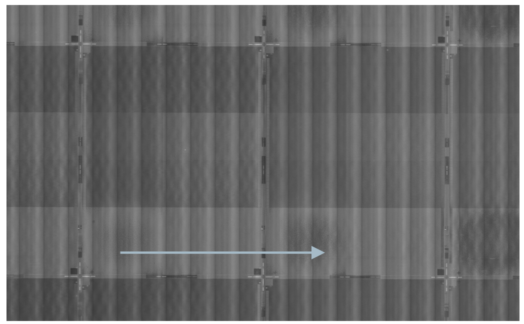
Example: long range topography for µ-LED wafers with 1 µm via / 2 µm pitch











- Max peak height 10 … 12 nm
- More peaks for layout RJ1
- Low amount of peaks

Summary / take-aways

- Wafer bonding is a high way to more than Moore
- CMP is THE enabling technology for a good number of bonding techniques
- ➢ Wafer bonding and CMP will come closer and closer
- It‘s all about CMP process control!
- It‘s all about CMP metrology!

Thank you for attention!

Dr. Knut Gottfried
+49 371 45001 299
+49 179 2042873
knut.gottfried@fraunhofer.de
knut.gottfried@erzm-tech.com