Investigation of W CMP Process for High Planarity

Seokjun Hong[1], Yanghee Lee[1], Jinwoo Bae[1], Byoungho Kwon[1], Jonghyuk Park[1], and Bo Un Yoon[1]

[1] Process Development Team, Semiconductor R&D Center, Samsung Electronics Co., South Korea

Chemical mechanical polishing (CMP) is an essential process to planarize inter-level dielectrics and isolate multiple layers in semi-conductor manufacturing [1]. In the CMP process, a slurry is used to polish a patterned wafer on a polishing pad to selectively remove materials from the wafer surface, as shown in Fig.1. As design rules become smaller due to the device miniaturization, the required level of planarity become more stringent. Thus, the control of wafer surface planarity is important to overcome device performances.

One of the major factors in deciding the amount of planarity is selectivity, which represents the ratio of material removal rates between the W and dielectric layer under the same process conditions. In other words, it is important to control the selectivity between W and oxide layer to achieve a high planarity in W CMP process. From the selectivity control, the local pressure can be uniformly distributed over the whole wafer surface.

In this study, the process conditions and consumables were optimized to control the material removal rates of each film (W, SiO2) on the patterned wafer. Consequently, the condition which the planarity was improved by 90% was found, as depicted in Fig.2. This research can be used to find the optimal condition for a high planarity in W CMP process.

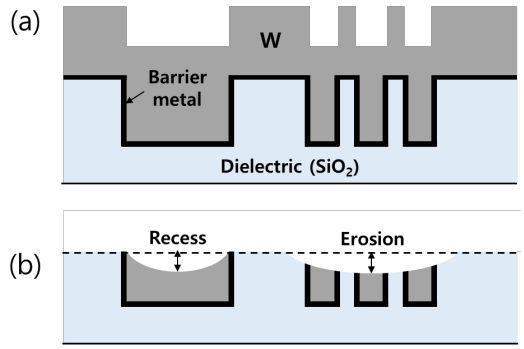

Figure 1. Schematics of W CMP process (a) before polishing and (b) after polishing

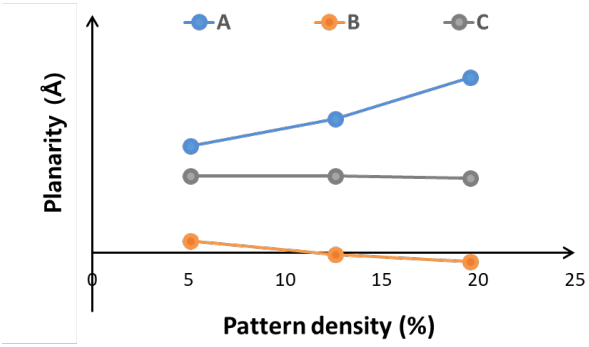

Figure 2. CMP planarity according to CMP conditions. (A, B, C)

Corresponding Author:
Seokjun Hong
Tel: +82 31-208-5467
E-mail: sj621.hong@samsung.com

Preference: ■ Oral ☐ Poster

Topic Area: CMP fundamentals, modeling, and simulation

References

[1] Babu, Suryadevara, ed. Advances in chemical mechanical planarization (CMP). Woodhead Publishing, 2016.