Chemical Mechanical Planarization (CMP) of thick Cu films for emissive arrays on GaN/InGaN micro-light emitting diodes

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We report the chemical mechanical planarization (CMP) process development and characterization for removing thick copper layer and barrier layer for emissive arrays based on blue or green GaN/InGaN micro light emitting diodes (µLEDs). An epitaxial GaN µLED array was fabricated on a 150mm sapphire substrate. The µ LED epitaxial structure consists of a n-GaN layer, an active region of GaN/InGaN multiple quantum wells (MQW), and a top p-GaN layer. A Cu P contact layer and SiO2 dielectric layer are deposited on epitaxial wafer. Through lithography and etching processes, the matrix pattern of P contacts is then created. GaN mesa etching down to the sapphire substrate fabricates cathode grids, compound barrier layer of Al/TiW/TiWN are then deposited to cover the grids surface. The cathode of the µLED matrix is electro-deposited to fill the mesa grid with ~15 um thick copper layer. (Fig. 1). Eventually, chemical mechanical planarization (CMP) is introduced to flatten the surface and remove copper/barrier layer. The CMP process must be precisely defined to exclude copper/barrier residue while ensuring no loss on the below dielectric SiO2 layer.

In this study, we proposed a 3-platen CMP process (Fig.2) on Applied Materials Mirra Durum® CMP configured with the membrane polishing head by using commercially available acidic slurry with amorphous silica abrasives. The bulk of copper is removed with the high copper removal rate slurry on the platen 1 and the remaining copper is removed at platen 2 with high selectivity slurry. This process is monitored and stopped by endpoint detection with In Situ Rate Monitor (ISRM) system. The ISRM system detects the endpoint at center, mid radius and edge locations on the wafer surface and stops the polishing when the required amount of a polished film is removed.

Once the endpoint is detected, over polishing is defined to compensate for the copper thickness variation and removal rate difference across wafer surface to ensure no copper residual. The barrier layer will not be eroded since the removal rate of barrier layer of the slurry used in this step is extremely low. CMP on platen 3 is defined for barrier removal by another HSS and is also aided by ISRM system.

Cross-sectional scanning electron microscopy (SEM) and optical metrology are utilized to inspect for conductor residue. Neither copper/barrier layer residue nor oxide loss is found at multiple pixels from SEM X-sectional image or by pixel-to-pixel optical inspection of inspection of optical of the fabricated µLED matrix

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Fig.1 Thick Cu integration for GaN µLED

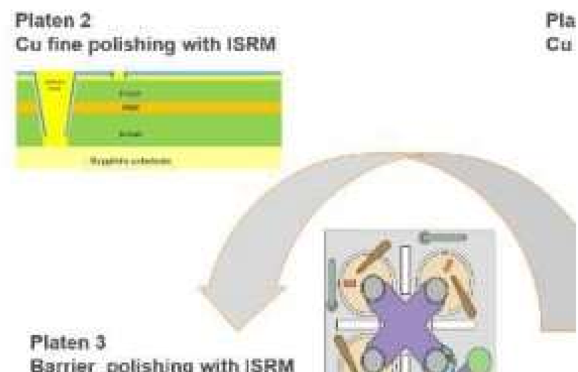

Fig.2 Three platen CMP process for thick Cu integration

Preference: X Oral ☐ Poster

Topic Area: CMP for emerging technologies such as MEMS/LEDs/power devices