Chemical Mechanical Planarization for IGBT Trench Gate Array

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Featured with high input impedance and low on resistance, IGBT (Insulated Gate Bipolar Transistor) is a superior semiconductor power device integrating MOS gate control with bipolar conductivity. The mainstream IGBT is trench field stop type IGBT due to higher cell density and better Vce_sat and Eo for trade-off-current. Chemical mechanical planarization (CMP) is a core process to improve the trench gate structure topography.

Targeting each material layers of the IGBT device, we have developed a CMP process with dedicated consumables combinations including high selectivity slurries (HSS) for polysilicon to oxide film and oxide to polysilicon film. The test was conducted on Applied Materials Mirra Mesa® CMP configured with the 5 zones membrane head. In this paper, the IGBT trench CMP integration solution is summarized including consumable comparisons and process parameter optimization.

The utilization of a 3-platen CMP process provided an optimal control lever for WINWNU, "dishing" and defectivity. The selectivity of chosen slurries maximized the remove rate for the targeted layer (Fig. 1). The platen 1 polysilicon process provided a remaining SiO_2 layer with less than 1.5% uniformity and thickness range of 60A. Across wafer dishing of 25nm (target specification: 20-30nm) was observed. For platen 2, the process focus is to maintain planarity and polish the SiO_2 layer to a thickness of 350±100A. SEM x-sectional images confirm that the remaining SiO_2 thickness and planarity targets (Fig.2). Finally, on platen 3, a de-ionized water (DIW) – poromeric pad buff process was used to reduce CMP induced defectivity.

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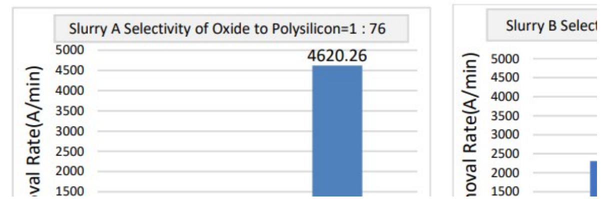

Fig.1 Selectivity for Oxide to Poly CMP and Poly to Oxide CMP

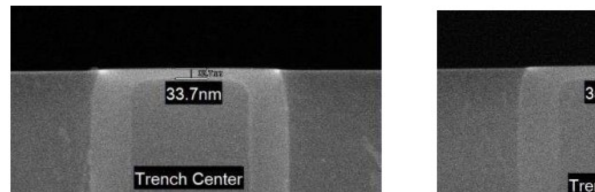

Fig.2 X-sectional SEM confirming remaining oxide and planarity targets

Preference: X Oral ☐ Poster

Topic Area: CMP for emerging technologies such as MEMS/LEDs/power devices