WAFER BEVEL EDGE ENGINEERING: EDGE CLEANING AND BONDING APPLICATIONS

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INTRODUCTION

Damages in the edge region of device wafers can lead to significant loss driving device costs up for semiconductor manufacturers [1]. These damages can extend from scratches or chipping to wafer breakage as thermal and mechanical stress imposed to dies during fabrication lead to an extremely fragile edge area. In addition, edge residues generated after deposition or etching can also significantly affect yield, as the particles tend to move to the wafer's interior after the multiple process steps.
Similar concerns were reported for wafer bonding, which is key process step for several technologies such MEMS and 3D integration [2]. Chipping, defects and high roughness areas can act as point of discontinuity with negative influence on the bonding behavior, generating voids and reducing bonding strengths.
The wafer edge area is a subject of many known phenomena and process non-uniformity. Adapting manufacturing processes to specifically address and prevent edge-related issues cannot be a solution, as it would result in extra costs and could not be generalized to different products lines.

In this context, Ebara Advanced Cleaning system (EAC) offers a perennial way out to address edge process problems. Several key semiconductor manufactures in the last years introduced the EAC systems for different types of applications. The reduced cost of ownership as well as the excellent results accelerate its adoption.

BACKGROUND

Ebara advanced cleaning System (EAC) helps to clean the edge and the bevel of wafers from dopants, metallic contaminants, and deposition residues. In addition, it allows reshaping the wafer edge to strengthen the bevel area. The EAC system includes two modules: Bevel module and Notch module as well as several cleaning modules allowing the use of chemicals for advanced cleaning.

Bevel Polishing:

The polishing process is non-selective, thus not requiring any chemicals for material removal. DIW is used during the process to remove particles generated during the polishing. The polishing is performed using heads with diamond abrasive tapes continually renewed. The heads can tilt to several angles in order to ensure uniform and effective polishing. The main wafer polished areas in the bevel module are top edge, bevel and backside (bottom edge), which prevents permanently contaminants to migrate again to the top active surface (Figure 1a and Figure 1b). Polish amount is controlled from the recipe parameters, such polishing pressure and polishing heads speed. This allows stopping in film or on silicon depending on the addressed application. Abrasive tapes wide selection ensures low wafer surface roughness under 1nm RMS.

Notch Polishing:

The notch polishing process is similar to the bevel one. DIW is used to remove the particles during process while the polishing is ensured by the heads with diamond abrasive tapes. The polishing depth and amount can be controlled from the recipe (Figure 2).

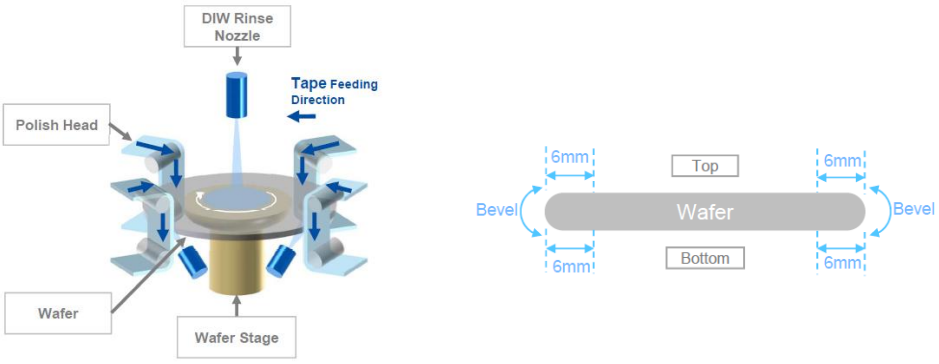

Fig. 1-a Schematic describing Bevel module , Fig. 1-b Wafers areas that can be polished in the Bevel module. Top edge width can vary from 0.8mm to 6mm

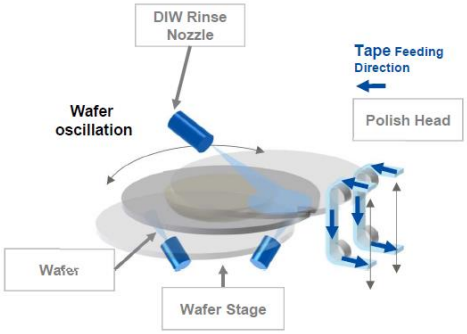

Fig. 2 Schematic describing Notch module

EXPERIMENTAL

In this section, we would like to highlight two different applications for bevel edge polishing with Ebara Cleaning Systems: Film removal to avoid contamination and surface preparation for bonding purpose.

Film removal:

As described earlier, many semiconductor manufactures and R&D institutions adopted EAC systems for several types of applications including decontamination when encapsulation could not be sufficient [3]. We highlight here a case where a 500nm metal film on 200 mm wafer is polished in the edge area (top side and bevel). The process was performed in EAC200bi-hp tool model in three steps for the bevel polishing and two steps for notch polishing. For bevel polishing, we used three different tapes with large size, middle size and small size diamond grains while for notch polishing we used two tapes with large size and small size diamond grains

Surface preparation for bonding purposes:

The test for trim first was performed in EAC300bi-rd model in collaboration with CEA LETI. Only two steps for top edge were required in the bevel module with two different tapes: Middle size diamond grains abrasive to remove ~70µm of silicon, and a fine tape with small size diamond grains to ensure low roughness. The process steps are describes in Figure 3: We performed Top Edge polishing on wafer 1 to create the edge Trim at 2 mm edge exclusion (b). This was followed by a cleaning step before the bonding (c). Wafer 1 undergoes a grinding step at the end of process (d).

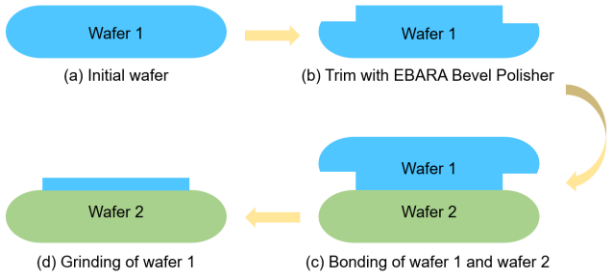

Fig.3 Description of the Trim first process with Bevel polishing step

DISCUSSION

Film removal:

Comparison before and after bevel polishing is shown in Figure 4. SEM (Scanning Electron Microscopy) images show the edge surface condition before the bevel process step and after. SEM observations show no remaining film or residues that can possibly contaminate the wafer interior during the following process steps. The results are similar when it comes to notch area (Figure 5). We used CCD camera for notch observations.

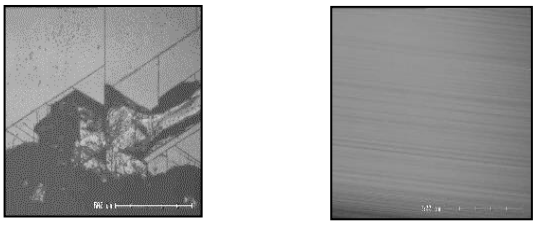

Fig. 4 Wafer edge surface before and after bevel polishing

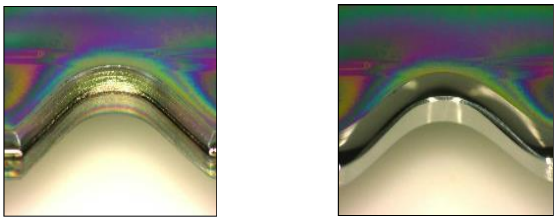

Fig. 5 Wafer notch area before and after notch polishing

Surface preparation for wafer bonding:

We could reach very promising results with EAC system for the Trim first application. Microscope observations in Figure 6 show no defects after the trim bevel polishing process and bonding. We could

demonstrate for the first time, in collaboration with CEA LETI, the bevel capabilities for trim first applications.

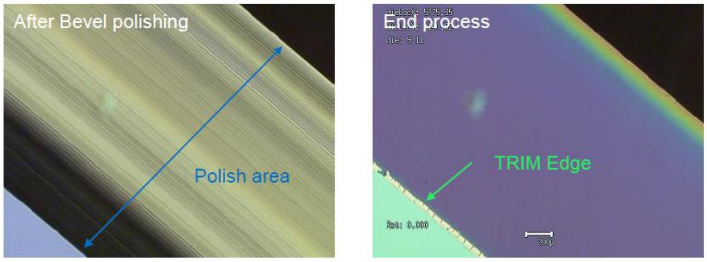

Fig. 6* Trim area condition after bevel polishing (in the left) and at the end of process (in the right)

Scanning acoustic microscope image in Figure 7 shows results after bonding. No defects were observed and results does not only meet state of the art specifications for wafer edge trimming before bonding, but also demonstrate less chipping areas comparing to conventional trim edge machines. We believe we can reach the conventional 100µm polish amount recommended for bonding applications by using a larger size diamond grains abrasive.

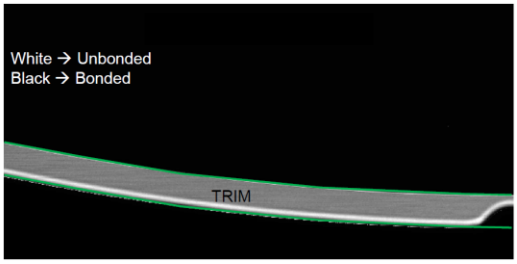

Fig. 7* Scanning acoustic image of the bonded wafers

CONCLUSIONS

Through our collaboration with semiconductor manufacturers and research institutions, we could demonstrate that the EAC system has a clear positive impact on the wafer edge area. It effectively reduces contamination and defects at the wafer edge allowing a better yield and decreasing loss. The EAC system is flexible with proven ability to polish different kinds of materials such Silicon, III-V, Oxide, SiN, Cu, W, Ti, TiN etc. We could also demonstrate high bonding strength at the wafer edge for reduced trim edge exclusion as 2 mm for Trim first applications. In addition, abrasive tapes with large size diamonds grains enable high removal rate as well as larger polish amount, which allows reaching the conventional 100µm trim recommended for bonding.

* Pictures are courtesy from CEA-LETI

[1] Po-Ying Chen et al., Volume 87, Issue 11, 2010, Pages 2065-2070, ISSN 0167-9317.
[2] Roy Knechtel et al., 2021 ECS J. Solid State Sci. Technol. 10 074008
[3] L. Brunet et al.," 2018 IEEE International Electron Devices Meeting (IEDM), 2018, Pages 7.2.1-7.2.4, doi: 10.1109/IEDM.2018.8614653.

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