LOW-k OXIDE CMP PROCESS DEVELOPMENT FOR SUBTRACTIVE METAL INTERCONNECT

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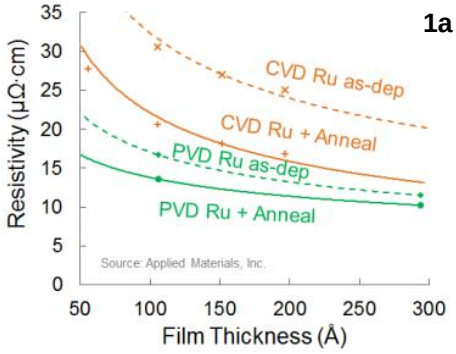
INTRODUCTION

Dual damascene Copper (Cu) has been widely used for BEOL interconnect fabrication. However, due to enhanced grain boundaries and surface scattering, use of Copper (Cu) below 3nm technology node is highly questionable due to increase in RC delay and line resistance (Rs). Effort is being made to replace Cu with alternative metals such as Ruthenium (Ru), Tungsten (W) and Molybdenum (Mo). Key requirement for alternative metal is that it needs to maintain low resistance through the integration cycle and it should have low edge roughness (LER)[1]. Currently, implementation of metal subtractive interconnect scheme is hampered by the availability of an optimized chemical mechanical planarization (CMP) process. Focus of the present work is to highlight CMP process development using low-k dielectric film (SiOCH) and Ru metal lines. Process development was done on blanket and 36nm pitch electrical pattern test vehicle (TV) using standard CMP consumable set and ceria based high selective slurry (HSS). The paper highlights current results and challenges that were encountered during the CMP process development work.

Electrical resistivity of metal wires increases as width decreases. For example, resistivity of 10nm-wide Cu interconnect is expected to be an order of magnitude larger than that of bulk Cu[2]. As alternative interconnect materials, Ru, W, and Mo offer the following advantages[1-3]:

- Low electron mean free path (EMFP) that help reduce sidewall scattering and enables resistance scaling at small dimensions.
- High melting point that enables good electromigration reliability.
- Metal etch feasibility at sub 36nm pitches

In the present work, Ru was selected as an interconnect material because it has low resistivity at smaller dimensions and as shown in the table below, it has better EMFP compared to Mo or W[1,2]. For Ru deposition, both Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD) techniques were considered. Figure 1a shows that PVD Ru having 40% lower resistivity than CVD Ru.



Metal	Melting Point (K)	EMPF (nm)
Cu	1375	39
Mo	2896	11-15
Ru	2607	6.79
W	3695	19.1

Fig. 1a: PVD Ru demonstrates lower resistivity compared with CVD Ru. The table summarizes the melting point and EMFP for Cu, Mo, Ru and W[2,3].

EXPERIMENTAL

Blanket thermal oxide, TeOS & low-k SiOCH wafers were used for CMP process development. For the dielectric material, standard SiO2 film (k~4.0) has been replaced with SiOCH film as it has k~2.4. Wafers were polished on standard consumable set (pad/disk) on Applied's Reflexion LK™ Prime Platform. High Selective Slurry (HSS) comprised of ceria abrasive and polymer additive. Abrasive and additive content were modified by pre-diluting slurry with DIW and by using Point-Of-Use (POU) mixing. Latter was achieved by modifying the abrasive and additive flow rates. POR or baseline mix ratio had lower ceria content compared to optimized slurry mix ratio.

For subtractive interconnect scheme, a 36nm (EUV single print) electrical pattern test vehicle (TV) was used for CMP process development, line resistance, and dielectric reliability studies. Ru metal blanket film was deposited using PVD metal deposition technique. After that 36nm pitch metal Ru lines were achieved through lithography and etch process. Low-k dielectric (SiOCH) was then used to fill the trenches between the Ru metal lines. Flowable CVD technology followed by cure was used to meet the gap-fill requirements. Nitride liner was used to provide good adhesion between flowable low-k film and Ru metal lines. Pre- and Post-CMP film stack for pattern wafer test vehicle is shown in Fig 2a & 2b.

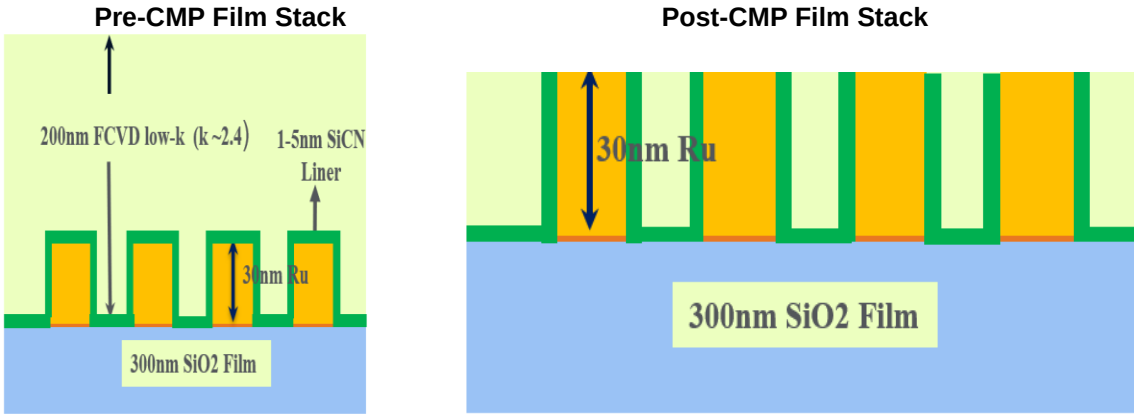
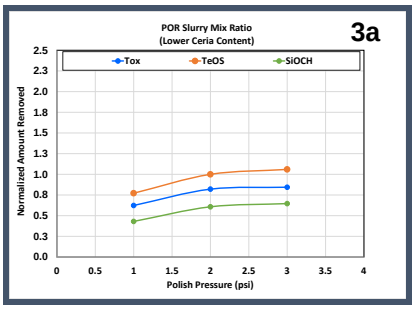


Fig 2a & 2b: Metal Subtractive pre- and post-CMP pattern test vehicle film stack with SiOCH dielectric film and Ru metal lines.

DISCUSSION

The blanket wafers were polished, at various platen/head speed and polish pressures, using the POR and optimized slurry mix ratio. Figure 3 illustrates normalized blanket rate for standard blanket oxide (thermal oxide & TeOS) and low-k SiOCH wafers. The pressure ladder data (1-3psi) indicates that optimized slurry ratio, with higher ceria content, has higher rate compared to POR slurry mix ratio. Figure 4a provides blanket rate comparison between thermal oxide, TeOS and SiOCH wafers. The rate was normalized to thermal oxide removal at 2psi and same platen/head speed. The bar-chart indicates that rate for blanket SiOCH film is much lower compared to thermal oxide and TeOS films. Blanket thermal oxide and TeOS rate for optimized slurry mix ratio is 2-2.5X higher compared to POR mix ratio. Figure 4b indicates the oxide to nitride selectivity difference for POR and Optimized slurry mix ratio at 2psi polish pressure. The latter has better selectivity mainly because it has higher oxide rate compared to nitride film.



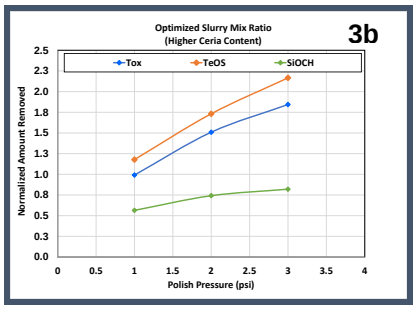
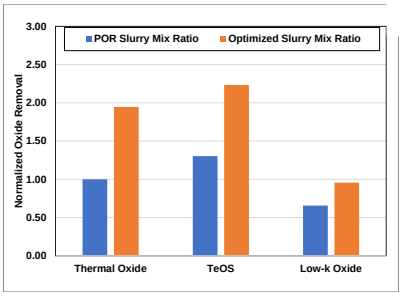


Fig 3a & 3b: Blanket oxide rate for POR & optimized slurry mix ratio. Higher ceria content results in higher oxide rate for all polish pressure and platen/head rpm conditions.



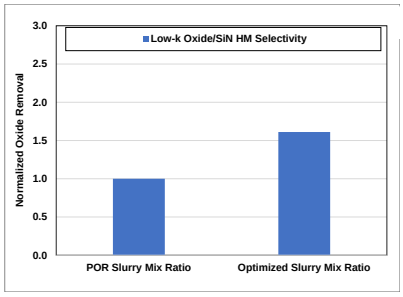
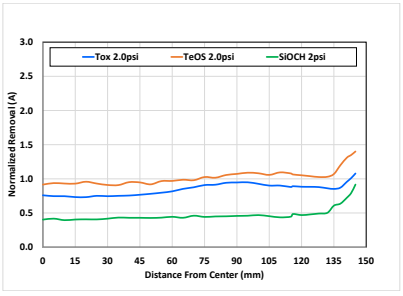
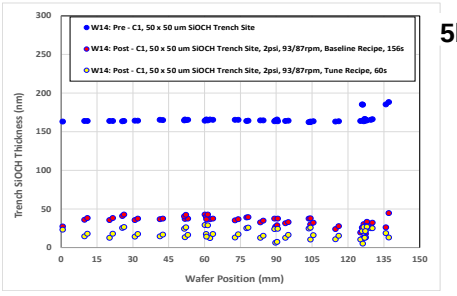


Fig 4a & 4b: Graph illustrates blanket oxide rate and selectivity data. Blanket rate was normalized to 2psi, thermal oxide film removal. Optimized slurry ratio has much higher rate compared to POR mix ratio. The higher rate also results in higher oxide to nitride selectivity.

Blanket thermal oxide, TeOS and low-k oxide profile is shown in Fig 5a. Further optimization of the blanket profile is being sought using Applied Materials Multi-Zone CMP head. Figure 5b illustrates SiOCH pre- and post-CMP thickness for 50 x 50 um trench site of the metal subtractive pattern wafer. Platen Motor torque, shown in Figure 6a & 6b, were used to detect transition from SiOCH to the nitride liner and thereby endpoint the CMP polish. Polish time for optimized slurry mix ratio was around 124s which is significantly lower compared to polish time of 260s for POR mix ratio. Fig 7 shows SEM and API image analysis for polished pattern TV. SEM image illustrates that CMP height difference observed between open area (~37nm) and 36nm pitch density Ru pattern area (~43nm). Figure 7b is the automatic pattern inspection (API) analysis which shows Ru damage issue with CMP overpolish. This can be mitigated by minimizing overpolishing of the wafers, improving with-in-wafer uniformity, and by further optimizing the slurry mix ratio.

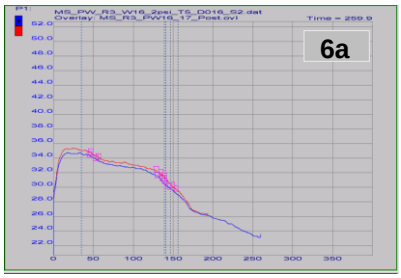


5a



5b

Fig 5a: Profile for thermal, TeOS and SiOCH blanket wafers. 5b: SiOCH pre- and post-CMP thickness data for 50 x 50µm trench site after 156s and 60s polish.



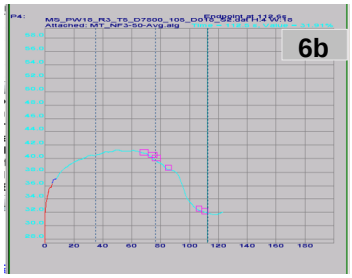
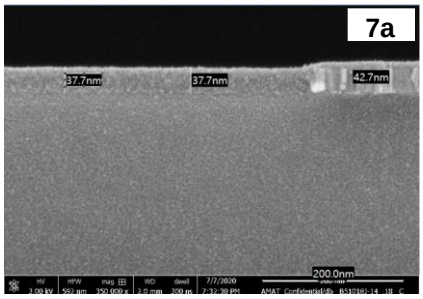
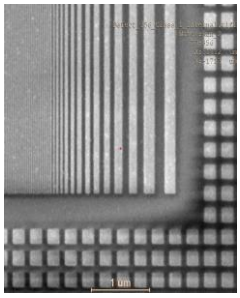


Fig: 6a: Platen Motor Torque signal for pattern TV polished with POR and Optimized slurry mix ratio. Polish time for optimized slurry mix ratio was 124s while that for POR ratio was 260s. By optimizing the ceria content, nearly 50% reduction in polish time was achieved





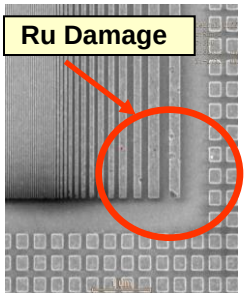


Fig: 7a: SEM cross-section of patterned TV after CMP process. Image illustrates CMP height difference between open (~37nm) and 36nm pitch density Ru pattern area (~43nm). Fig 7b: API analysis with and without Ru damage.

Key challenges encountered during CMP process development were: 1) low SiOCH film removal, 2) improve with-in-wafer uniformity which will help to enhance motor torque signal, and 3) mitigate Ru damage by minimizing wafer overpolish. Currently, additional work is being done to address these issues. Development of a viable CMP solution is important for successful implementation of subtractive metal interconnect for advanced technology nodes.

CONCLUSIONS

Blanket oxide rate was evaluated for different slurry mix ratios. Higher rate was achieved by optimizing HSS mix ratio which resulted in 50% reduction in pattern wafer polish time. Platen motor torque was used to endpoint CMP process. Further improvement in process required to minimize overpolish and mitigate Ru damage.

REFRENCES

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