3-D Contact Engineering for Stacked Nano-Sheets and Beyond Requires Optimized Implant + Anneal Modules!

John Borland

J.O.B. Technologies

Dec 8, 2022

2020 Samsung Memory Suited Over MeV Retrograde Triple Well By Greenthread LLC

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

GREENTHREAD, LLC, a Texas limited liability company, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., a Korean business entity, SAMSUNG SEMICONDUCTOR, INC., a California corporation, SAMSUNG ELECTRONICS AMERICA, INC., a New York corporation, and SAMSUNG AUSTIN SEMICONDUCTOR, LLC, a Delaware limited liability company. Defendants.	Civil Action No. _____ JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Greenthread, LLC ("Plaintiff" or "Greenthread"), by its attorneys, hereby alleges patent infringement against Defendants Samsung Electronics Co., Ltd. ("SEC"), and its U.S. subsidiaries and related entities Samsung Electronics America, Inc. ("SEA"), Samsung Semiconductor, Inc. ("SSI"), and Samsung Austin Semiconductor, LLC ("SAS") (individually or collectively "Defendants" or "Samsung") as follows:

INTRODUCTION

1. This is an action for patent infringement under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq.* Greenthread alleges that Samsung has infringed and continues to infringe, directly and/or indirectly, four Greenthread patents: U.S. Patent Nos. 8,421,195 ("Rao '195" or "'195 patent"), 9,190,502 ("Rao '502" or "'502 patent"), 8,106,481 ("Rao '481" or "'481 patent"), and 9,647,070 ("Rao '070" or "'070 patent") (collectively, the "Greenthread Patents"), copies of which are attached hereto as Exhibits 1-4, respectively.

2. The Greenthread Patents cover foundational semiconductor technologies in the design and manufacture of integrated circuits such as memory, including but not limited to DRAM and NAND flash, and image sensors. Specifically, the Greenthread Patents describe semiconductor devices that employ graded dopants and well regions for, *e.g.*, creating electric fields for aiding and/or retarding the movement of carriers to and/or from the semiconductor surface to/from the semiconductor substrate.

3. Samsung has infringed and continues to infringe the Greenthread Patents, directly and indirectly, by making, using, selling, offering for sale, and/or importing into the United States, semiconductor products with infringing graded dopant regions and/or electronics products containing the same; and, at least from the date of this Complaint, by inducing third parties to use, sell, offer for sale, and/or import into the United States, Samsung semiconductor products with infringing graded dopant regions and/or to make, use, offer for sale, sell in the United States, and/or import into the United States electronics products containing the same, with knowledge of the Greenthread Patents and of the third parties' infringement resulting therefrom.

FACTUAL BACKGROUND

I. The Greenthread Patents

16. Plaintiff Greenthread solely owns all rights, titles, and interests in and to the Greenthread Patents, including the exclusive rights to bring suit with respect to any past, present, and future infringement thereof.

17. The Rao '195 patent, entitled "Semiconductor Devices with Graded Dopant Regions," was duly and legally issued on April 16, 2013, from a patent application filed January 12, 2007, with G.R. Mohan Rao as the named inventor. The Rao '195 patent claims priority from U.S. Patent Application No. 10/934,915 (Pub. No. US 2006/0049464 A1), filed on September 3, 2004.

18. The Rao '502 patent, entitled "Semiconductor Devices with Graded Dopant Regions," was duly and legally issued on November 17, 2015, from a patent application filed October 16, 2014, with G.R. Mohan Rao as the named inventor. The Rao '502 patent claims priority from U.S. Patent Application No. 10/934,915 (Pub. No. US 2006/0049464 A1), filed on September 3, 2004.

19. The Rao '481 patent, entitled "Semiconductor Devices with Graded Dopant Regions," was duly and legally issued on January 31, 2012, from a patent application filed August 27, 2009, with G.R. Mohan Rao as the named inventor. The Rao '481 patent claims priority from U.S. Patent Application No. 10/934,915 (Pub. No. US 2006/0049464 A1), filed on September 3, 2004.

20. The Rao '070 patent, entitled "Semiconductor Devices with Graded Dopant Regions," was duly and legally issued on May 9, 2017, from a patent application filed November 3, 2015, with G.R. Mohan Rao as the named inventor. The Rao '070 patent claims priority from U.S. Patent Application No. 10/934,915 (Pub. No. US 2006/0049464 A1), filed on September 3, 2004.

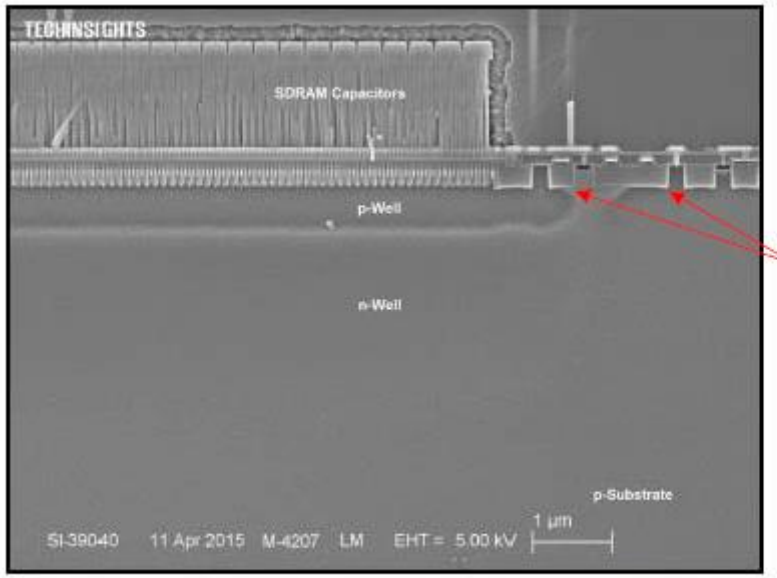


Figure 2.1.3: SDRAM array well structure, SEM cross-section through edges of SDRAM array in bitline direction, silicon etch.

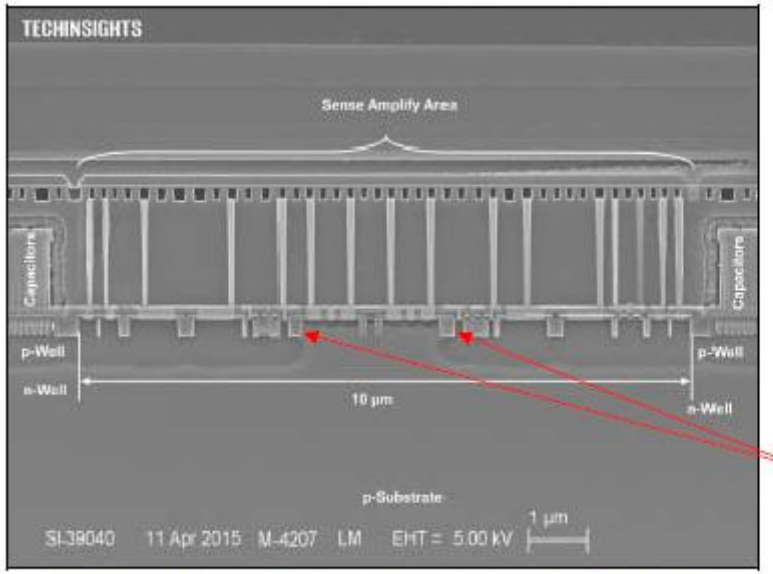


Figure 3.2.1: Sense amplify area between two SDRAM arrays, SEM cross-section in bitline direction with Si etch.

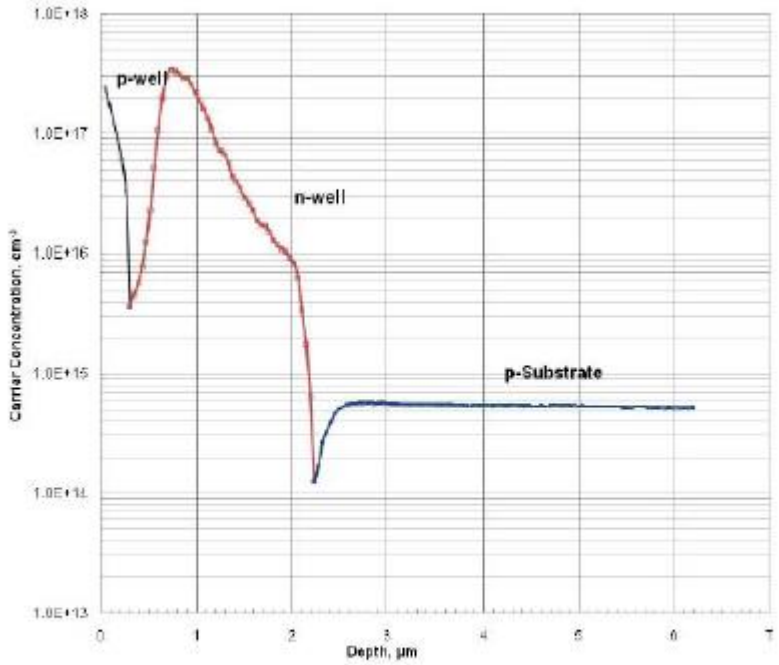


Figure 2.1.2: Spreading resistance profile of an p-well in embedded n-well in SDRAM array.

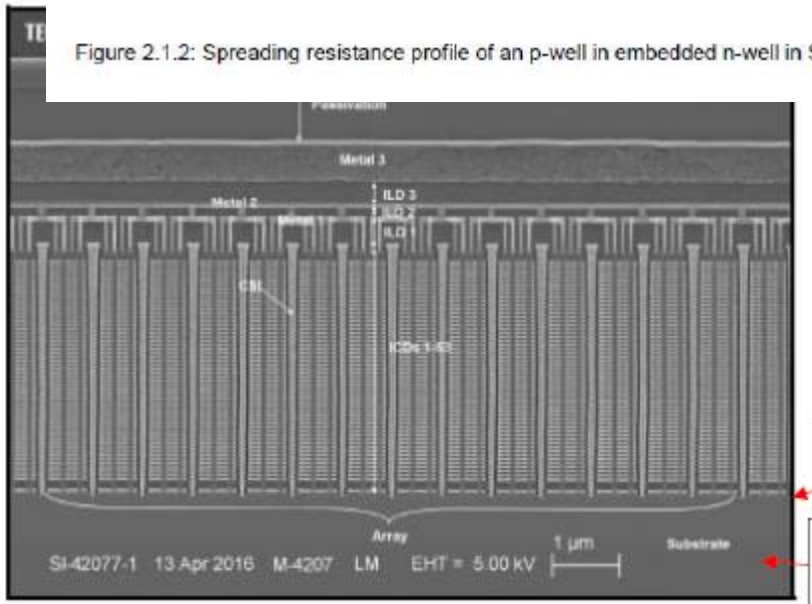


Figure 2.0.2: Process overview, array circuitry (SEM)

117. The Accused NAND Instrumentalities comprise a plurality of well regions,

Samsung's Lawyers Contacted Me in May 2020 For Technical Historical Data

United States Patent [19]

Borland

[11] **Patent Number: 5,501,993**

[45] **Date of Patent: Mar. 26, 1996**

[54] **METHOD OF CONSTRUCTING CMOS VERTICALLY MODULATED WELLS (VMW) BY CLUSTERED MEV BILLI (BURIED IMPLANTED LAYER FOR LATERAL ISOLATION) IMPLANTATION**

[75] Inventor: **John O. Borland**, South Hamilton, Mass.

[73] Assignee: **Genus, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **343,116**

[22] Filed: **Nov. 22, 1994**

[51] **Int. Cl.**[6] **H01L 21/8238**

[52] **U.S. Cl.** **437/34**; 437/154; 437/931

[58] **Field of Search** 437/34, 149, 150, 437/154, 931; 148/DIG. 157

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,710,477 12/1987 Chen 437/34

5,160,996 11/1992 Odanaka 257/375

5,384,279 1/1995 Stolmeijer et al. 437/34

OTHER PUBLICATIONS

Diffusion/Implantation, Dec. 1993 "MeV Implantation Technology Next–generation manufacturing with current–generation equipment" John Ogawa Borland, Ron Koelsch. brochure pp. 1–8.

Fowler, "MosFet Devices with high–gate dielectric integrity", IBM TDB, vol. 17, No. 1, Jun. 1974.

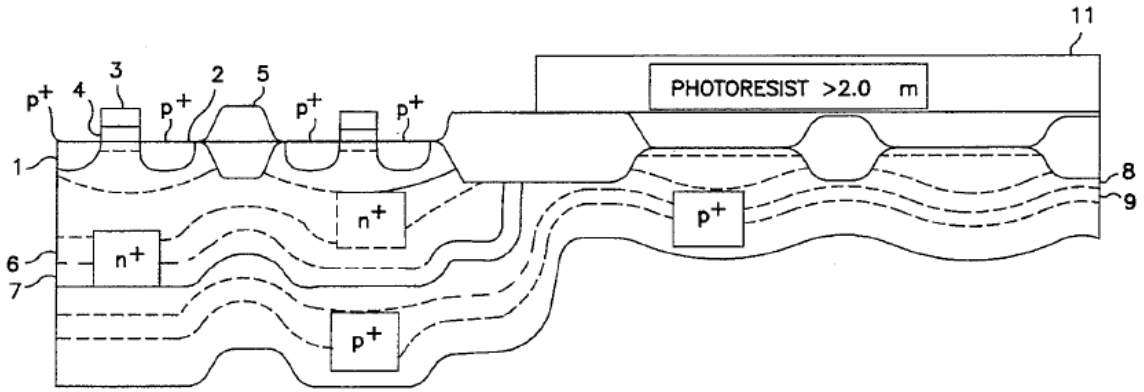
Primary Examiner—Chandra Chaudhari

Attorney, Agent, or Firm—Nields & Lemack

[57] **ABSTRACT**

CMOS vertically modulated wells are constructed by using clustered MeV ion implantation to form a structure having a buried implanted layer for laterial isolation.

21 Claims, 5 Drawing Sheets



United States Patent [19]

Borland

[11] **Patent Number: 5,821,589**

[45] **Date of Patent: Oct. 13, 1998**

[54] **METHOD FOR CMOS LATCH-UP IMPROVEMENT BY MEV BILLI (BURIED IMPLANTED LAYER FOR LATERNAL ISOLATION) PLUS BURIED LAYER IMPLANTATION**

[75] Inventor: **John O. Borland**, South Hamilton, Mass.

[73] Assignee: **Genus, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **822,537**

[22] Filed: **Mar. 19, 1997**

[51] **Int. Cl.**[6] **H01L 29/76**; H01L 29/94

[52] **U.S. Cl.** **257/369**; 257/374; 257/375; 257/376; 438/228; 438/526; 438/529

[58] **Field of Search** 257/369, 374, 257/375, 376; 438/228, 526, 529

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,710,477 12/1987 Chen 437/24

5,160,996 11/1992 Odanaka 257/375

5,292,671 3/1994 Odanaka 437/29

5,384,279 1/1995 Stolmeijer et al. 437/57

5,501,993 3/1996 Borland 437/34

OTHER PUBLICATIONS

Diffusion/Implantation, Dec. 1993, "MeV Implantation Technology Next–generation manufacturing with current–generation equipment" John Ogawa Borland, Ron Koelsch. brochure pp. 1–8.

Fowler, "MosFet Devices with high–gate dielectric integrity", IBM TDB, vol. 17, No. 1, Jun. 1974.

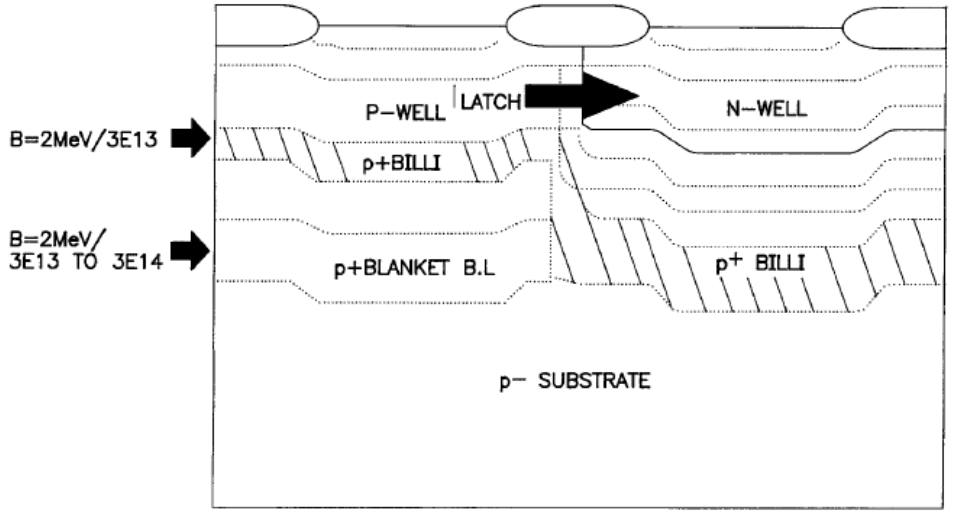
Primary Examiner—Valencia Wallace

Attorney, Agent, or Firm—Nields, Lemack & Dingman

[57] **ABSTRACT**

CMOS vertically modulated wells are constructed by using a blanket implant to form a blanket buried layer and then using clustered MeV ion implantation to form a structure having a buried implanted layer for lateral isolation in addition to said blanket buried layer.

1 Claim, 4 Drawing Sheets

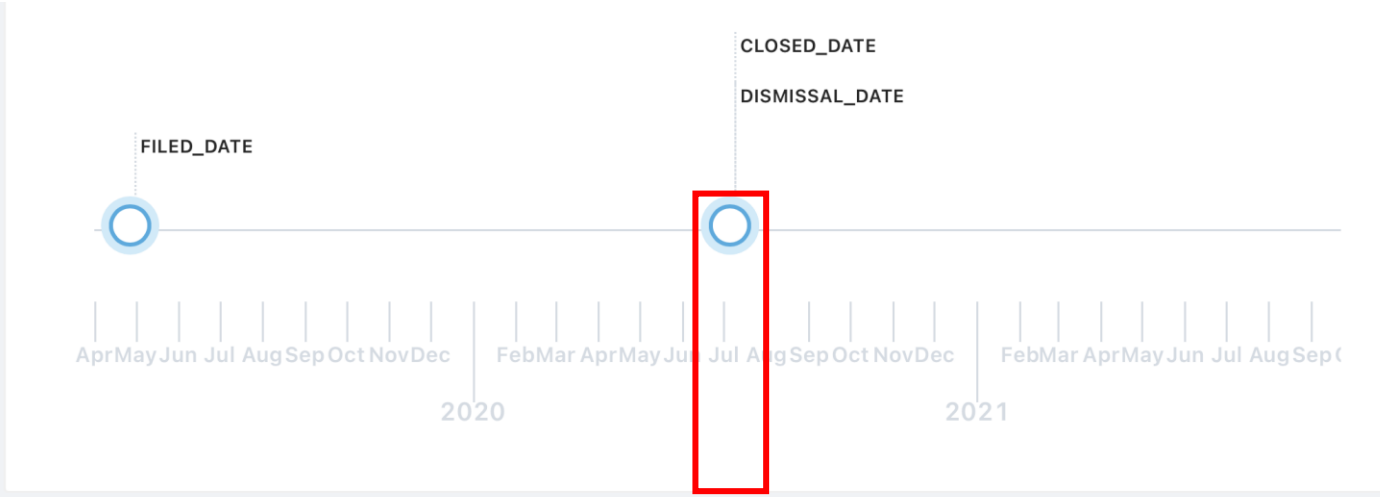


Amend/Correct Docket Control Order. Signed by District Judge Rodney Gilstrap on 7/8/2020. (ch,) (Entered: 07/08/2020)

Notice of Filing of Patent/Trademark Form (AO 120) at termination of case. AO 120 mailed to the Director of the U.S. Patent and Trademark Office. (ch,) (Entered: 07/10/2020)

ORDER granting 104 Motion to Dismiss. ORDERED that Plaintiffs claims for relief against Defendants are DISMISSED WITH PREJUDICE. Signed by District Judge Rodney Gilstrap on 7/9/2020. (ch,) (Entered: 07/10/2020)

Joint MOTION to Dismiss with Prejudice by Greenthread, LLC. (Attachments: # 1 Text of Proposed Order)(Morton, Cyrus) (Entered: 07/09/2020)



Greenthread LLC –vs- Intel/Dell Jan 2022

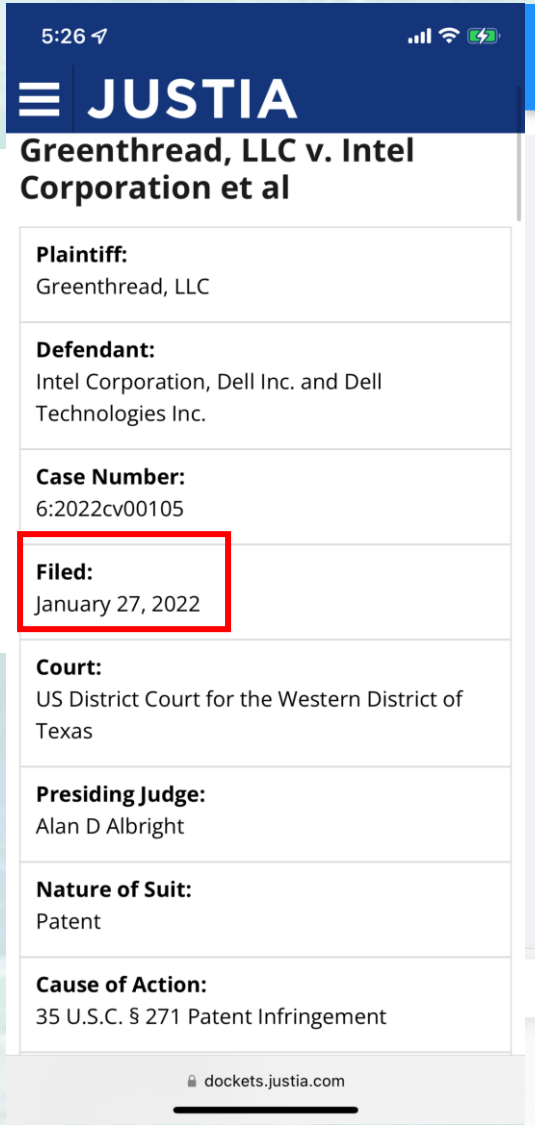
Greenthread Asserts Rao Patents Against Dell and Intel in Single West Texas Complaint (/news/69396-greenthread-asserts-rao-patents-against-dell-and-intel-in-single-west-texas-complaint)

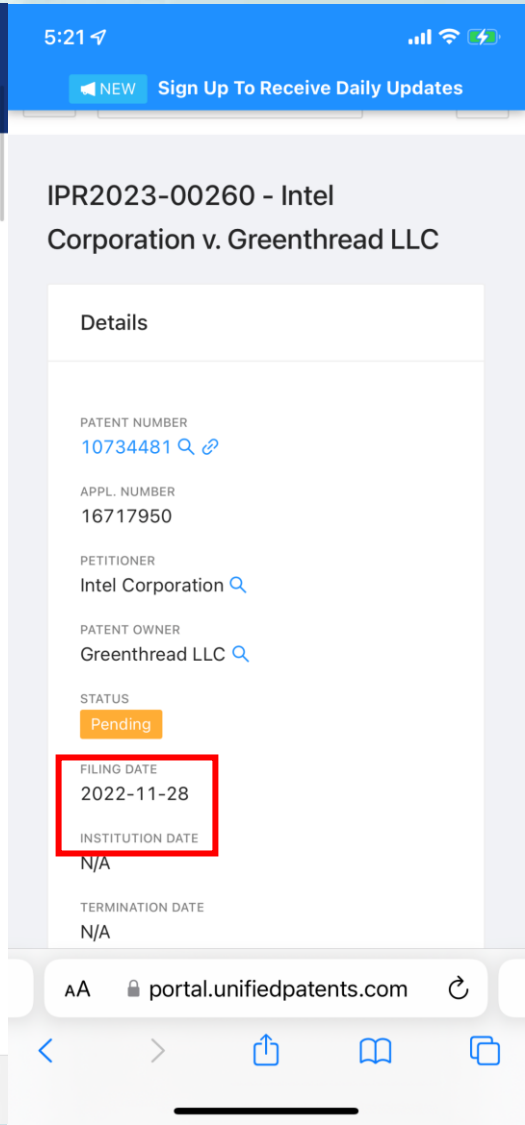
January 30, 2022

Texas plaintiff Greenthread, LLC (https://insight.rpxcorp.com/entity/1120895-greenthread-llc) has sued Dell and Intel (6:22-cv-00105 (https://insight.rpxcorp.com/litigation/txwdce-1160451-greenthread-v-intel)) in a single suit, targeting the provision of Intel's 10th, 11th, and 12th generation of semiconductors (Comet Lake, Tiger Lake, and Alder Lake-series devices), alleged to be incorporated in various Dell laptops (Inspiron, New Inspiron, XPS, New XPS, G15, and Alienware-series products). Greenthread asserts five semiconductor fabrication patents, received from sole named inventor G.R. Mohan Rao, one of the plaintiff's directors. Texas records indicate that this campaign is backed by a funder relatively new to patent monetization.

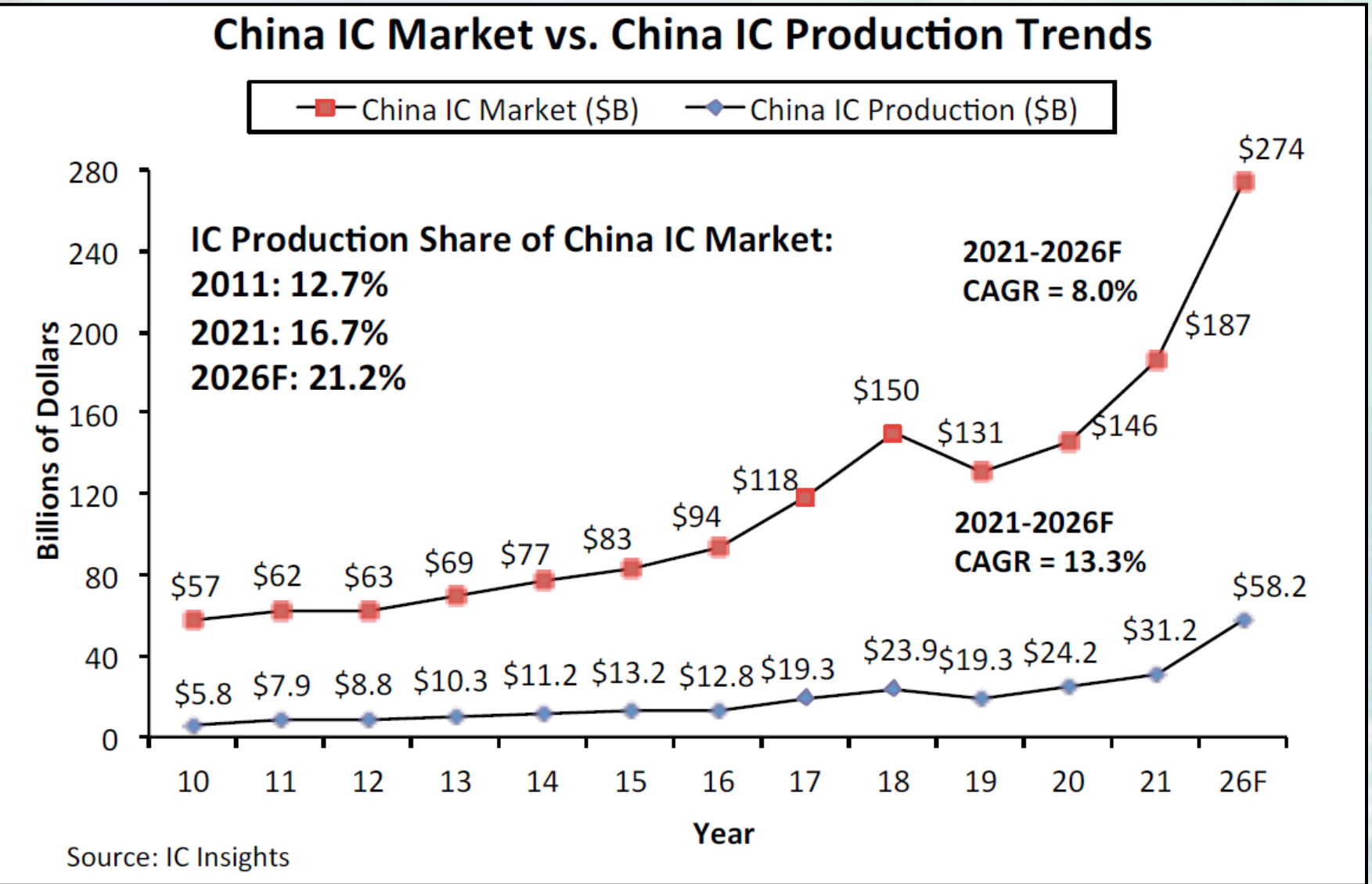
J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Intel Counter Suit





Why Chips ACT? China Only Produces 16.7% And Must Import 83.3% Chips in 2021 compared to 84.5% in 2018



Source: IC Insights

2021	
Worldwide IC Market ($B)	$510.5
China IC Market ($B)	$186.5
China-based IC Production ($B)	$31.2
% of WW IC Market	6.1%
% of China IC Market	16.7%
China-HQ IC Production ($B)	$12.3
% of total China IC Production	39.4%
% of WW IC Market	2.4%
% of China IC Market	6.6%

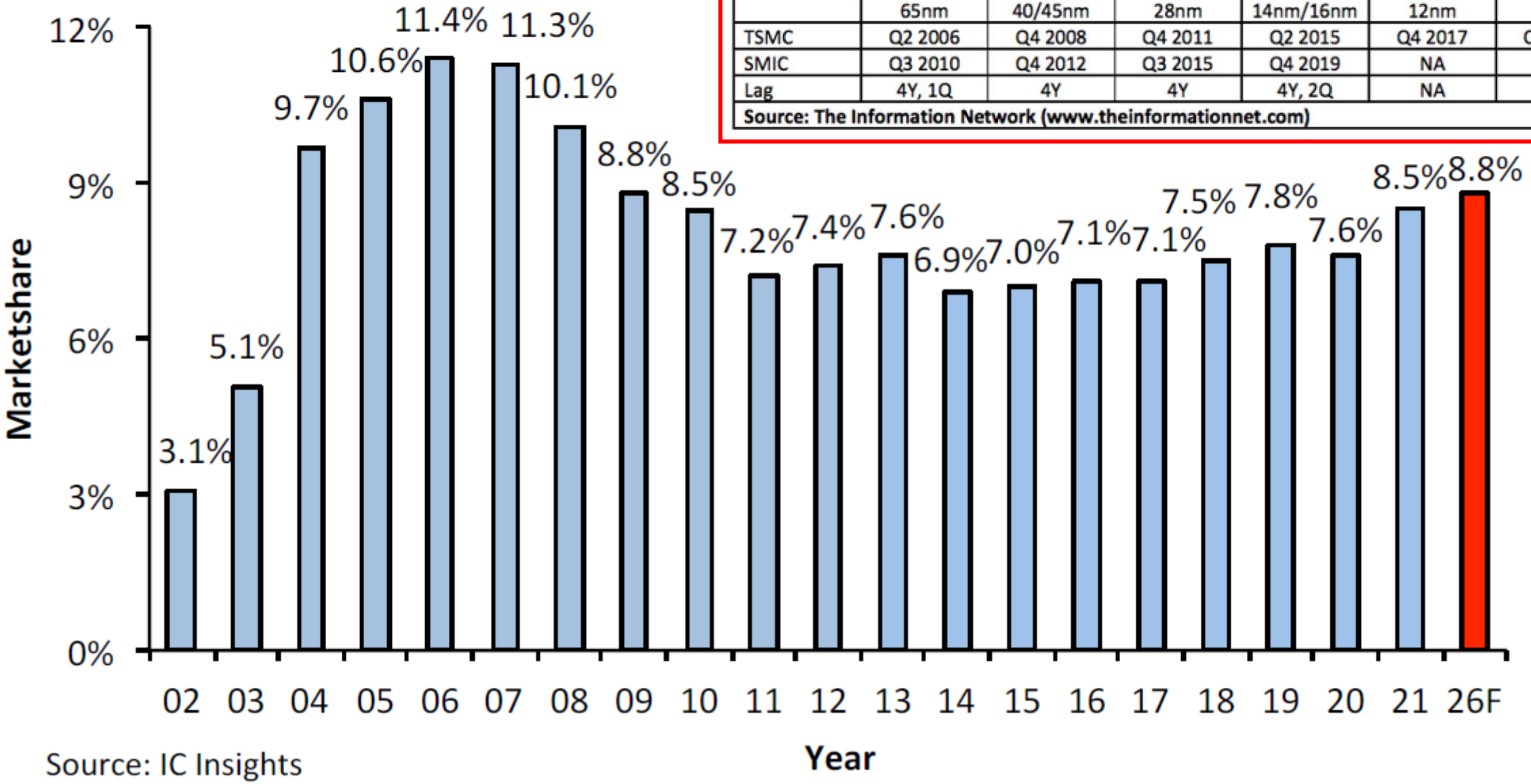
2018	
Worldwide IC Market ($B)	421.7
China IC Market ($B)	155.1
China-based IC Production ($B)	24.0
% of WW IC Market	5.7%
% of China IC Market	15.5%
China-HQ IC Production ($B)	6.5
% of total China IC Production	27.1%
% of WW IC Market	1.5%
% of China IC Market	4.2%

China assembles iPhones, Computers (Apple, Dell, HP etc.)

US needs not semiconductor chip Act but assembly of electronic products in US!

Chinese Companies' Share of the Total Foundry Market

Table 2 - Initial Volume Production Comparison between TSMC and SMIC						
	65nm	40/45nm	28nm	14nm/16nm	12nm	7nm
TSMC	Q2 2006	Q4 2008	Q4 2011	Q2 2015	Q4 2017	Q2 2018
SMIC	Q3 2010	Q4 2012	Q3 2015	Q4 2019	NA	NA
Lag	4Y, 1Q	4Y	4Y	4Y, 2Q	NA	NA
Source: The Information Network (www.theinformationnet.com)						



Source: IC Insights

Capable Players at different Process Nodes

32nm/28nm	22nm/20nm	16nm/14nm	10nm	7nm	5nm	3nm
Panasonic						
STM						
HLMC						
UMC						
IBM		UMC FinFET				
SMIC	IBM	SMIC FinFET				
GF	GF	GF FinFET	SMIC			
Samsung	Samsung	Samsung FinFET	Samsung	Samsung	Samsung	Samsung Nanosheet
TSMC	TSMC	TSMC FinFET	TSMC	TSMC	TSMC	TSMC
Intel	Intel FinFET	Intel	Intel	Intel	Intel	Intel

Seeking Alpha α

Long Ideas

Taiwan Semiconductor Vs. Samsung Vs. Intel: Battle At The Leading Edge

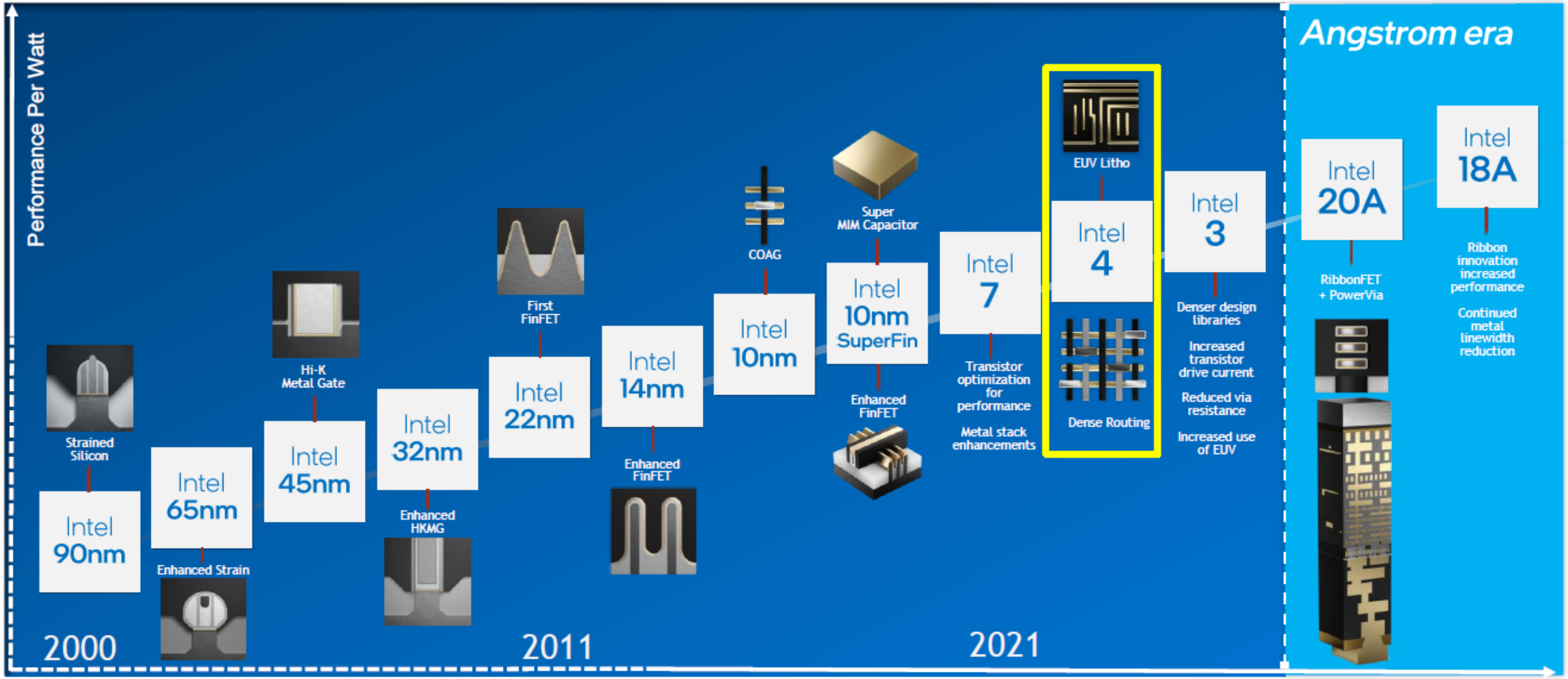
Oct. 27, 2022 8:00 AM ET | **Taiwan Semiconductor Manufacturing Company Limited (TSM)**, **INTC**, **SSNLF**, **SSNNF** | AMD, QCOM, AMZN... | 10 Comments | 12 Likes

Albert Lin, CFA

Sales & Technology)

Technology Node Scaling

Nano-sheet



*Graphics for illustrative purposes only and not to scale.

Key performance booster post 2000 → Strain Si, HKMG, FinFET, DTCO, PowerVia, RibbonFET

(19) **United States**

(12) **Patent Application Publication**

HUANG et al.

(10) **Pub. No.: US 2021/0407999 A1**

(43) **Pub. Date: Dec. 30, 2021**

(54) **STACKED FORKSHEET TRANSISTORS**

(71) Applicant: **Intel Corporation**, Santa Clara, CA (US)

(72) Inventors: **Cheng-Ying HUANG**, Portland, OR (US); **Gilbert DEWEY**, Beaverton, OR (US); **Anh PHAN**, Beaverton, OR (US); **Nicole K. THOMAS**, Portland, OR (US); **Urusa ALAAN**, Hillsboro, OR (US); **Seung Hoon SUNG**, Portland, OR (US); **Christopher M. NEUMANN**, Portland, OR (US); **Willy RACHMADY**, Beaverton, OR (US); **Patrick MORROW**, Portland, OR (US); **Hui Jae YOO**, Portland, OR (US); **Richard E. SCHENKER**, Portland, OR (US); **Marko RADOSAVLJEVIC**, Portland, OR (US); **Jack T. KAVALIEROS**, Portland, OR (US); **Ehren MANNEBACH**, Beaverton, OR (US)

(21) Appl. No.: **16/913,796**

(22) Filed: **Jun. 26, 2020**

Publication Classification

(51) **Int. Cl.**

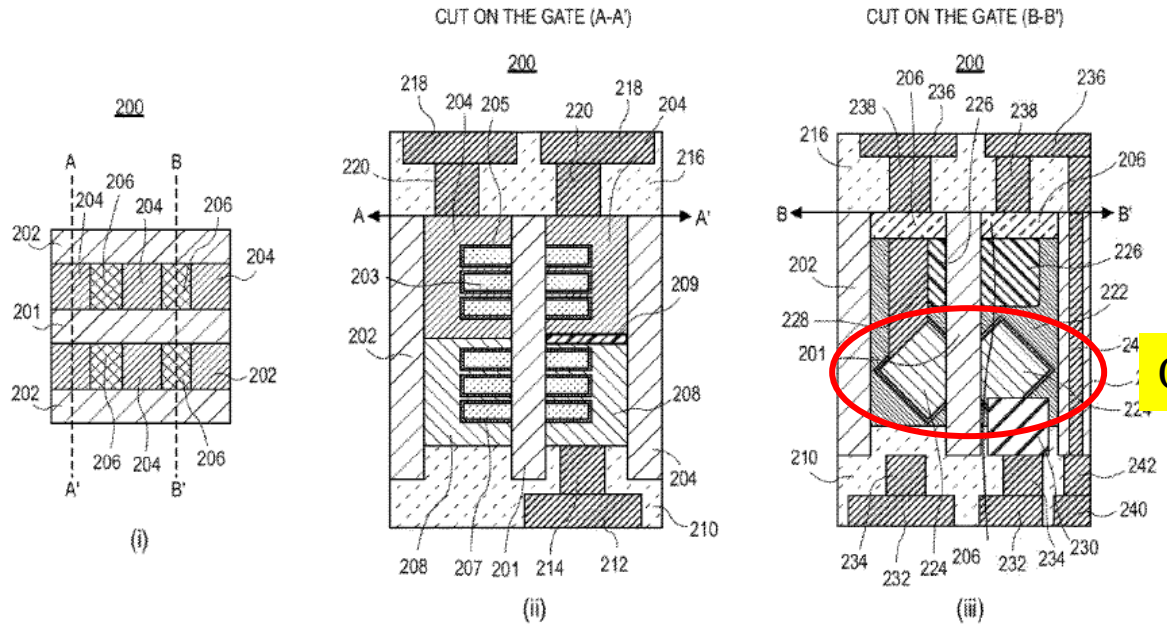
H01L 27/092	(2006.01)
H01L 29/06	(2006.01)
H01L 29/78	(2006.01)
H01L 29/775	(2006.01)
H01L 29/423	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 27/0924*** (2013.01); ***H01L 29/0673*** (2013.01); ***H01L 29/4232*** (2013.01); ***H01L 29/775*** (2013.01); ***H01L 29/7851*** (2013.01)

(57) **ABSTRACT**

Embodiments disclosed herein include stacked forksheet transistor devices, and methods of fabricating stacked forksheet transistor devices. In an example, an integrated circuit structure includes a backbone. A first transistor device includes a first vertical stack of semiconductor channels adjacent to an edge of the backbone. A second transistor device includes a second vertical stack of semiconductor channels adjacent to the edge of the backbone. The second transistor device is stacked on the first transistor device.



Contact Resistance

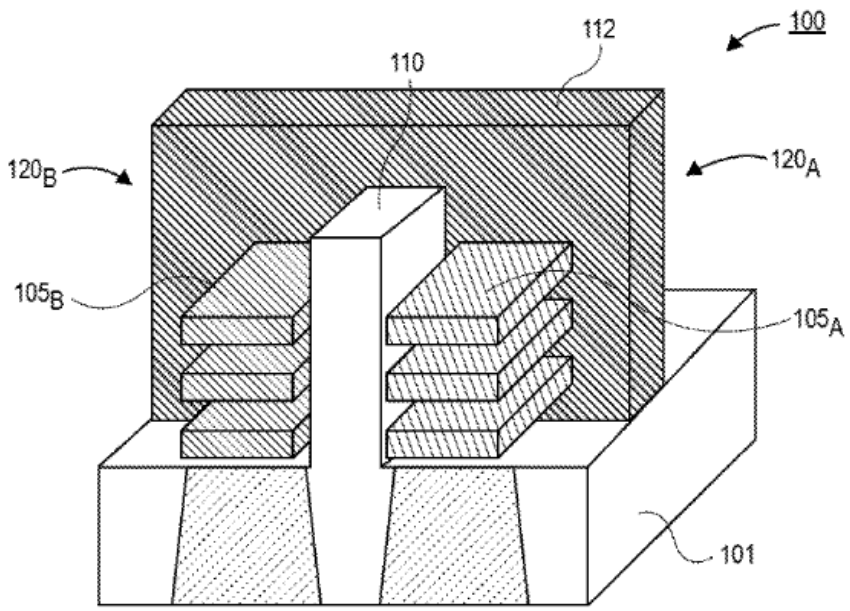


FIG. 1A

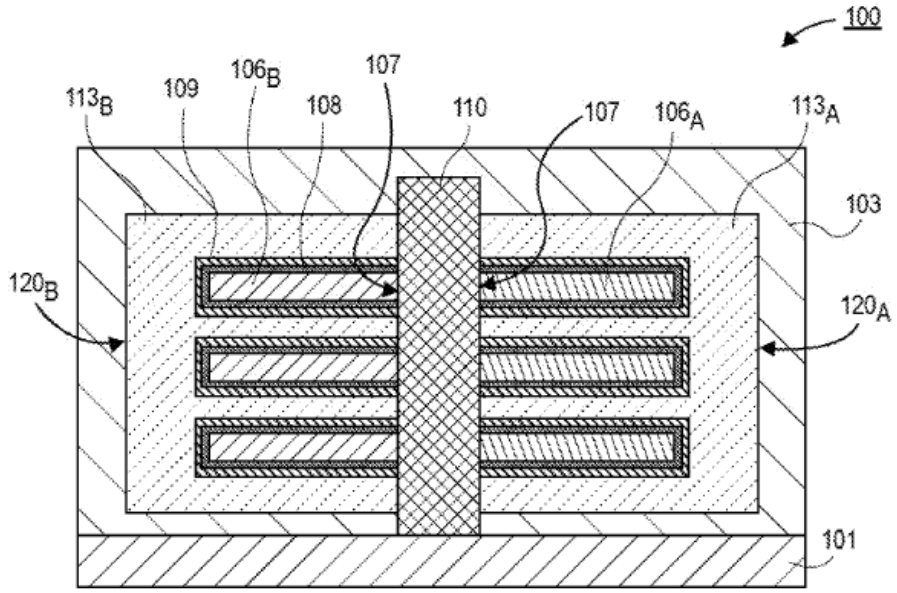


FIG. 1B

Intel's Stacked Nanosheet Transistors Could Be the Next Step in Moore's Law

Process that builds two transistors—one directly atop the other—will boost chip density

By **Samuel K. Moore**

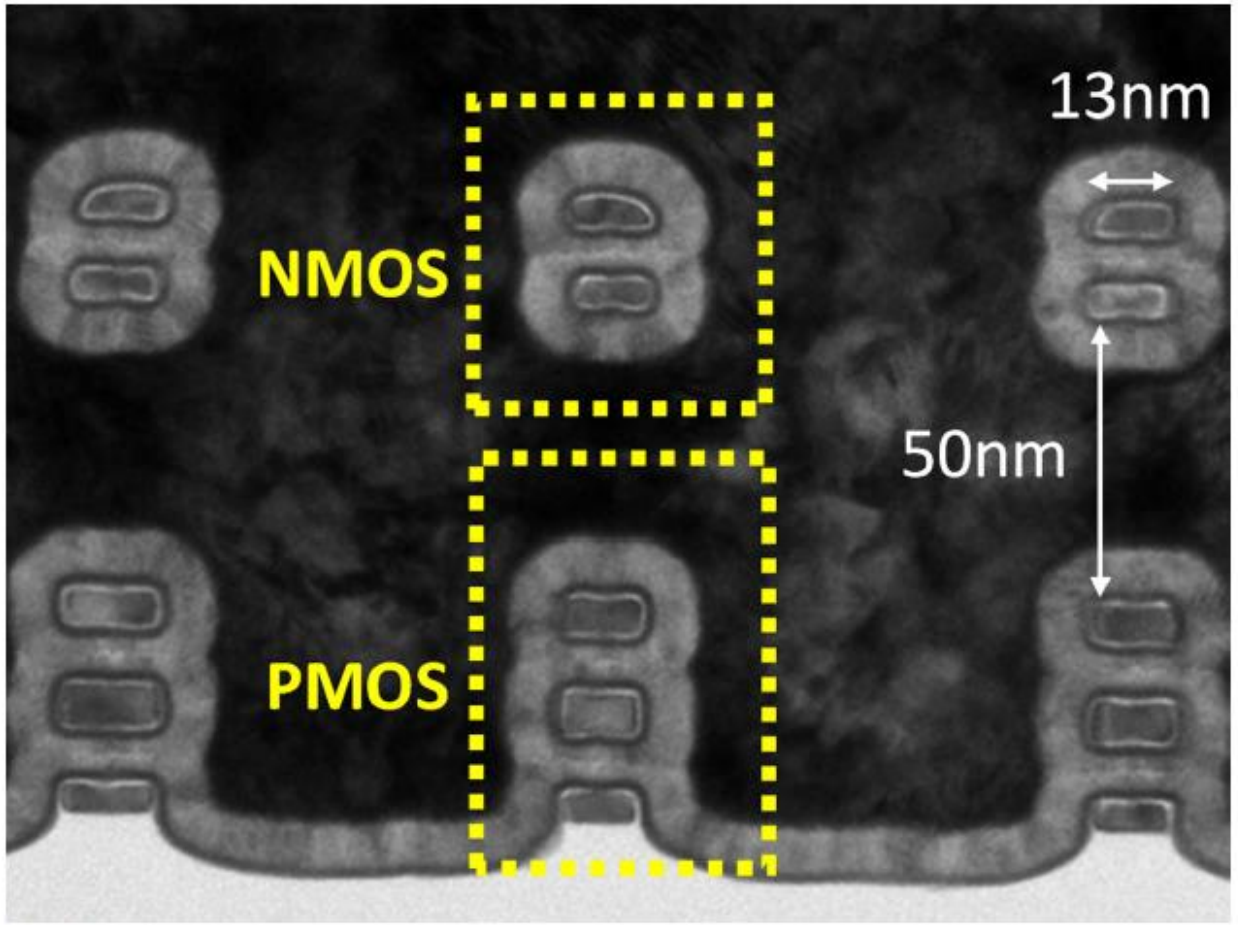
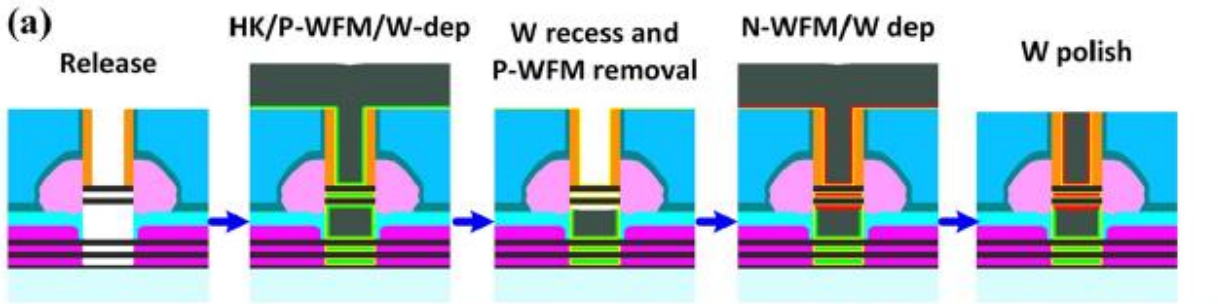
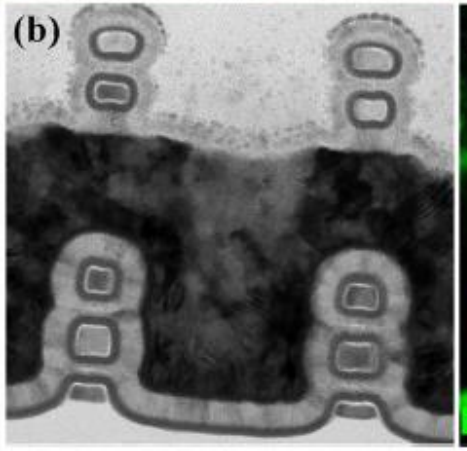
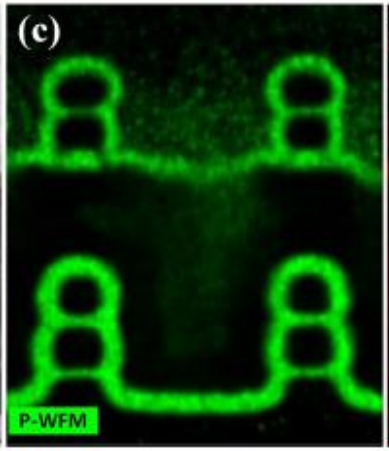


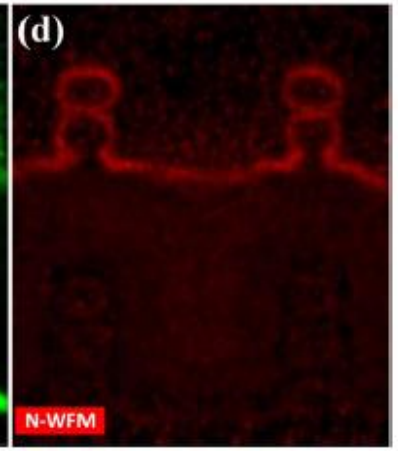
Image: Intel

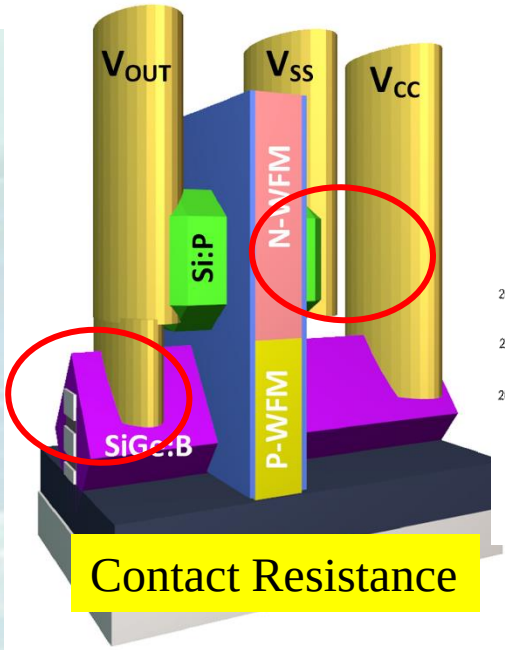
NMOS and PMOS devices usually sit side-by-side on chips. Intel has found a way to build them atop one another, compressing circuit sizes.



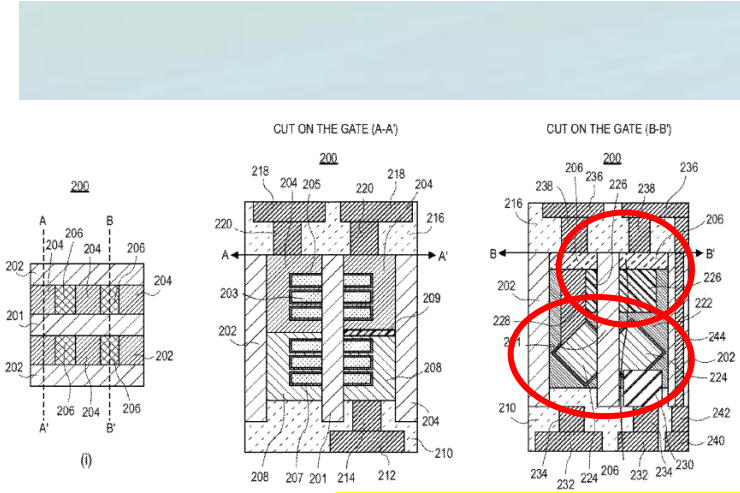








Contact Resistance

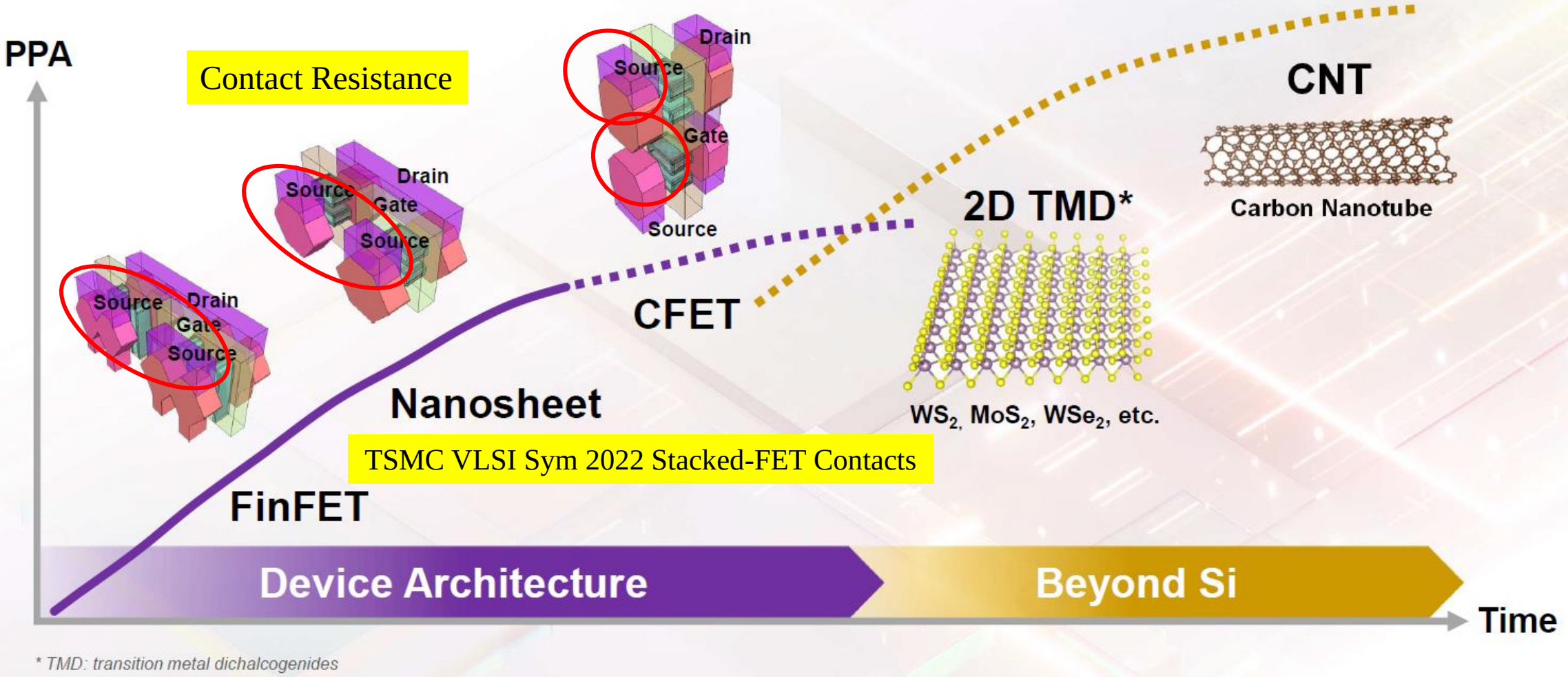


Contact Resistance

Semiconductor Innovations, from Device to System

Yuh-Jier Mii
Research and Development, TSMC, Hsinchu, Taiwan; Email: yjmii@tsmc.com

Device Architecture Outlook



* TMD: transition metal dichalcogenides

Critical Process Features Enabling Aggressive Contacted Gate Pitch Scaling for 3nm CMOS Technology and Beyond

IEDM-2022 paper 27.1

Chih-Hao Chang, V.S. Chang, K.H. Pan, K.T. Lai, J. H. Lu, J.A. Ng, C.Y. Chen, B.F. Wu, C.J. Lin, C.S. Liang, C.P. Tsao, Y.S. Mor, C.T. Li, T.C. Lin, C.H. Hsieh, P.N. Chen, H.H. Hsu, J.H. Chen, H.F. Chen, J.Y. Yeh, M.C. Chiang, C.Y. Lin, J.J. Liaw, C.H. Wang, S.B. Lee, C.C. Chen, H.J. Lin, R. Chen, K.W. Chen, C.O. Chui, Y.C. Yeo, K.B. Huang, T.L. Lee, M.H. Tsai, K.S. Chen, Y.C. Lu, S.M. Jang, and S.-Y. Wu

Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C, email: chihhao_chang@tsmc.com

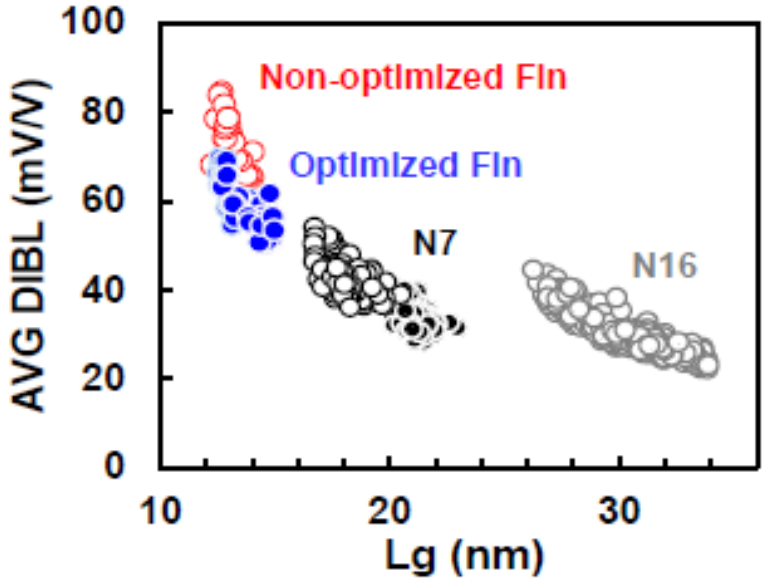


Fig.1 FinFET Lg scaling trend vs DIBL. Fin profile optimization is critical but is at the limit for further Lg scaling.

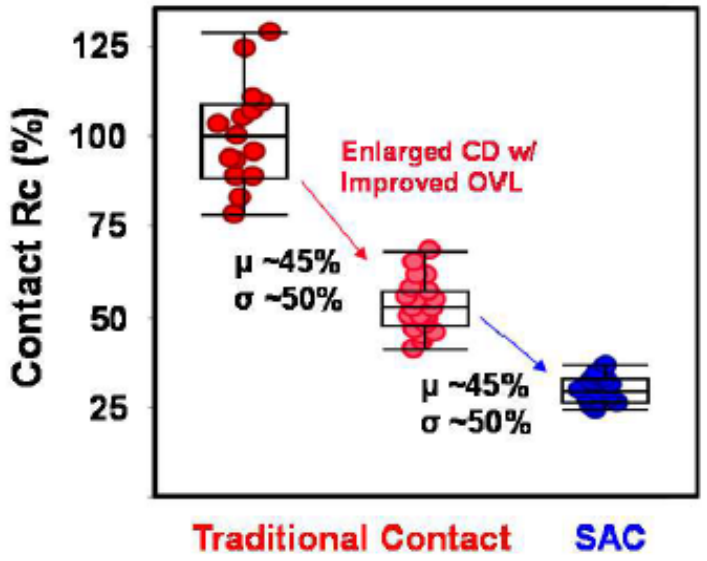


Fig.5 Contact resistance and variation comparison. SAC reduces resistance by 45% and variation by 50% from traditional contact scheme.

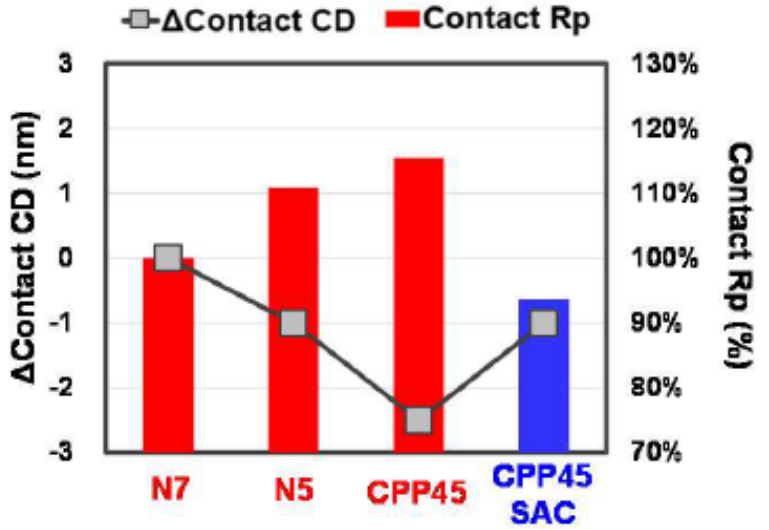


Fig.6 Contact CD and resistance comparison. SAC disrupts CD reduction trend while providing an even smaller resistance in this work.

Said to extend FinFET another generation requires lower contact resistance!

Gate length scaling beyond Si: Mono-layer 2D Channel FETs Robust to Short Channel Effects

C. J. Dorow*[1], A. Penumatcha[1], A. Kitamura[1], C. Rogan[1], K. P. O'Brien[1], S. Lee[1], R. Ramamurthy[2], C. -Y. Cheng[3], K. Maxey[1], T. Zhong[1], T. Tronic[1], B. Holybee[1], J. Richards[2], A. Oni[2], C. -C. Lin[1], C. H. Naylor[1], N. Arefin[4], M. Metz[1], R. Bristol[1], S. B. Clendenning[1], U. Avci[1]
Components Research[1], Quality and Reliability[2], Technology Development[3], Global Sourcing for Equipment and Materials[4],
Intel Corporation, Hillsboro, OR 97214, USA.

Intel IEDM-2022 paper 7.5

Needs Low Contact Resistance For PMOS

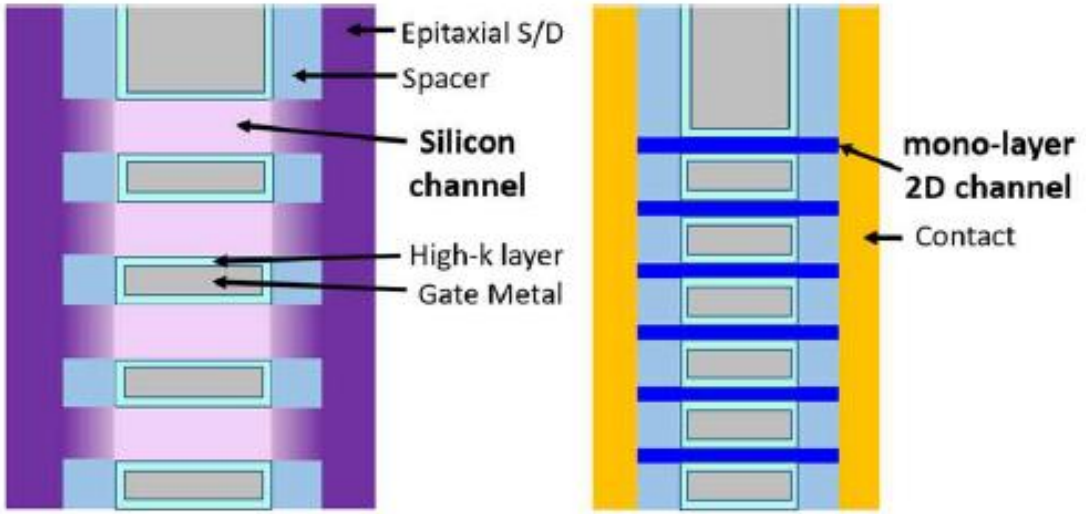


Fig. 1. 2D mono-layer nanosheet channels allow for ultra-scaled gate lengths and increased number of channels per stack height.

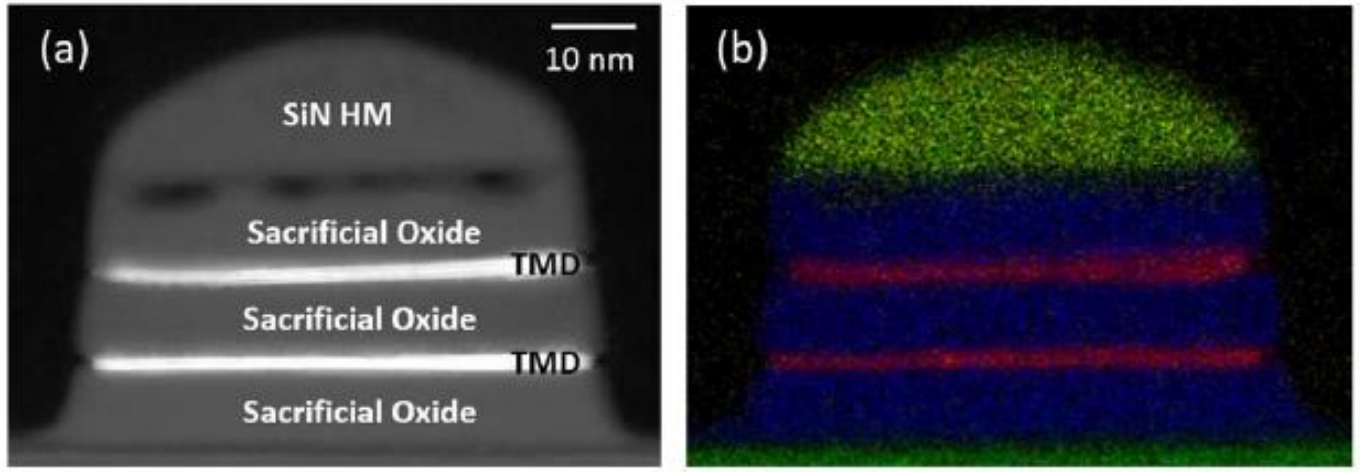


Fig. 2. TEM cross section of a two-layer TMD stacked nanoribbon structure showing 2 – 3 ML per nanoribbon. (b) TEM elemental mapping of stacked 2D nanoribbons.

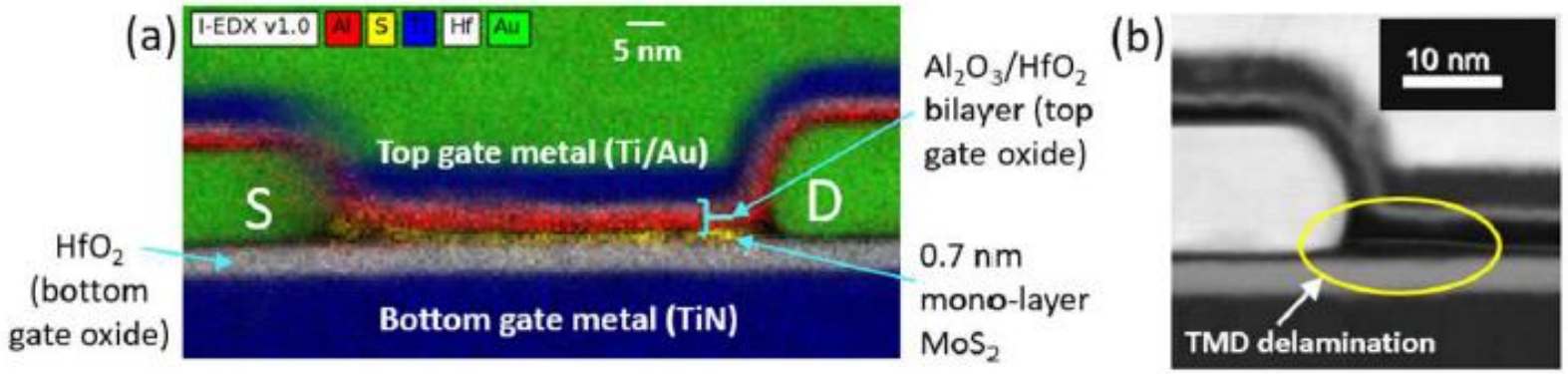


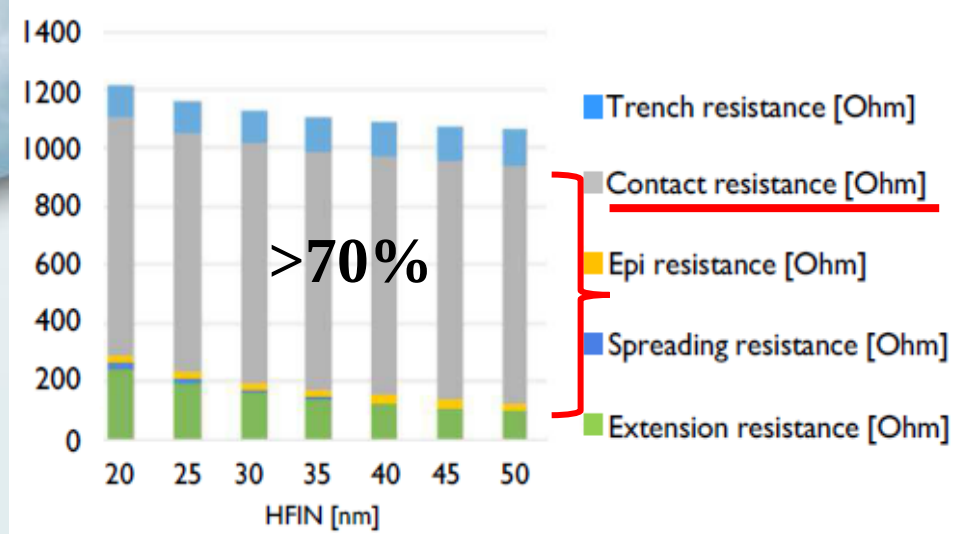
Fig. 6. (a) TEM elemental mapping of double gated device. (b) TMD delamination near S/D contacts.

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

Millisecond and Sub-Millisecond Annealing

Jacob Jensen, Intel, IIT-2022 Sept-2022, TH1.01 paper

- Advanced Precision Annealing Needed
- New Material Modification
- Surface Selective Anneals
  - Maybe Laser Anneal
- Work on Process Variability
- His Last Comment: Contact Resistance is more critical than in the past



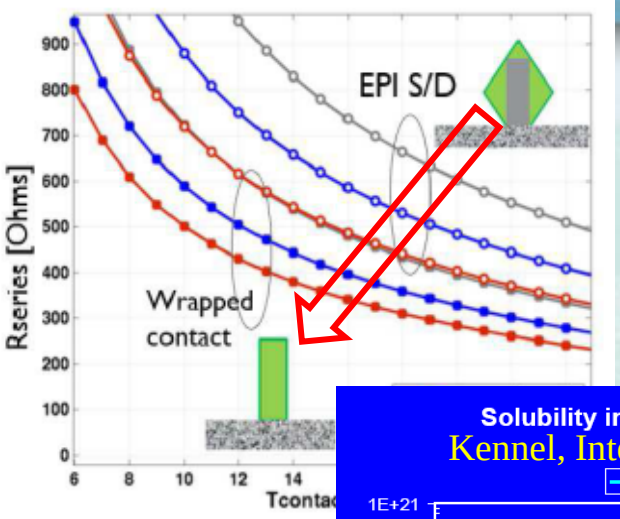
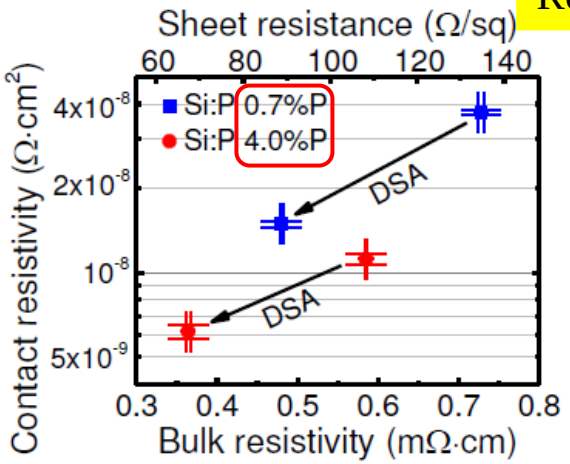
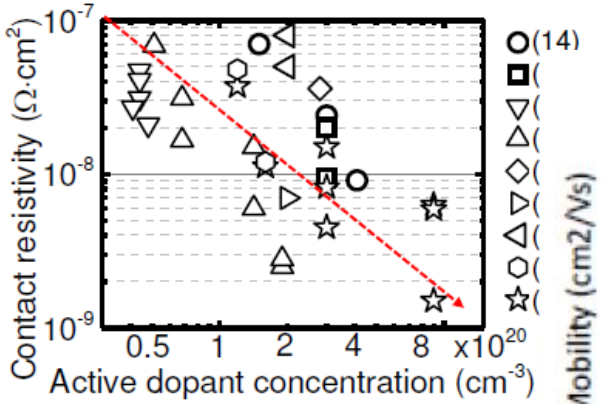
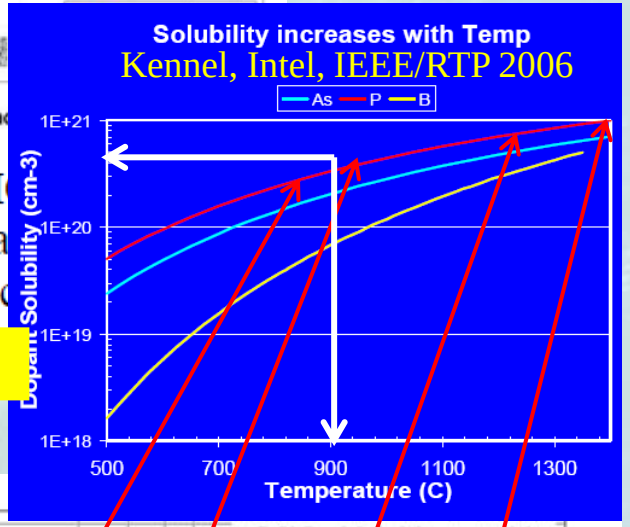


Figure 1. From (1). Left : N7 Series resistance simulations for a 4 fin PM
parts of the device as function of the fin height. Right : N7 Series resista
versus contact width for standard epi S/D contacts and wrapped contac
contact resistivities.

Rosseel et al., IMEC/ASM, ECS Oct 2016







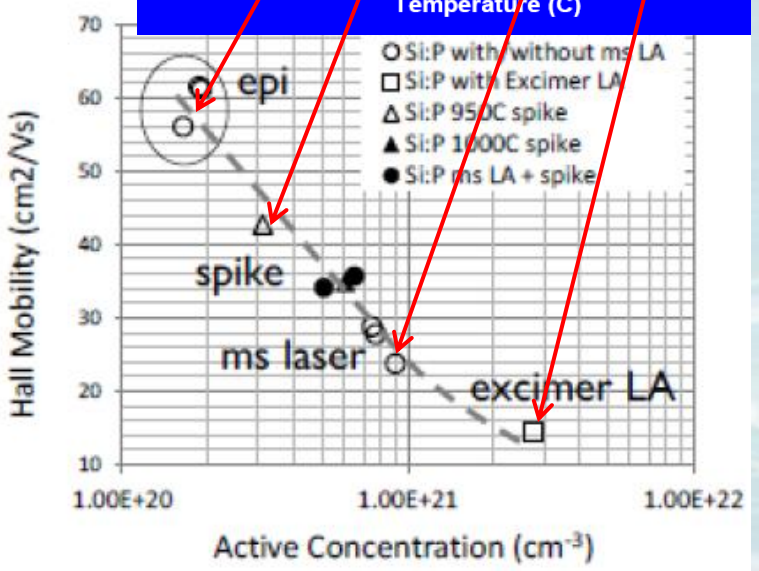


Figure 7. From (22). Left : MR-CTLM based contact resistivity versus sheet resis
layers with different P concentrations ($3 \cdot 10^{20}$ cm^{-3} or 0.7% vs $2 \cdot 10^{21}$ cm^{-3} or 4%)
contact metal. Right : Contact resistivity benchmark plot on n-Si indicating th
importance of the active dopant concentration.

Low temperature source / drain epitaxy and functional silicides: essentials for ultimate contact scaling

IEDM-2022 paper 34.1

C. Porret[1], J.-L. Everaert[1], M. Schaekers[1], L.-A. Ragnarsson[1], A. Hikavyy[1], E. Rosseel[1], G. Rengo[1], R. Loo[1], R. Khazaka[2], M. Givens[2], X. Piao[1], S. Mertens[1], N. Heylen[1], H. Mertens[1], C. Toledo de Carvalho Cavalcante[1], G. Sterckx[1], S. Brus[1], A. Nalin Mehta[1], M. Korytov[1], D. Batuk[1], P. Favia[1], R. Langer[1], G. Pourtois[1], J. Swerts[1], E. Dentoni Litta[1] and N. Horiguchi[1]
[1]Imec. Leuven. Belgium. email: Clement.Porret@imec.be [2]ASM. Leuven. Belgium

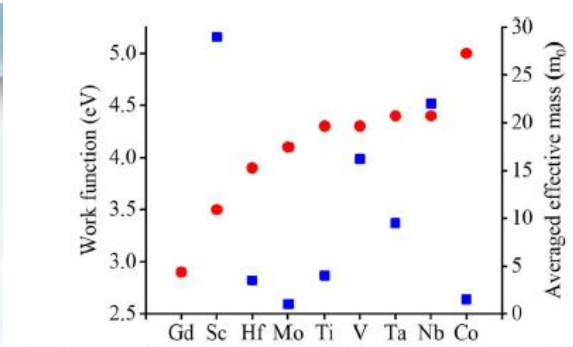


Figure 2. Work function and average effective mass of considered metals.

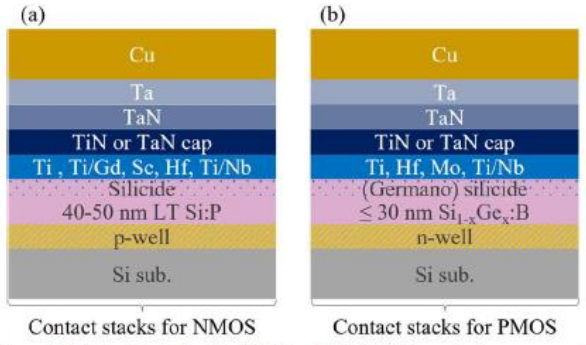


Figure 3. Material stacks for (a) N and (b) PMOS contact assessments.

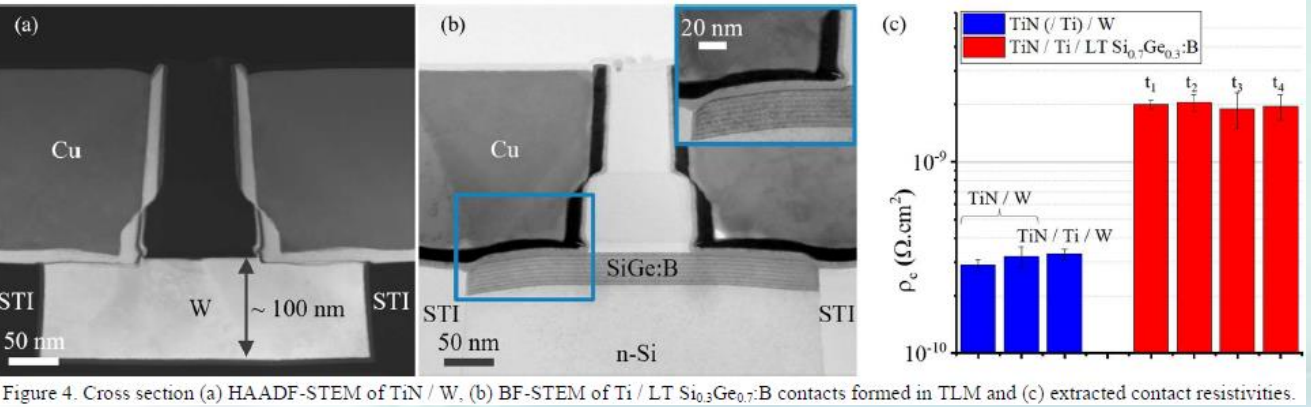


Figure 4. Cross section (a) HAADF-STEM of TiN / W, (b) BF-STEM of Ti / LT $Si_{0.3}Ge_{0.7}$:B contacts formed in TLM and (c) extracted contact resistivities.

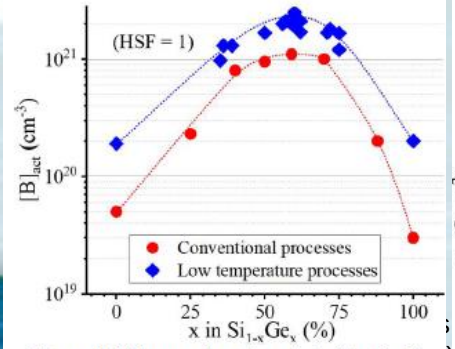


Figure 8. $[B]_{act}$ as a function of x in $Si_{1-x}Ge_x$:B. Dashed lines are guides for the eye.

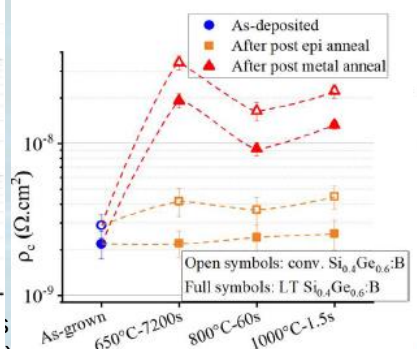


Figure 10. Ti / SiGe:B contact resistivities obtained after several post epi and metal deposition anneals.

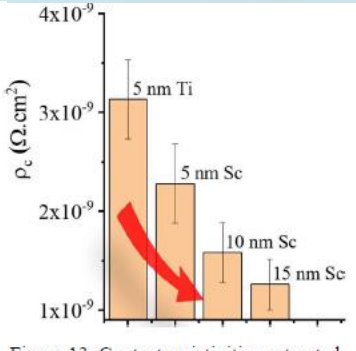


Figure 13. Contact resistivities extracted from Ti and Sc / LT Si:P stacks with various Sc thicknesses.

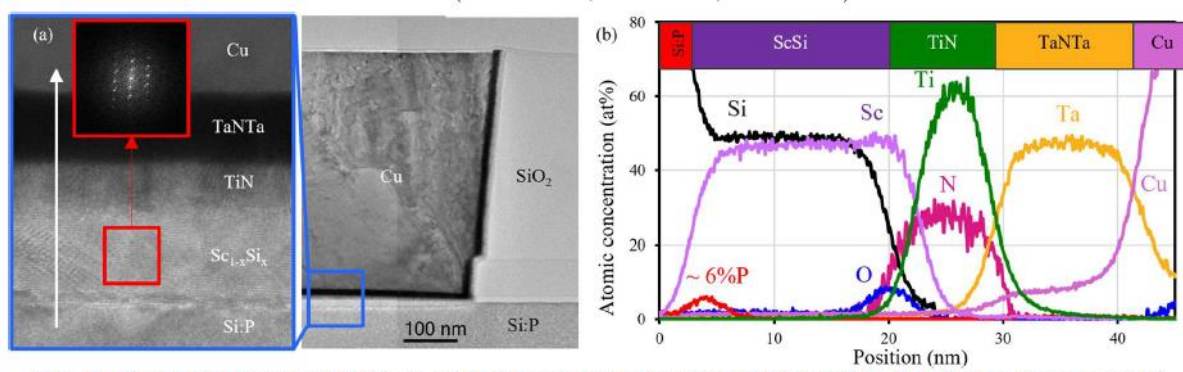


Figure 14. (a) ABF-STEM cross-section of 15 nm Sc / LT Si:P contacts and (b) corresponding EDS analysis, along the white arrow shown in (a).

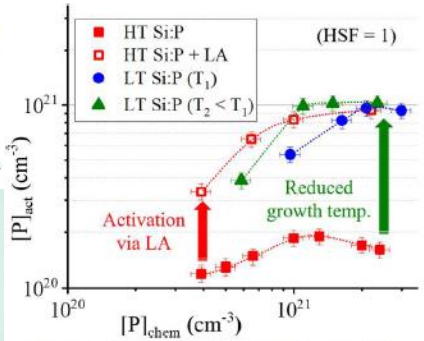


Figure 5. $[P]_{act}$ as a function of $[P]_{chem}$ in Si:P. Dashed lines are guides for the eye.

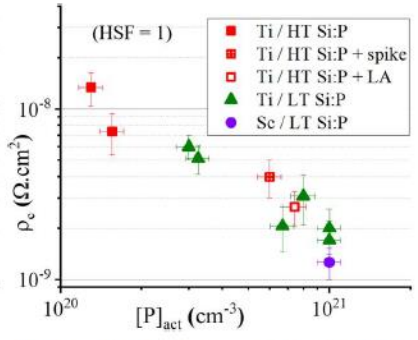


Figure 6. Ti / Si:P contact resistivity as a function of $[P]_{act}$.

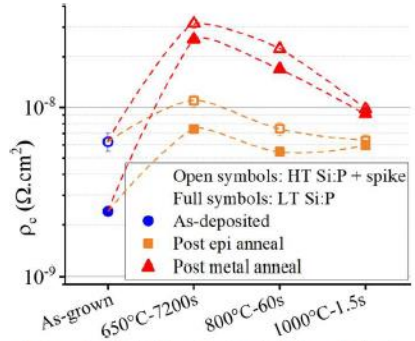


Figure 7. Ti / Si:P contact resistivities obtained after several post epi and metal deposition anneals. Dashed lines are guides for the eye.

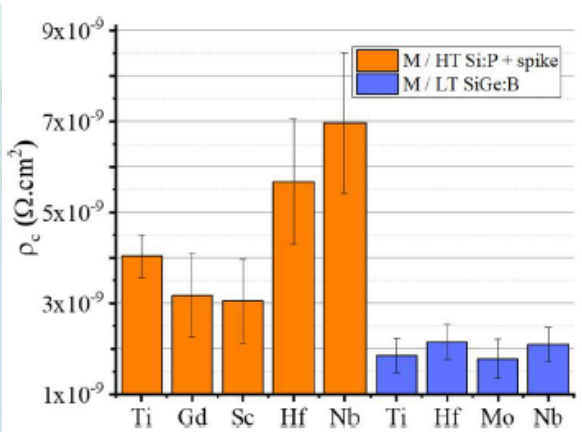


Figure 11. Contact resistivities extracted from various M / SC stacks. The metal (M) films are 5 nm thick.

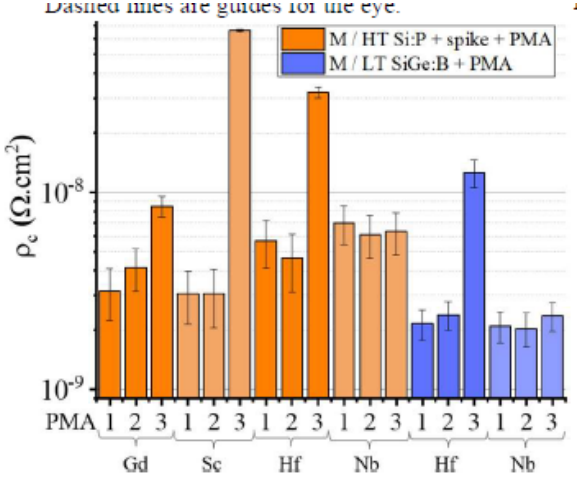


Figure 12. Evolution of M / Si:P and M / SiGe:B contact resistivities extracted for several metals as a function of PMA temperature (1: 420°C-20min; 2: 525°C-1min; 3: 650°C-1min).

Si: Trumbore, Bell Labs, 1959

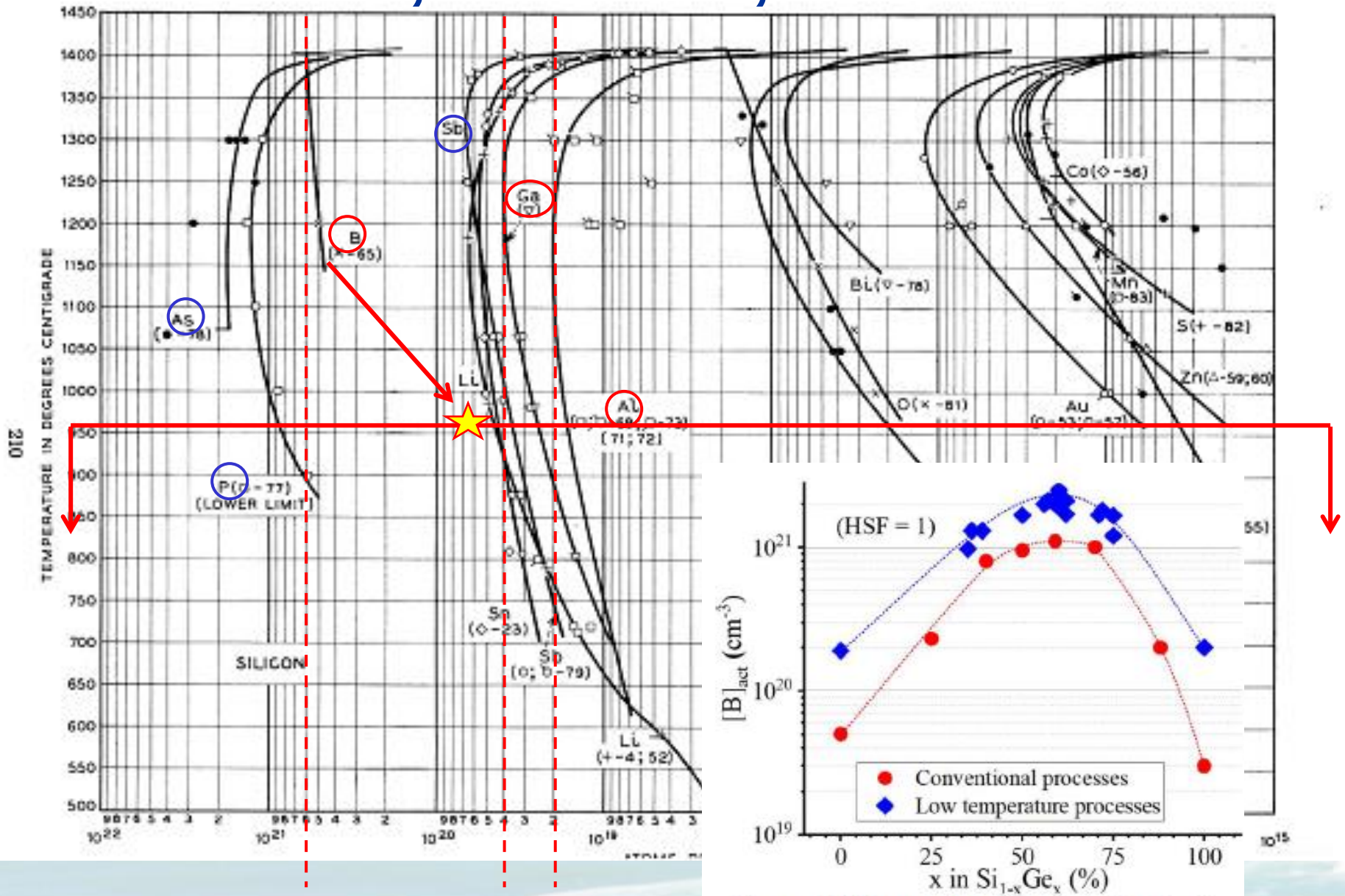


Figure 8. $[B]_{act}$ as a function of x in $Si_{1-x}Ge_x$:B. Dashed lines are guides for the eye.

VLSI Sym June 2016

Session 7: Contact Resistance Innovations for Sub-10nm Scaling

Paper 7.5: UMC/AMAT ultralow p+ SiGe contact resistivity (5.9E-9Ω-cm2)

Paper 7.1: IMEC/AMAT/Samsung ultralow resistivity contacts (2.1E-9Ω-cm2)

Pre-contact PAI

SiP =2E21/cm^3 + **Ge-PAI**=2.1x10^{-9} Ω-cm^2
70%-SiGeB + **Ge-PAI**= 2.1x10^{-9} Ω-cm^2

Paper 7.3: AMAT 7nm node ultralow n+ contact resistivity (<1.0E-9Ω-cm2)

DSA versus nsec laser annealing

Paper 7.4: GF/IBM canceled: Sub-2x10^{-9} Ω-cm^2 N- and P-Contact Resistivity with Si:P and Ge:Ga Metastable Alloys for FinFET CMOS Technology

Paper 7.4: **GF/IBM** paper was withdrawn and not reported nor published. The title said "Sub-2E-9 Ω-cm^2 contact resistivity with SiP and Ge:Ga FinFET. **Ultratech** sent out a press release announcing their LXA nsec laser melt system was used, what a mistake! The **Applied** results in paper 7.3 above and the **IMEC** results in paper 7.1 are all better!

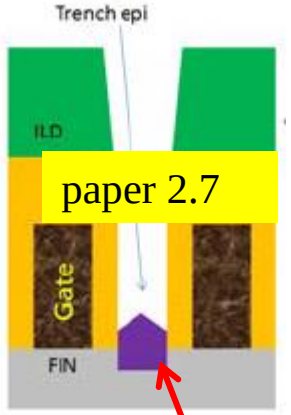
FinFET performance with Si:P and Ge:Group-III-Metal Metastable Contact Trench Alloys

IEDM-2016 paper 2.7

O. Gluschenkov[1], Z. Liu[1], H. Niimi[2], S. Mochizuki[1], J. Fronheiser[2], X. Miao[1], J. Li[1], J. Demarest[1], C. Zhang[1], C. Niu[2], B. Liu[2], A. Petrescu[1], P. Adusumilli[1], J. Yang[1], H. Jagannathan[1], H. Bu[1], and T. Yamashita[1]

[1]IBM Research at Albany NanoTech, 257 Fuller Road, Albany NY 12203, email: olegg@
[2]GLOBALFOUNDRIES Inc., 257 Fuller Road, Albany NY 12203

Abstract— We achieved mid-10^{-10} Ω-cm^2 n-type S/D contact resistivity ($n\rho_c$) and 1.9x10^{-9} Ω-cm^2 p-type S/D contact resistivity ($p\rho_c$) by employing laser-induced liquid or solid phase epitaxy (LPE/SPE) of Si:P and Ge:Group-III-Metal metastable alloys inside nano-scale contact trenches. The Ge:Group-III-Metal alloy allows for a metal-Ge Fermi level pinning effect to lower Schottky barrier height (SBH) while reducing both bulk and unipolar heterojunction resistances. Correspondingly, large R_{on} reduction and I_d gain have been realized in scaled n- and p-FinFETs with the contact length of less than 20nm.



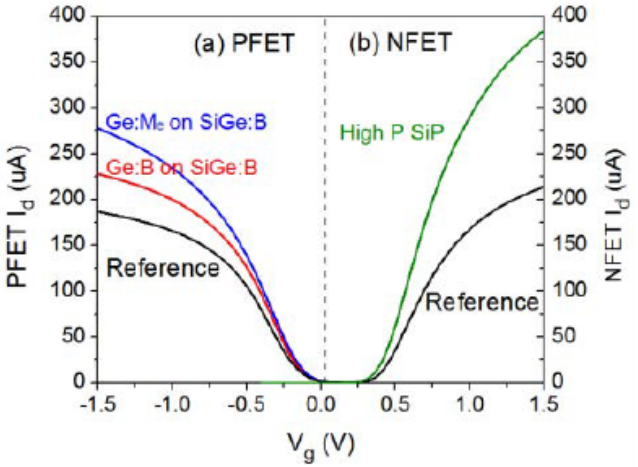


Fig. 7. I_d/V_g characteristics of (a) PFET and (b) NFET. L_g at 20nm, and V_{ds} at 0.05V. Both Ge:Group-III-Metal and Si:P metastable alloys improve electrical properties. NFET and PFET devices are the same as in Fig. 5 and Fig. 16, respectively.

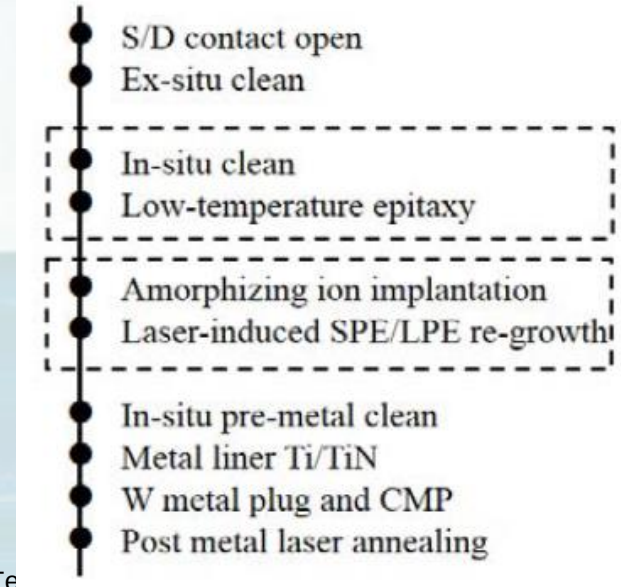


Fig. 2. Process flow for metastable alloy formation.

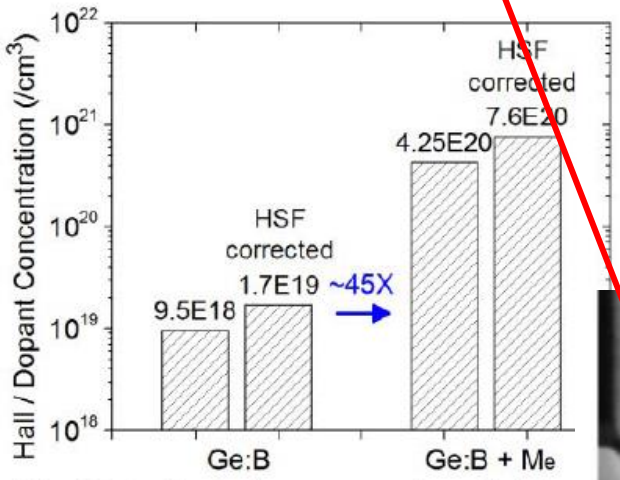
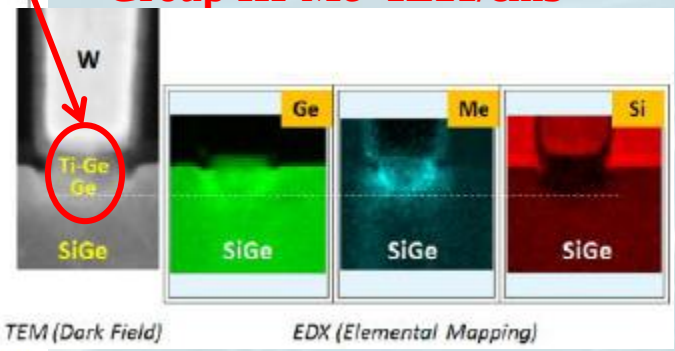


Fig. 12. Active hole concentrations for B ar Group-III-Metal in Ge by Hall measuremen Group-III-Metal chemical concentration [M is ~1x10^{21} cm^{-3} while [B] is ~2x10^{19} cm^{-3}. H scattering factor (HSF) is 1.8.

B=2E19/cm3
Group III-Me=1E21/cm3



Paper 16.1: Liu of **IBM/GF/UTEK** reported on their study using UltraTech's non-melt msec laser (LSA) versus melt nsec 532nm laser for low n+ and p+ contact resistance. Fig.2 below shows the process flow of S/D contact formation by SPE and LPE using an amorphous-SiP pocket on n+ SiP-S/D or amorphous-Ge pocket on p+ SiGe-S/D. The process window for LPE (liquid phase epi) is shown in Fig.5 versus Ge content and Table 1 shows actual results for specific laser power levels. Fig.7 shows X-TEM for the n+ contact using SiP with non-melt msec LSA. Fig.9 below shows n+ contact resistance results with melt laser values much lower than non-melt msec LSA result but yield fails for nsec laser anneal temperatures >1300C due to gate stack damage. Fig.8 shows p+ contact resistance results with non-melt msec LSA showing best result at 800C while all the nsec laser melt results were worse also for Fig.11. Gate stack yield failure occurs also at >1300C.

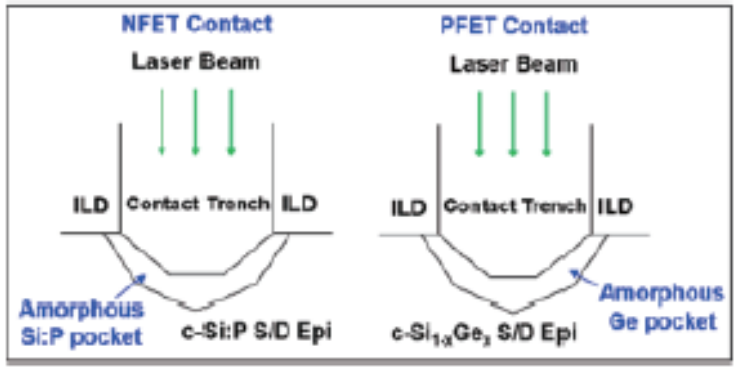


Fig.2 Process flow of S/D contact formation by SPE/LPE.

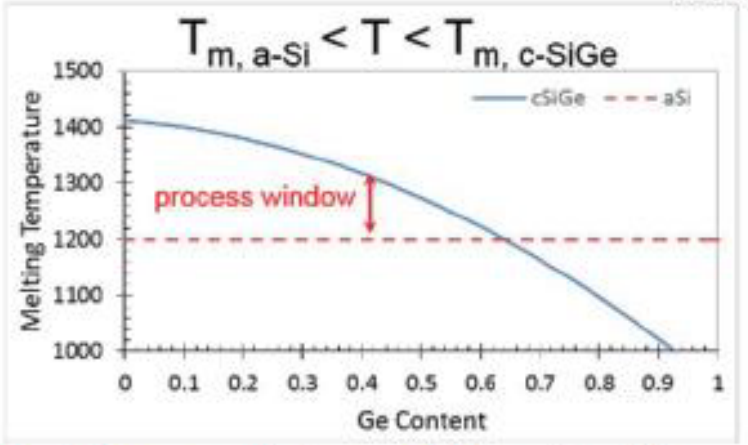


Fig.5 Process window of LPE: a-Si, SiGe.

Wafer	Pre-heat	Power%	Target T
A	700 C	90	1396 C
		82	1335 C
		74	1273 C
		66	1211 C
B	450 C	64	945 C
		56	883 C
		48	821 C
		40	759 C

Si(1-x)	Ge(x)	liquidus
1	0	1412
0.8	0.2	1380
0.5	0.5	1274
0	1	940

Table.1 (a) pre-heat & nSec laser power settings and interpolated temperatures, (b) Si & SiGe liquidus vs Ge content.

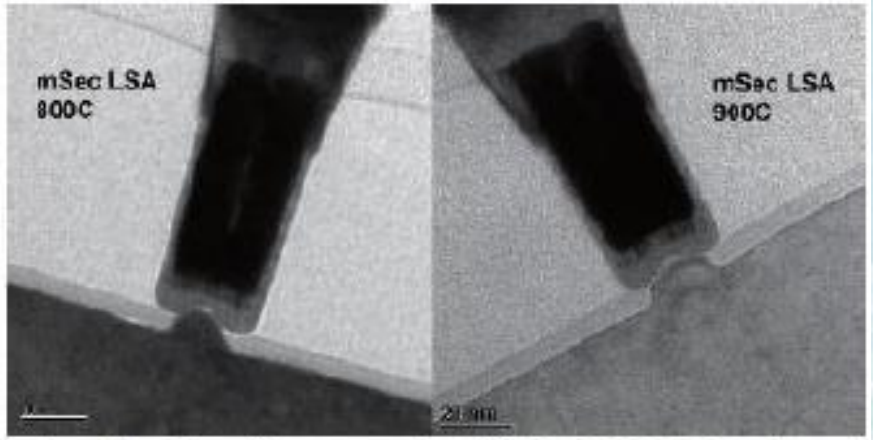
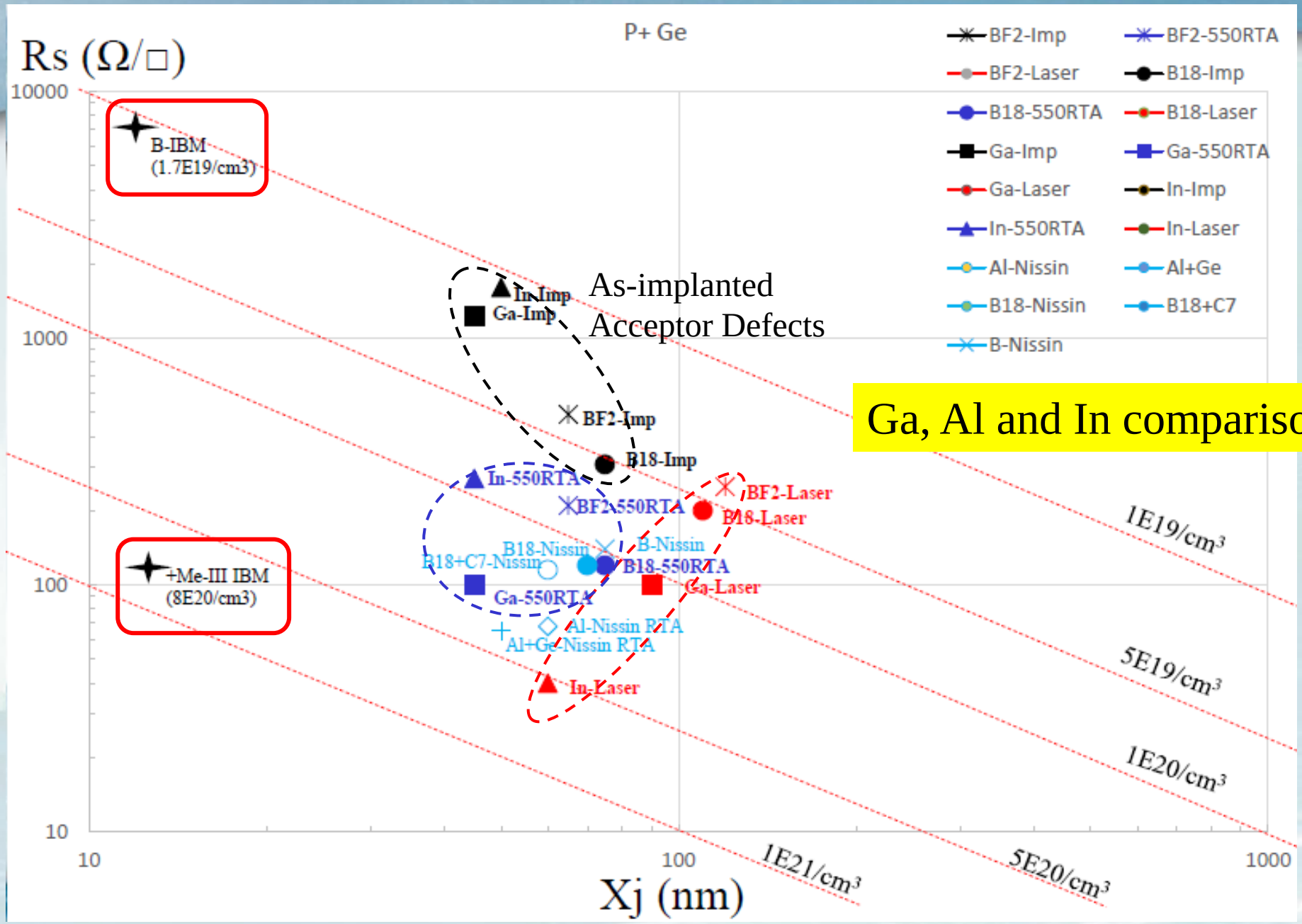


Fig.7 Partial re-growth of Si:P at 800C DB mSec LSA and full re-growth at 900C.

VLSI-2017



Ga, Al and In comparison in Ge

Ge: Trumbore, Bell Labs, 1959

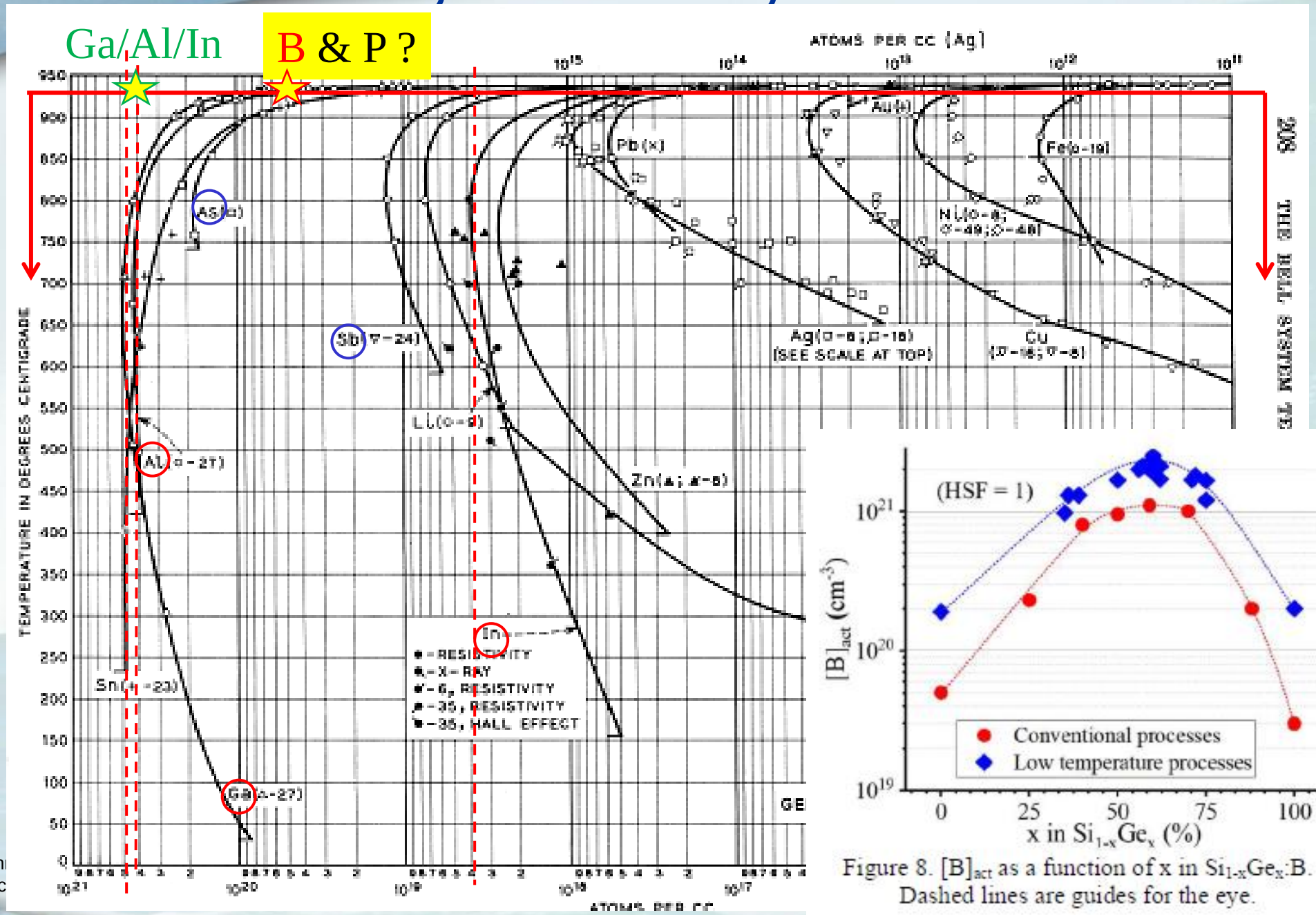
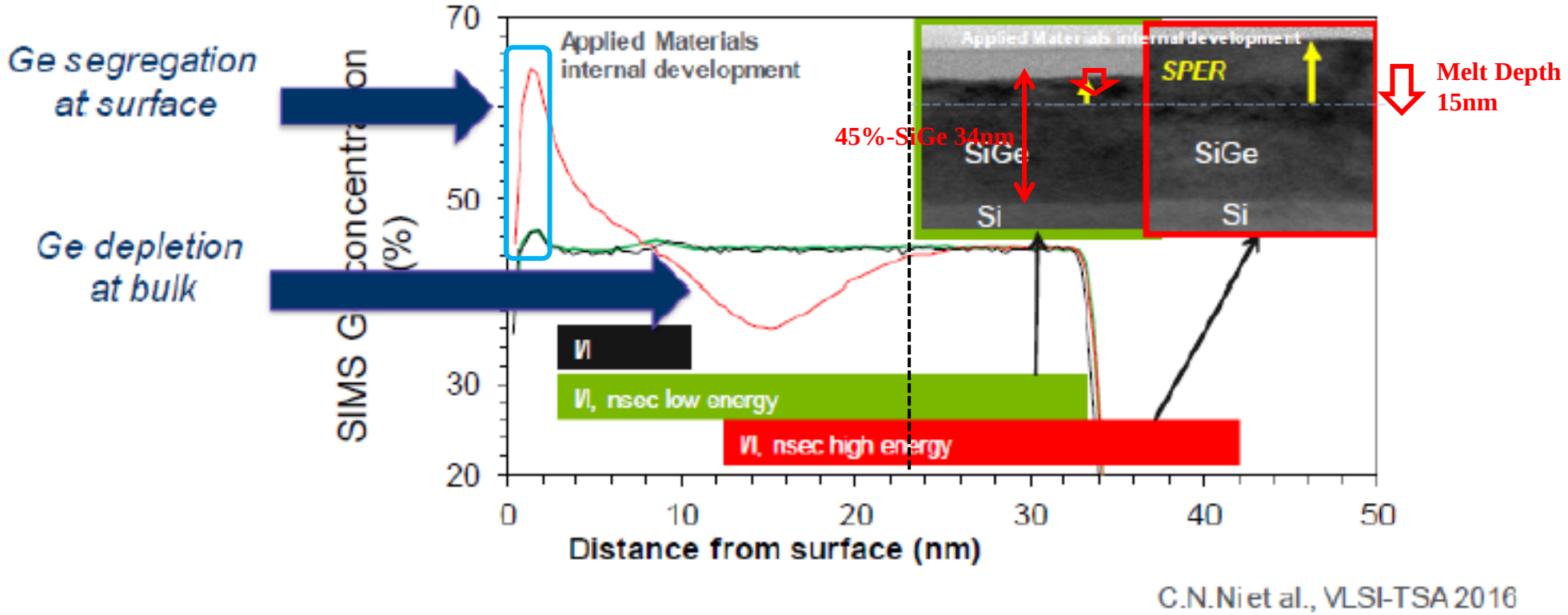


Figure 8. $[B]_{act}$ as a function of x in $Si_{1-x}Ge_x$:B. Dashed lines are guides for the eye.

Ge-rich Surface Formation by Nanosecond Laser Anneal



C.N.Ni et al., VLSI-TSA 2016

Ge is segregated towards SiGe surface with Implant + NLA

ECS Transactions, 86 (7) 29-39 (2018)
10.1149/08607.0029ecst ©The Electrochemical Society

ECS Oct-2018

Composition and Strain Evolution of Undoped $Si_{0.8}Ge_{0.2}$ Layers Submitted to UV-Nanosecond Laser Annealing

L. Dagault[a,b], P. Acosta-Alba[a], S. Kerdilès[a], J. P. Barnes[a], J. M. Hartmann[a], P. Gergaud[a], T. T. Nguyen[a], A. Grenier[a], J. Aubin[c] and F. Cristiano[b]

[a] Université Grenoble Alpes, CEA, LETI, 38000 Grenoble, France
[b] LAAS-CNRS, Université de Toulouse, UPS, 31031 Toulouse, France
[c] SCREEN-LASSE, 92230 Gennevilliers, France

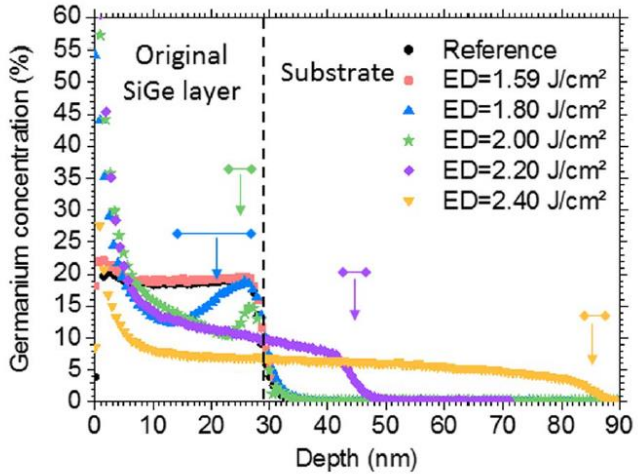


Figure 2. ToF-SIMS germanium atomic concentration depth profiles in samples annealed at laser energy densities ranging from 1.59 to 2.40 J/cm^2. Arrows indicate the melt depth for samples with partial or total melt of the initial SiGe layer.

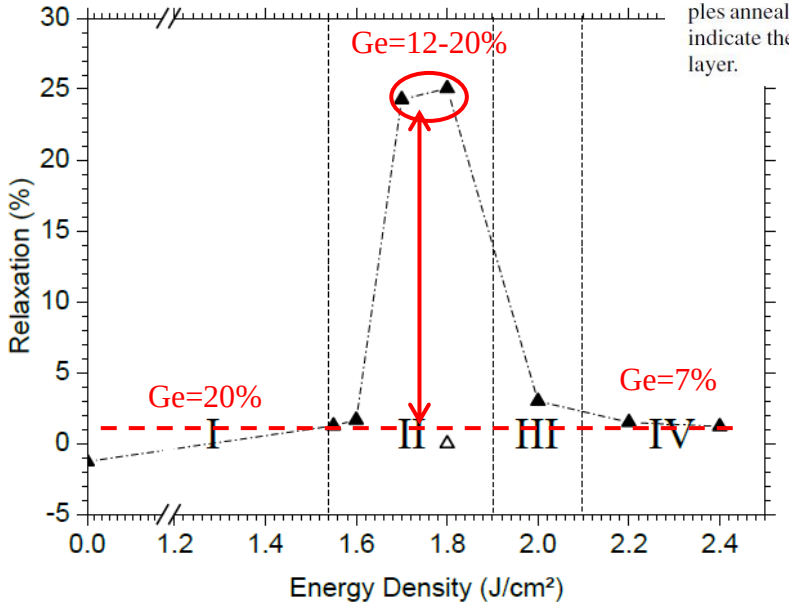
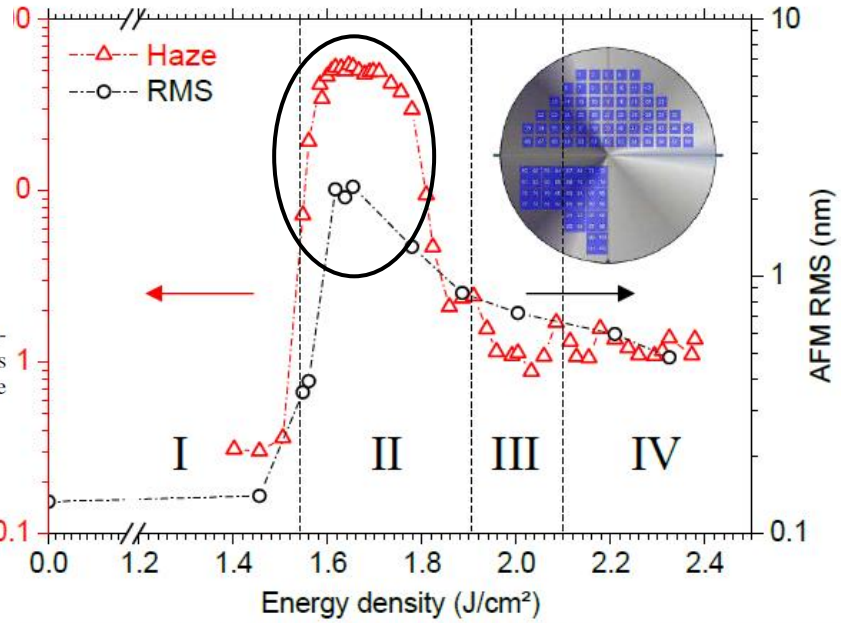


Figure 4. Evolution of the macroscopic degree of strain relaxation of initially 30 nm thick $Si_{0.8}Ge_{0.2}$ layers as a function of the energy density, calculated with data obtained from Figure 3 RSMs. An increase of the relaxation, up to 25%, is evidenced for samples annealed at 1.70 and 1.80 J/cm². The open symbol point at 1.80 J/cm² corresponds to the additional weak contribution observed in the associated (224) RSM. The dotted line is to be used only as a guide for the eyes.



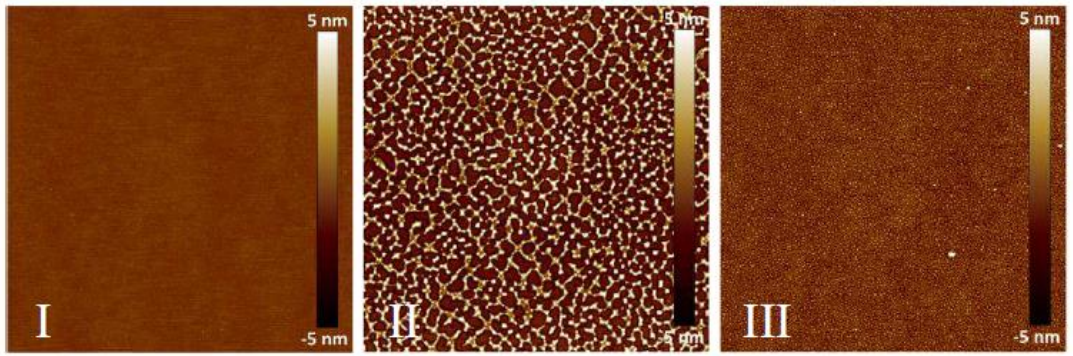


Figure 2. (a) Evolution of SP2 haze and AFM RMS roughness (10×10 µm² scans) of initially 30 nm thick $Si_{0.8}Ge_{0.2}$ layers, as functions of laser energy density. A strong increase of both roughness metrics occurs around 1.55 J/cm², corresponding to the melt threshold of the SiGe surface. (b) AFM images (10×10 µm²) corresponding to samples annealed at 1.42 (regime I), 1.65 (regime II) and 2.00 J/cm² (regime III).

IIT-2022, TU3.03 paper

Time Resolved Reflectometry with Pulsed Laser Melting of Implant Amorphized $Si_{1-x}Ge_x$

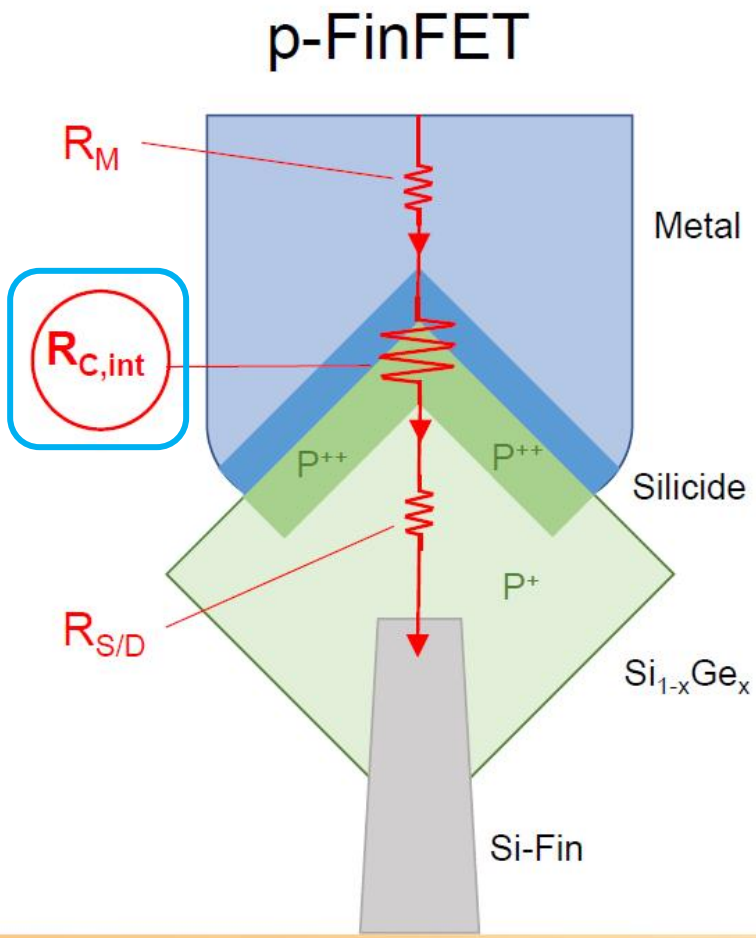
Jesse A. Johnson II [4], Xuebin Li [2], Chris Hatem [3], David Brown [1], Bruce Adams [2], **Kevin S. Jones** [1];

[1] University of Florida, Gainesville, Florida, [2] Applied Materials, Santa Clara, California; [3] Applied Materials – Varian Semiconductor Equipment, Gloucester, Massachusetts, [4] Mainstream Engineering, Rockledge FL

Reducing ρ_c for pMOS

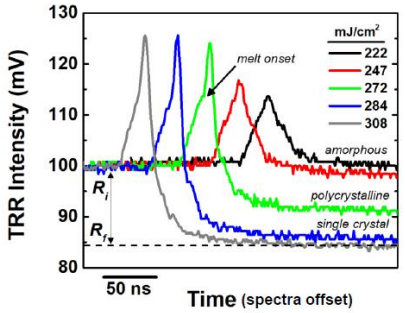
- At S/D metal interface need:
  - High Active Dopant Concentration (N_A)
  - Minimal Defects / Lateral Uniformity (Φ_B)
  - Biaxial-strained SiGe S/D (Φ_B, m^*)
  - Increased [Ge] at S/D-contact interface (Φ_B)

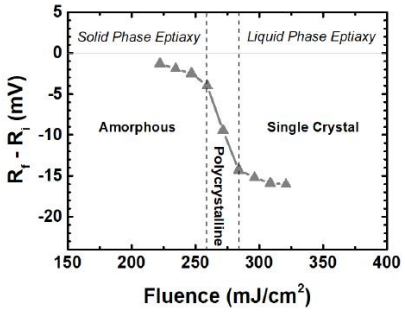
How do we accomplish this?



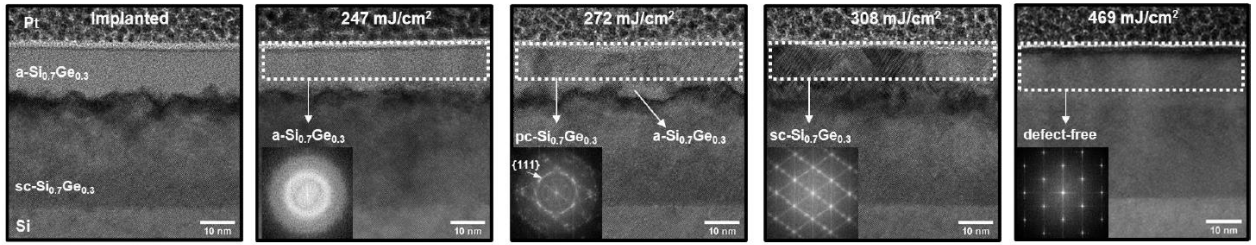
J.O.B. Technolo
Sales & Techno

Sub-melt to Threshold for Liquid Phase Epitaxy

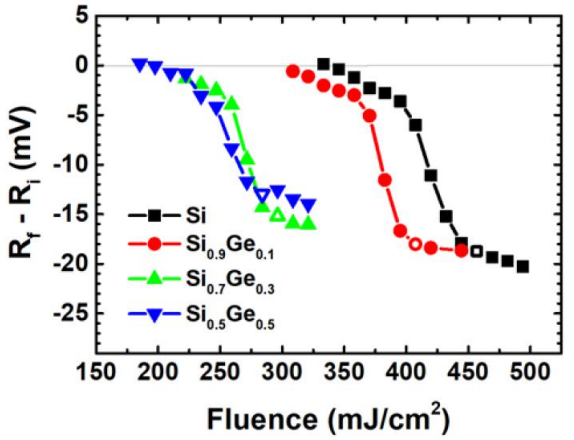




- $Si_{0.7}Ge_{0.3}$
- Ge^+ implants,10 keV, 1.4 x 10^{14} cm^{-2}
- Inflection points in ΔR plot correlate with solidification regimes
- In-situ method of generating S curve for the first time



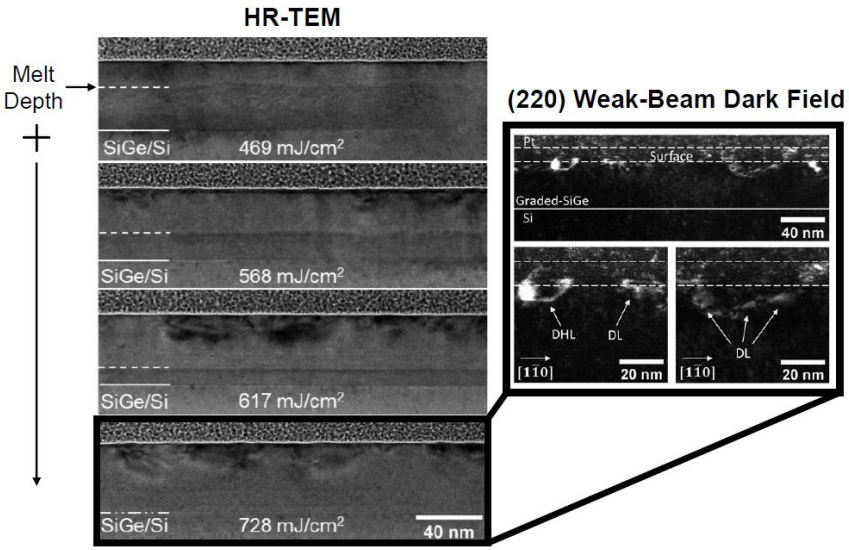
Reflectivity and Absorption Response to Alloy Concentration



- Si_xGe_{1-x} alloys x = 1 to 0.5
- Implanted Ge^+ 10 keV, 1.4 x 10^{14} cm^{-2} RT
- Single pulse laser anneal at varying powers
- TRR measurements
- Study S curve response as Ge concentration increases
- Phase boundaries resolved up to 50% Ge
- Profile shift is a function of alloy T_m and pulsed laser absorption
- At 50% Ge the power to melt stops decreasing due to decreased laser absorption
- **ΔR plot allows for estimation of fluence threshold for amorphous layer melt evolution**

J. Johnson et al. Applied Surface Science Volume 564, 2021, 150408

Influence of Melt Depth on Liquid Phase Epitaxial Regrowth of $Si_{0.7}Ge_{0.3}$



Johnson et al, Appl. Surf. Sci. **564**, (2021)

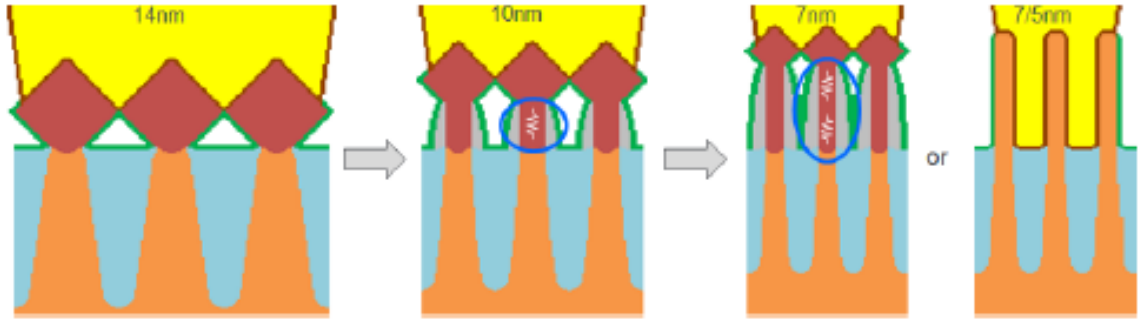
- $Si_{0.7}Ge_{0.3}$
- Melt to different depths
- Regrows defect free then breaks down (Bilayer formation)
- Surface irregularities for melt depths > 22nm
- STEM-EDS shows evidence of lateral Ge segregation
- (220) WBDF shows dislocation half loops terminating at surface

Activation Engineering is needed

- Low epi resistivity is needed to drive $R_{S/D}$ down and drive ρ_c down.

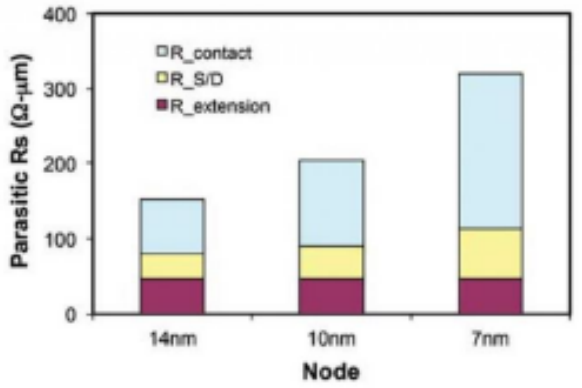
$$R_{S/D} \propto \rho \qquad \rho_c \propto e^{q\times\varphi_B/\sqrt{N_a}}$$

- Solution to both is to engineer materials with better electrical performance
- The approach industry is looking at is to increase N_a - but adequate feedback is lacking.



"Fin pitch scaling with each CMOS node reduces contact area and drives up Rc, while narrower and taller fins result in increase in RSD"

F.A Khaja, "Contact Resistance Improvement for Advanced Logic by Integration of Epi, Implant and Anneal Innovations", Volume 4, Issue 48 (Electronics and Photonics) 2019 , pp. 2559-2576.



https://sst.semiconductor-digest.com/2014/12/laser-spike-annealing-resolves-sub-20nm-logic-device-manufacturing-challenges/

Pg. 7

Active Layer Parametrics
Electrical Characterization at Atomic-Level Resolution

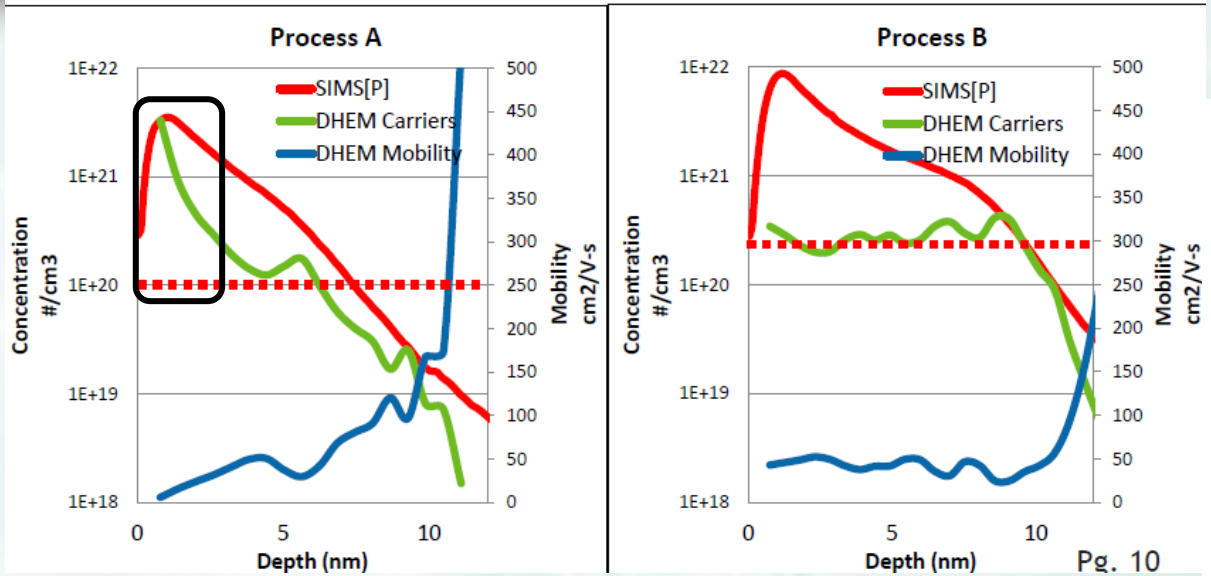
Measuring Activation Depth Profiles in very Highly Doped Ultra-Thin Semiconductors at Sub-nm Depth Resolution

AJ Joshi (ALP Inc.)
ajoshi@alpinc.net

Ion Implantation Technology 2022
28th Sept 2022

Sub-nm Carrier Concentration Profiles

- In reality, Process A has higher activation in the near-surface than Process B.
- Bulk data cannot capture *near-surface activation* which is crucial for good contacts.



J.O.B. Technologies (Strategic Marketing, Sales & Technology)

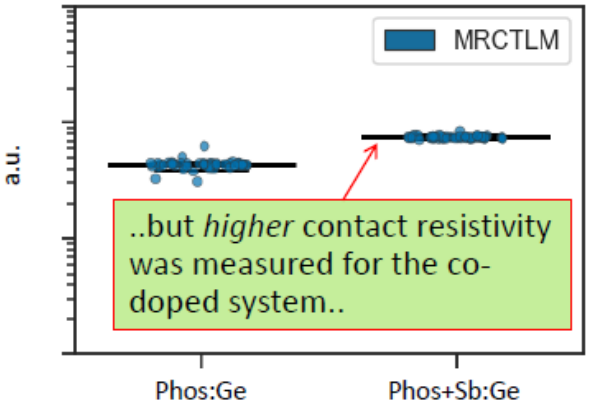
Near-Surface Activation Engineering for Better n-Ge Contacts

- Near-surface activation has an oversized impact on contact resistivity, so understanding the effects of process on near-surface activation is crucial.

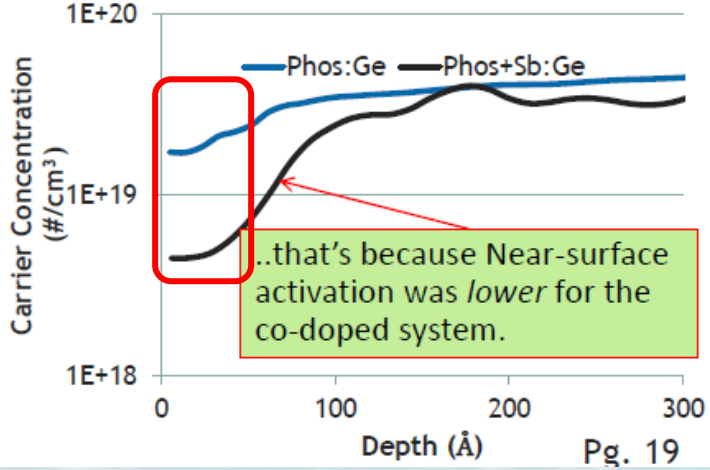
Sample	Rs (Ω/□)	μ (cm2/V-s)	*Active Dose* (#/cm2)
Phos:Ge	39.9	270.1	*5.8e14*
Phos+Sb:Ge	38.5	246.3	*6.6e14*

+14% in activation w/ co-doping..

Ge Contacts Summary: Specific Contact Resistivity



ALPro™ Activation profiles

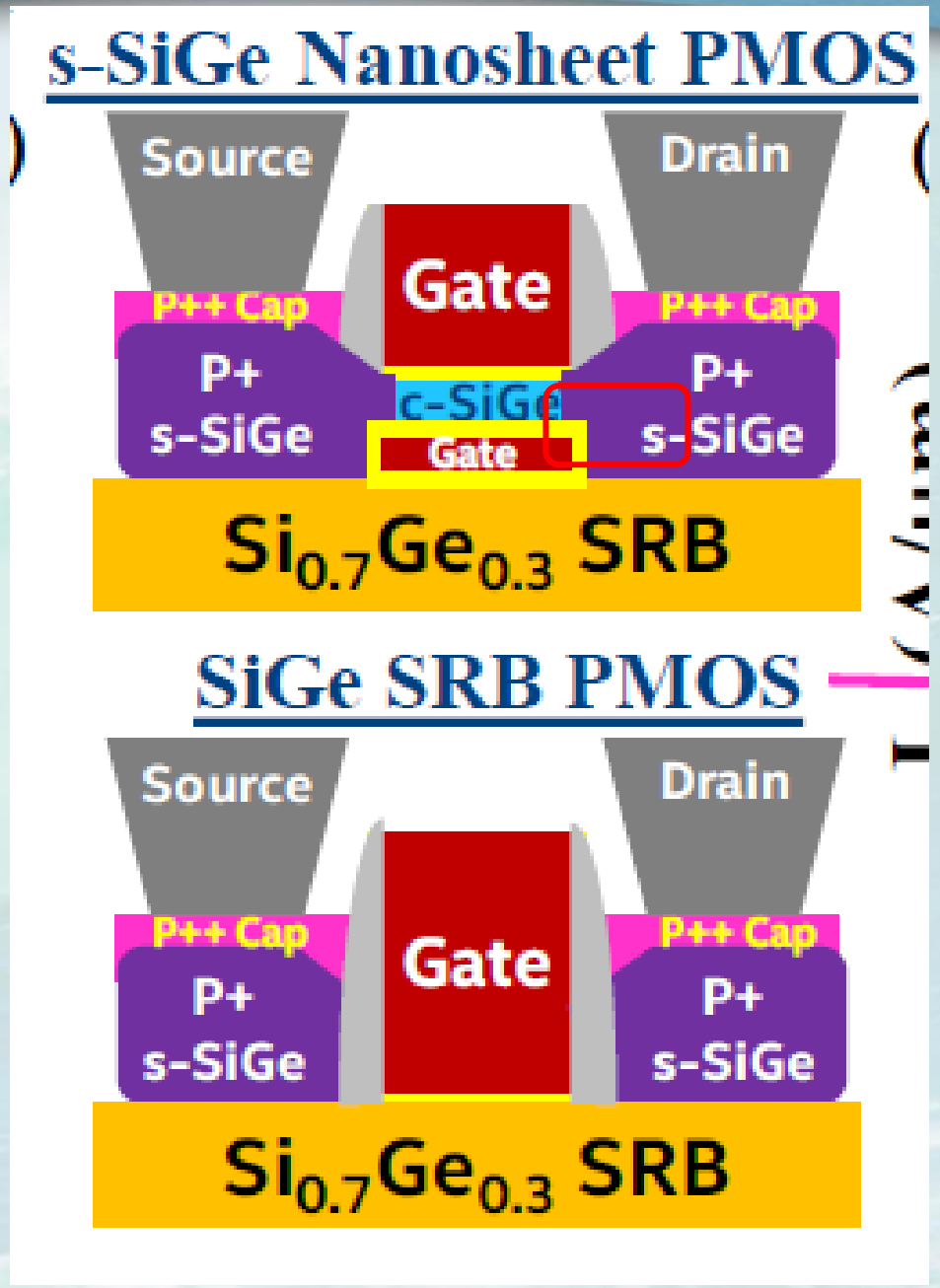


Gate-All-Around Strained $Si_{0.4}Ge_{0.6}$ Nanosheet PMOS on Strain Relaxed Buffer for High Performance Low Power Logic Application

A.Agrawal[1], S. Chouksey[1], W. Rachmady[1], S. Vishwanath[2], S. Ghose[2], M. Mehta[2], J. Torres[1], A.A. Oni[2], X. Weng[2], H. Li[2], D. Merrill[2], M. Metz[1], A. Murthy[2] and J. Kavalieros[1]
[1]Components Research, Intel Corporation, Hillsboro, OR 97124, USA
[2]Portland Technology Development, Intel Corporation, Hillsboro, OR 97124, USA
Contact: E-mail ashish1.agrawal@intel.com

IEDM-20 paper 2.2

Abstract— For the first time, we report a short channel high performance, gate-all-around strained $Si_{0.4}Ge_{0.6}$ nanosheet PMOSFET with aggressively scaled dimensions. We demonstrate realization of s-$Si_{0.4}Ge_{0.6}$ nanosheet with 5nm thickness and device with L_G=25nm featuring record high I_{ON}=508 µA/µm at I_{OFF}=100nA/µm and V_{DS}= -0.5V. This result is obtained with the combination of (a) novel Si-cap-free gate oxide solution featuring thin EOT=9.1A, low D_{IT} and N_{IT} for s-$Si_{0.4}Ge_{0.6}$ channel, (b) record high hole mobility= 450 cm^2/Vs owing to compressive strain imparted by $Si_{0.7}Ge_{0.3}$ strain relaxed buffer (SRB), (c) low R_{EXT}=150 Ω-µm due to highly active, strained source/drain SiGe process and novel p++ cap layer, (d) optimized source/drain tip and junction to minimize GIDL impact to I_{OFF}. Additionally, the impact of operating temperature on GIDL and I_{OFF} is comprehensively studied to prescribe optimal V_{CC} range of operation for this technology.



Laser Annealing Applications For Advanced FinFETs and Beyond

Oleg Gluschenkov, IBM Research, IIT-2022 Sept-2022, TU1.01 paper

Nano-Sheets and 3-D Stacked Nano-sheets/FinFETs require lower External Resistance (Contact Resistance) more critical than transistor!

Planar	**FinFET**	**Nano-sheet**	**3-D Stacking**
Wc/Wg ~1	Wc/Wg ~1/3	Wc/Wg ~1/6	
Rext/Rch <1	Rext/Rch ~1	Rext/Rch ~3	Rext/Rch ~3

Strain/Lattice Characterization of Si+Ge, SiGe+Ge, SiGe+C, Ge+C, Ge+Sn & Si+Ge+Sn Surface Layers Formed By Implantation With RTA or Laser Annealing Using SIMS, XPS, TEM-EDX, XRD and Raman Analysis

IIT-2022 September 29, 2022

John Borland, J.O.B. Technologies, Aiea, HI, USA

Shota Komago, Ryo Yokogawa, Kazutoshi Yoshioka, Naomi Sawamoto and Atsushi Ogura, Meiji University, Kawasaki, Japan

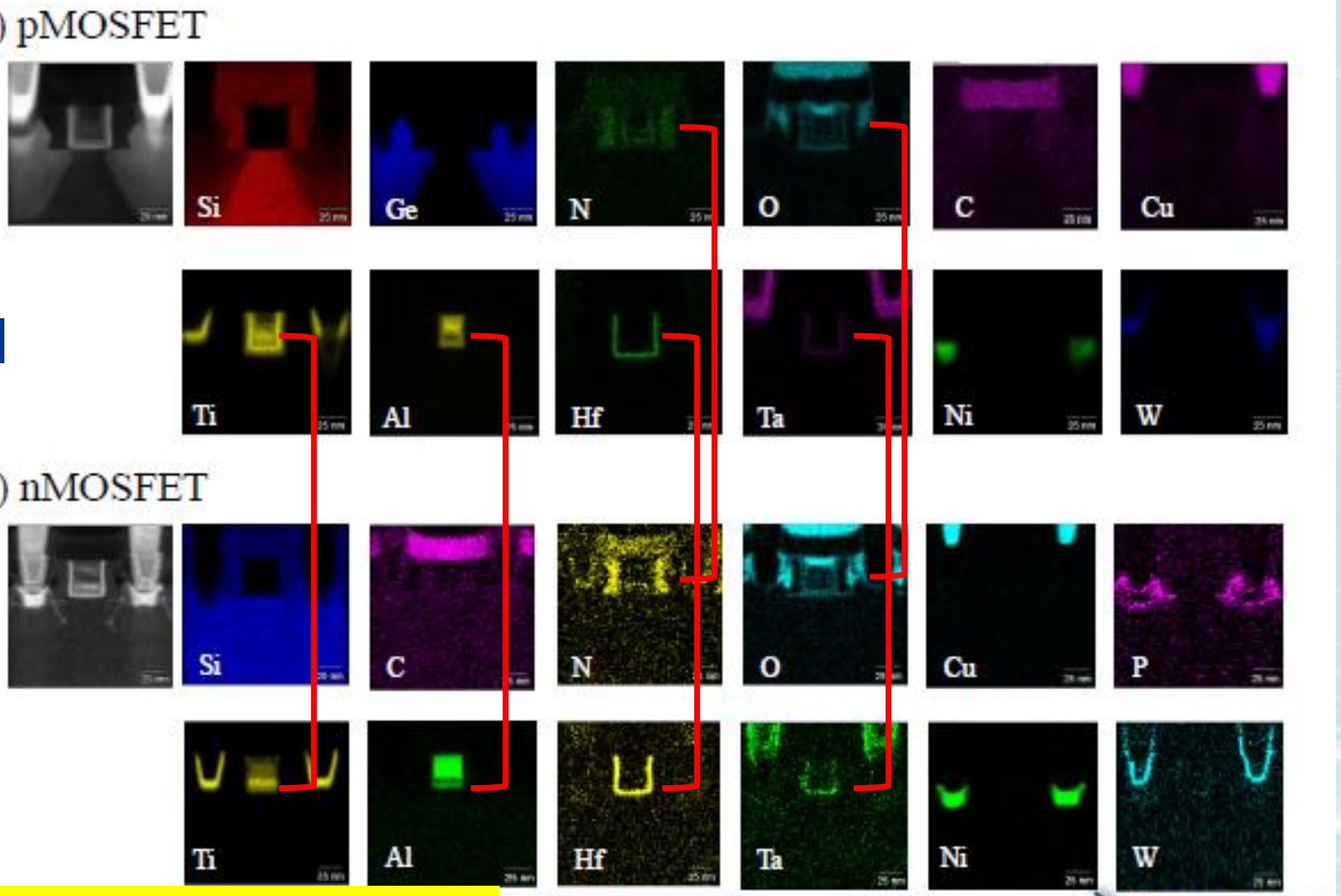
Gary Goodman, Nadya Khapochkina and Temel Buyuklimanli, EAG, Sunnyvale, CA, USA

Outline

At IEDM-2022 Tuesday EDS Panel on Materials for Electronic Devices:
Think Crazy Ideas for University Material Research!

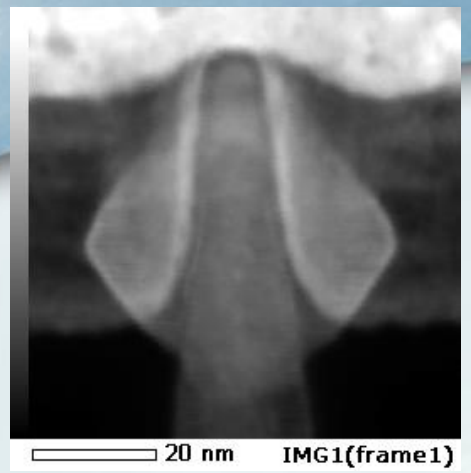
- Introduction: Lattice Constant Engineering to Replace Epi Buffer Layer (Power Devices or III-V Solar) or Boost p+SiGe /n+Si Contact Resistance.
  - Chemical: SIMS → XPS → TEM-EDX for 2-D mapping
  - Strain: XRD → Raman
- Experimentation:
  - Substrate Wafer: Si-Cz wafers, SiGe-Epi, Ge-Cz wafers and Ge-Epi
  - Ion Implantation (Ge, Sn & Ge+Sn)
  - Anneals (RTA or Laser-melt)
- Results:
  - Chemical Analysis: SIMS, XPS and TEM-EDX
  - Strain: XRD and Raman
- Summary/Conclusion:
- Acknowledgements

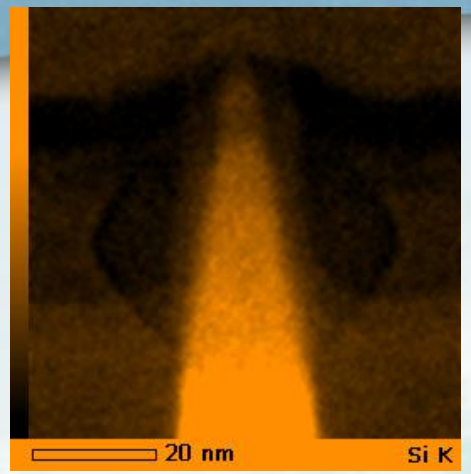
TEM-EDX For 3-D Chemical Mapping

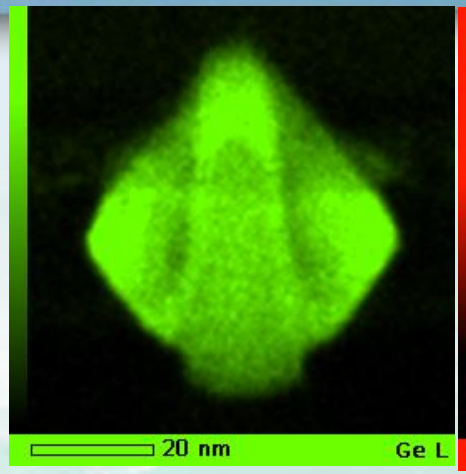


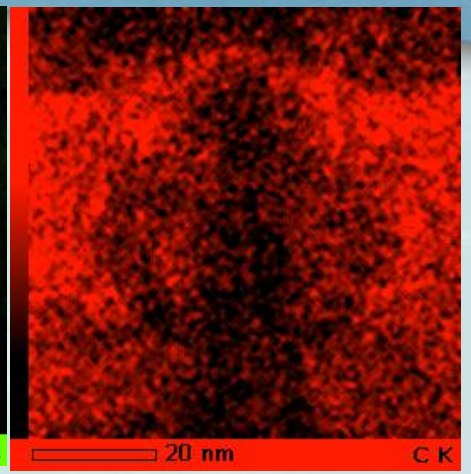
Meiji Univ. July -2012, Intel 32nm Planar

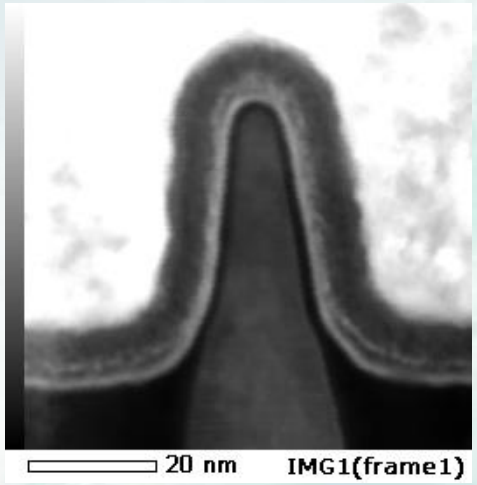
X-TEM With EDX

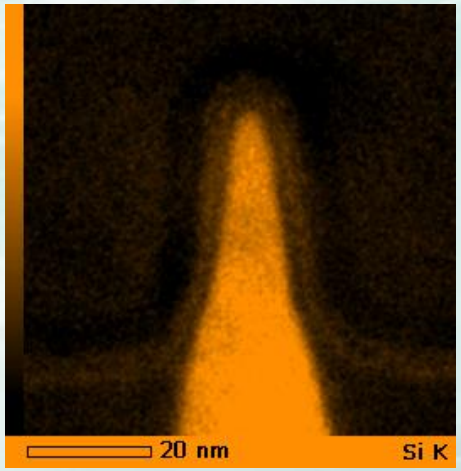


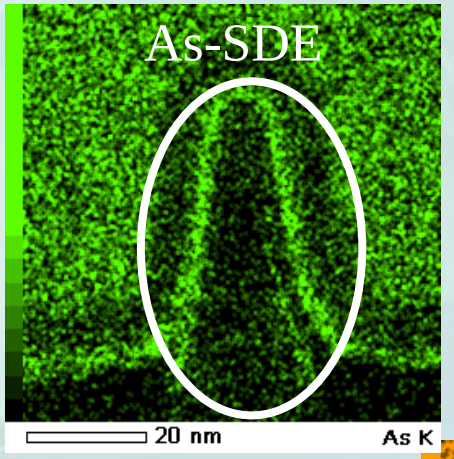


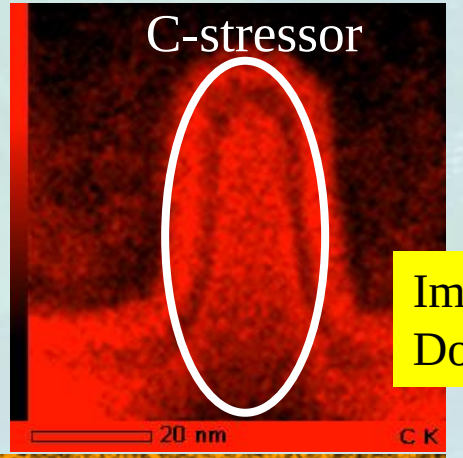








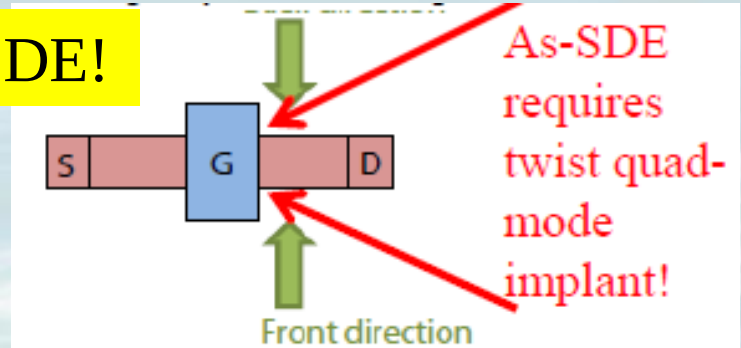


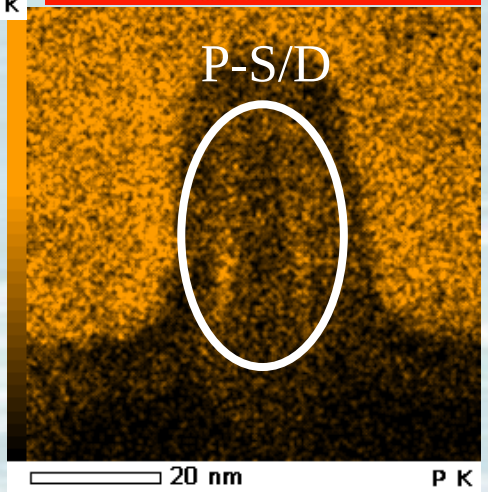


Implant Strain & Doping Critical!

Prof. Ogura, Meiji Univ. 3/1/16

Reveals FinFET As n+S/D and P nSDE!





ECS Transactions, 50 (9) 47-58 (2012)
©The Electrochemical Society

Stress techniques and mobility enhancement in FinFET architectures

G. Eneman, L. Witters, J. Mitard, G. Hellings[1], A. De Keersgieter, D.P. Brunco[2], A Hikavyy, B. Vincent, E. Simoen, P. Favia, H. Bender, A. Veloso, T. Chiarella, G. Boccardi, M. Kim, M. Togo, R. Loo, K. De Meyer[1], N. Horiguchi, N. Collaert, A. Thean

Imec, Kapeldreef 75, 3001 Leuven, Belgium
[1] ESAT-INSYS department, Katholieke Universiteit Leuven, 3001 Leuven, Belgium
[2] GLOBALFOUNDRIES assignee at imec, 3001 Leuven, Belgium

On n-FinFETs, tensile stressed Contact Etch-Stop Layers (t-CESL) are less effective than on planar FETs when a gate-first scheme is used. For gate-last schemes, CESL is as effective as on planar FETs, moreover a strong boost is expected when compared to gate-first schemes. CESL becomes very ineffective for layouts with narrow fin pitches with merged fins: about 3 times lower mobility increase is predicted than for isolated fins.

Tensile stressed gates are shown to be an effective stressor on gate-first n-FinFETs, but not on gate-last: in the latter case a slight mobility degradation is predicted.

Si:C source/drain stressors are very effective and show similar width dependence as on planar FETs. Significant mobility enhancement is predicted both in isolated and tight-pitch/merged fin configurations.

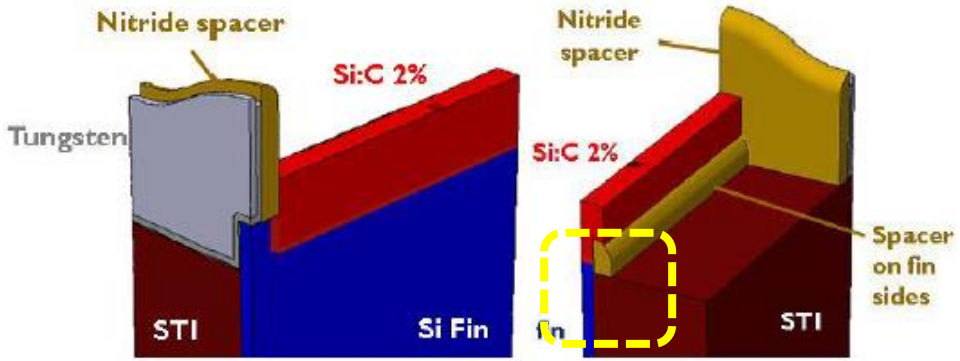


Figure 9. (Left) front and (right) backside view of an isolated fin with Si:C (2% C) source/drain. The 30 nm-high Si fin is first recessed by 25 nm, and regrown by 50 nm of Si:C. Spacers are left at the sides of the fin.

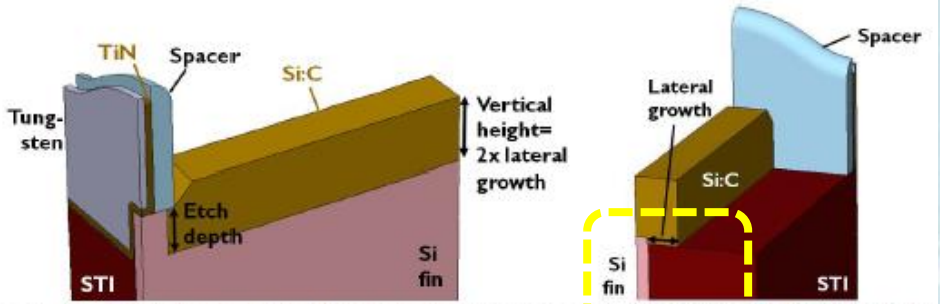


Figure 12. (Left) front and (right) backside view of an isolated fin with Si:C (2% C) source/drain. A 2:1 Si:C growth anisotropy is assumed, i.e. the vertical thickness of the Si:C is twice the thickness deposited on the fin sides. Spacers are removed from the fin sidewalls.

July 2012 Synopsys visit said best FinFET results when Fin is completely doped uniformly to 2E18/cm3 and NO extension. Also said from simulations the only way Intel gets the nMOS device performance is to use eSiC epi grown in confined etched out Fin structure with sidewall spacer in place! See ECS-2012 IMEC paper.

July 2014 WCJUG seminar Victor admitted to me his simulations were WRONG 2 years ago!

(12) **United States Patent**
Borland et al.

(10) **Patent No.: US 7,259,036 B2**
(45) **Date of Patent: Aug. 21, 2007**

(54) **METHODS OF FORMING DOPED AND UN-DOPED STRAINED SEMICONDUCTOR MATERIALS AND SEMICONDUCTOR FILMS BY GAS-CLUSTER-ION-BEAM IRRADIATION AND MATERIALS AND FILM PRODUCTS**

(75) Inventors: **John O. Borland**, South Hamilton, MA (US); **John J. Hautala**, Beverly, MA (US); **Wesley J. Skinner**, Andover, MA (US); **Martin D. Tabat**, Nashua, NH (US)

(73) Assignee: **TEL Epion Inc.**, Billerica, MA (US)

(58) **Field of Classification Search** 438/36, 438/37, 45, 87, 473, 474, 795; 427/562, 427/585
See application file for complete search history.

(56) **References Cited**

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2002/0036261	A1	3/2002	Dykstra	250/287
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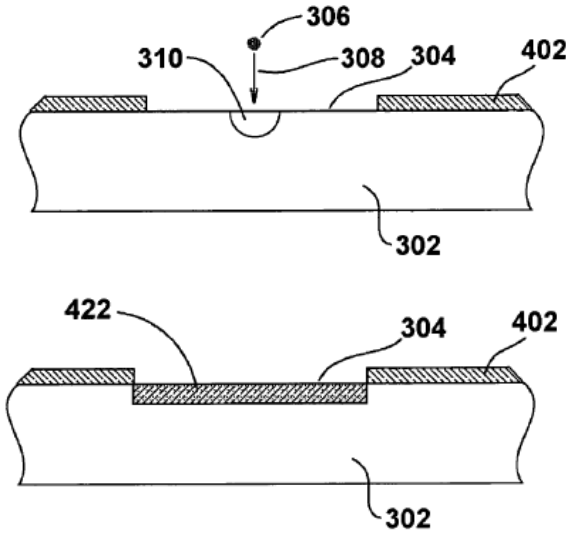
2003/0109092	A1	6/2003	Choi et al.	438/200

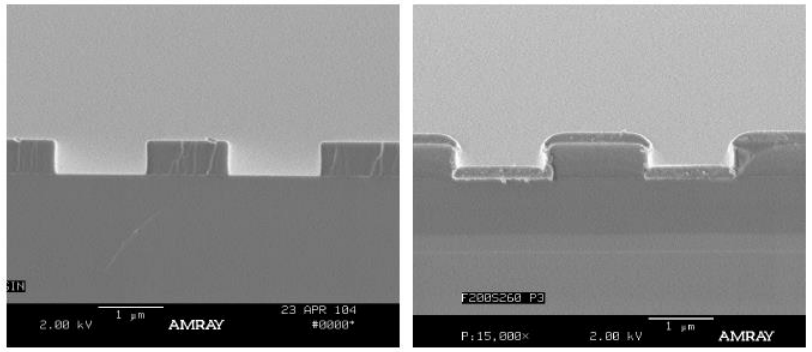
(57) **ABSTRACT**

Methods and apparatus are described for irradiating one or more substrate surfaces with accelerated gas clusters including strain-inducing atoms for blanket and/or localized introduction of such atoms into semiconductor substrates, with additional, optional introduction of dopant atoms and/or C. Processes for forming semiconductor films infused into and/or deposited onto the surfaces of semiconductor and/or dielectric substrates are also described. Such films may be doped and/or strained as well.



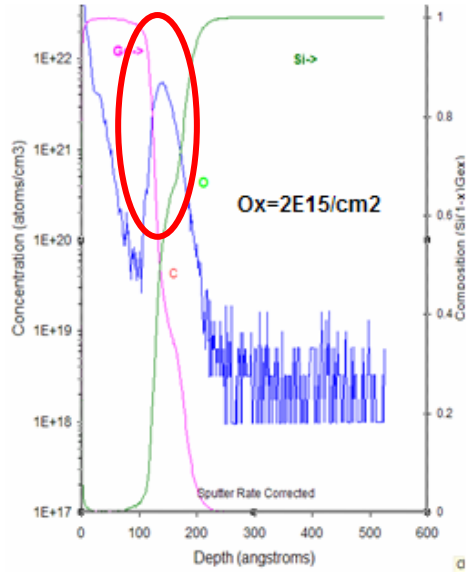
Room Temperature Processing : PR compatible

200nm Ge Infusion Deposition On Photo Resist

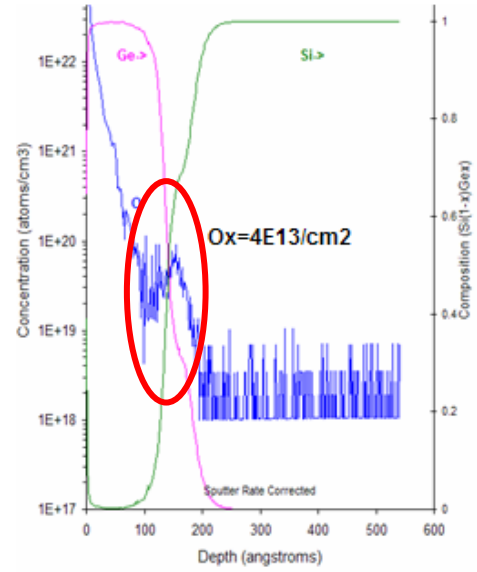


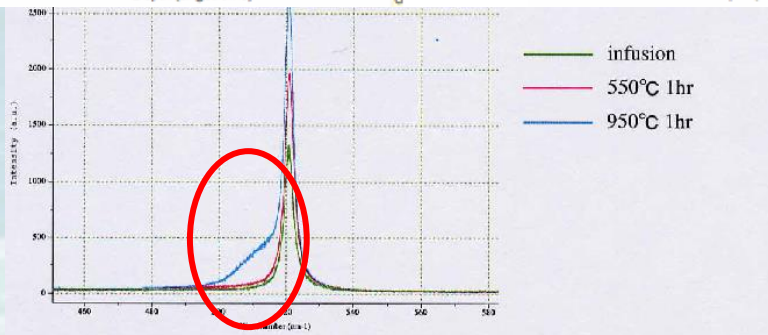
epion corporation

No Surface Cleaning



HF-Dip Surface Cleaning





infusion後と550℃アニール後ではSi層以外からの信号は検出されない。
950℃では、SiGe層からの信号有るが非常にブロード（濃度分布？）。

Also used PR for localized/selective deposition

Borland et al., ECS Oct 2004

(57) **ABSTRACT**

A method of making a semiconductor device patterns a first fin in a pFET region, and patterns a second fin in an nFET region. A plurality of conformal microlayers containing a straining material are deposited on the first and second fins. A protective cap material is formed on the first fin, and the conformal layers are selectively removed from the second fin. The straining material is then thermally diffused into the first fin. The protective cap material is removed from the first fin after the thermal annealing and after the conformal micro layers are selectively removed from the second fin.

(12) **United States Patent**
Berliner et al.

(10) **Patent No.: US 8,900,973 B2**
(45) **Date of Patent: Dec. 2, 2014**

(54) **METHOD TO ENABLE COMPRESSIVELY STRAINED PFET CHANNEL IN A FINFET STRUCTURE BY IMPLANT AND THERMAL DIFFUSION**

(75) Inventors: **Nathaniel C. Berliner**, Albany, NY (US); **Pranita Kulkarni**, Slingerlands, NY (US); **Nicolas Loubet**, Albany, NY (US); **Kingsuk Maitra**, Guilderland, NY (US); **Sanjay C. Mehta**, Niskayuna, NY (US); **Paul A. Ronsheim**, Hopewell Junction, NY (US); **Toyoji Yamamoto**, Yokohama (JP); **Zhengmao Zhu**, Pougkeepsie, NY (US)

Assignees: **International Business Machines Corporation**, Armonk, NY (US); **Globalfoundries Inc.**, Santa Clara, CA (US); **Renesas Electronics America Inc.**, Santa Clara, CA (US); **STMicroelectronics, Inc.**, Coppell, TX (US)

(58) **Field of Classification Search**
CPC H01L 21/845; H01L 27/1211; H01L 29/7848
USPC 438/468
IPC H01L 21/845, 27/1211, 29/7848
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,728,619 A 3/1988 Pfiester et al.
7,759,175 B2 7/2010 Clavelier et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP 1 833 094 A1 9/2007

OTHER PUBLICATIONS

Tezuka, et al., "Strain analysis in ultrathin SiGe-on-Insulator layers formed from strained Si-on-Insulator substrates by Ge-condensation process," Applied Physics Letters 90, 181918, 2007, pp. 90, 181918-

Blanket/conformal deposition then selective removal

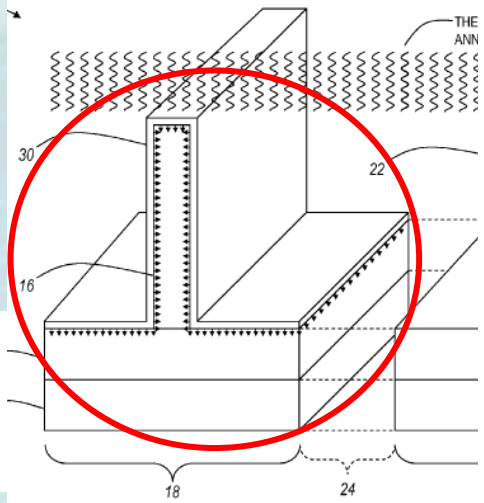
extension and source/drain regions. A process referred to herein as Plasma Doping (PD) can be used as one method for the deposition/implantation of the Ge layers. PD uses plasma to generate active radicals of species to be deposited. For Germanium, PD uses GeH4 precursor. PD can be operated both in the implant mode as well as un-biased deposition mode (to minimize damage to substrate). The methods described herein are not limited to the FinFET or TriGATE geometries, but also extend to the fully depleted planar extremely thin silicon-on-insulator (ETSOI) devices where the operation in the implant mode can cause irreparable damage to the thin substrate, potentially amorphizing the entire substrate.

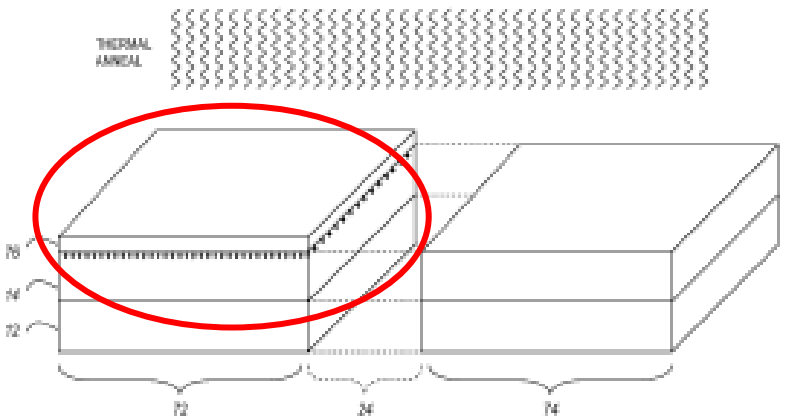
2. The method of making a semiconductor device according to claim 1, said conformal layers comprising several monolayers of conformal material.

3. The method of making a semiconductor device according to claim 1, said bias charge comprising a bias below 3 kV.

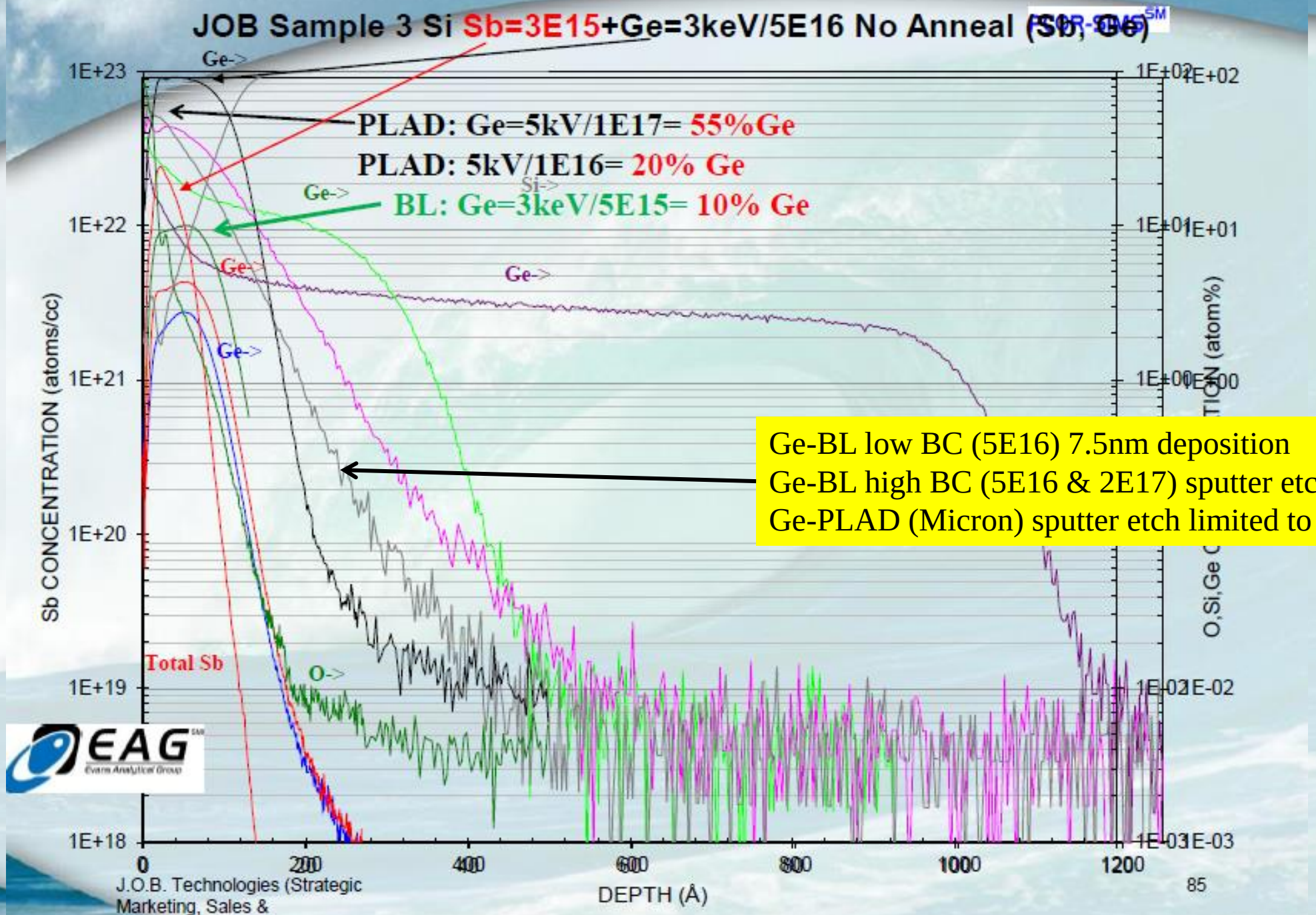
plasma doping an impurity layer on said first FinFET said nFET

The straining material imparts a compressive strain to the surface Si channel of the first FinFET device and converts a portion of the surface Si of the fin into an alloy of silicon. By introducing Ge in the channel by Ge diffusion in pFET fins prior to the gate patterning, this processing lowers the threshold voltage and enhances carrier mobility. The straining material may comprise, for example, Germanium or Carbon.





16 is a schematic diagram illustrating the selective removal of the monolayers **76** from the nFET region **74** such that the monolayers **76** remain on the pFET region **72** of the planar device **70**. This selective removal of the layer **76** is accom-



Ge-BL low BC (5E16) 7.5nm deposition
Ge-BL high BC (5E16 & 2E17) sputter etch limited to 80%
Ge-PLAD (Micron) sputter etch limited to 55%

J.O.B. Technologies (Strategic Marketing, Sales & Technology)

85

Borland et al., IWJT-2013, paper S4-4, p.49

Borland et al., ECS Oct 2014, paper P7-1771

Outline

- Introduction: Strain Characterization
  - Chemical: SIMS → XPS → TEM-EDX
  - Strain: XRD → Raman
- Experimentation:
  - Substrate Wafers: Si-Cz wafers from Renesas, 45% SiGe-Epi from IMEC, Ge-Epi from NDL (Taiwan) and Ge-Cz from SMIT
  - Ion Implantation (Ge, Sn, Ge+Sn, Si & C) by Nissin and SMIT
  - Anneals (RTA by Meiji and Laser Anneal by LASSE-Screen)
- Results:
  - Chemical Analysis: XPS and TEM-EDX
  - Strain: XRD and Raman
- Summary/Conclusion:
- Acknowledgements

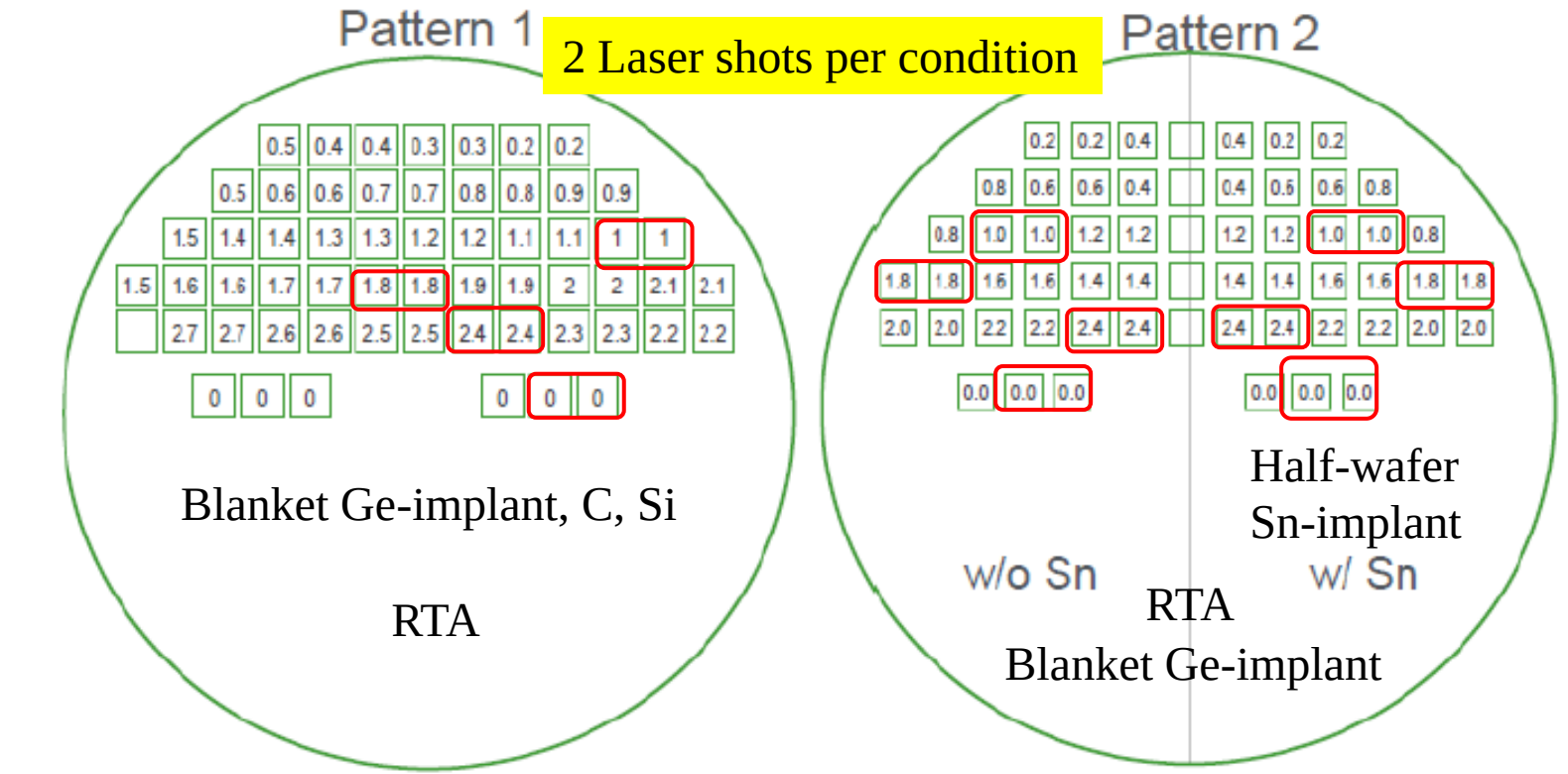
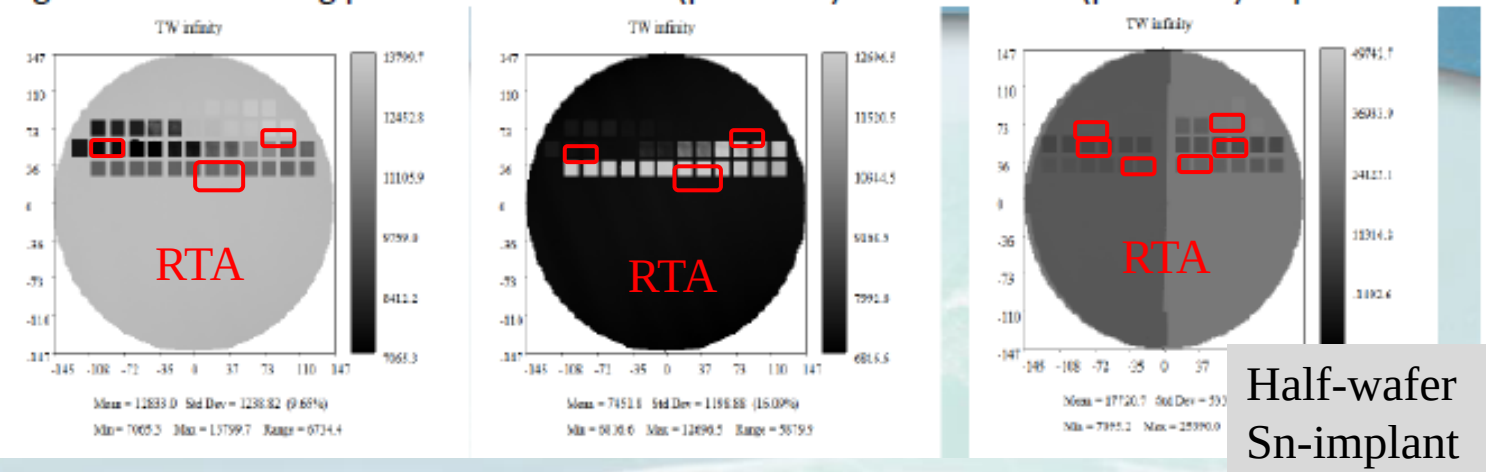
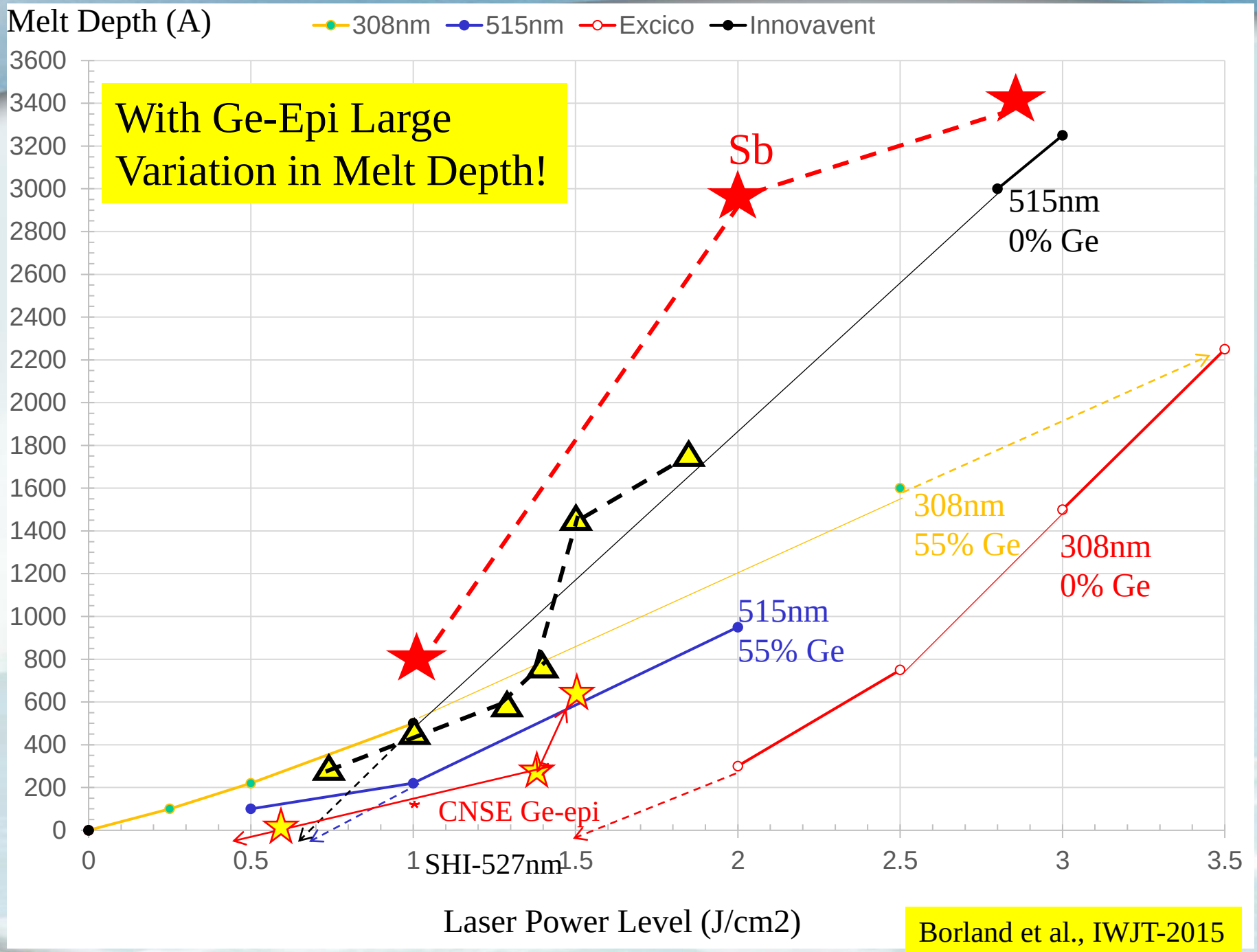


Fig.1: Laser annealing pattern for full wafer (pattern 1) and half wafer (pattern 2) implants.



Therma-wave Analysis

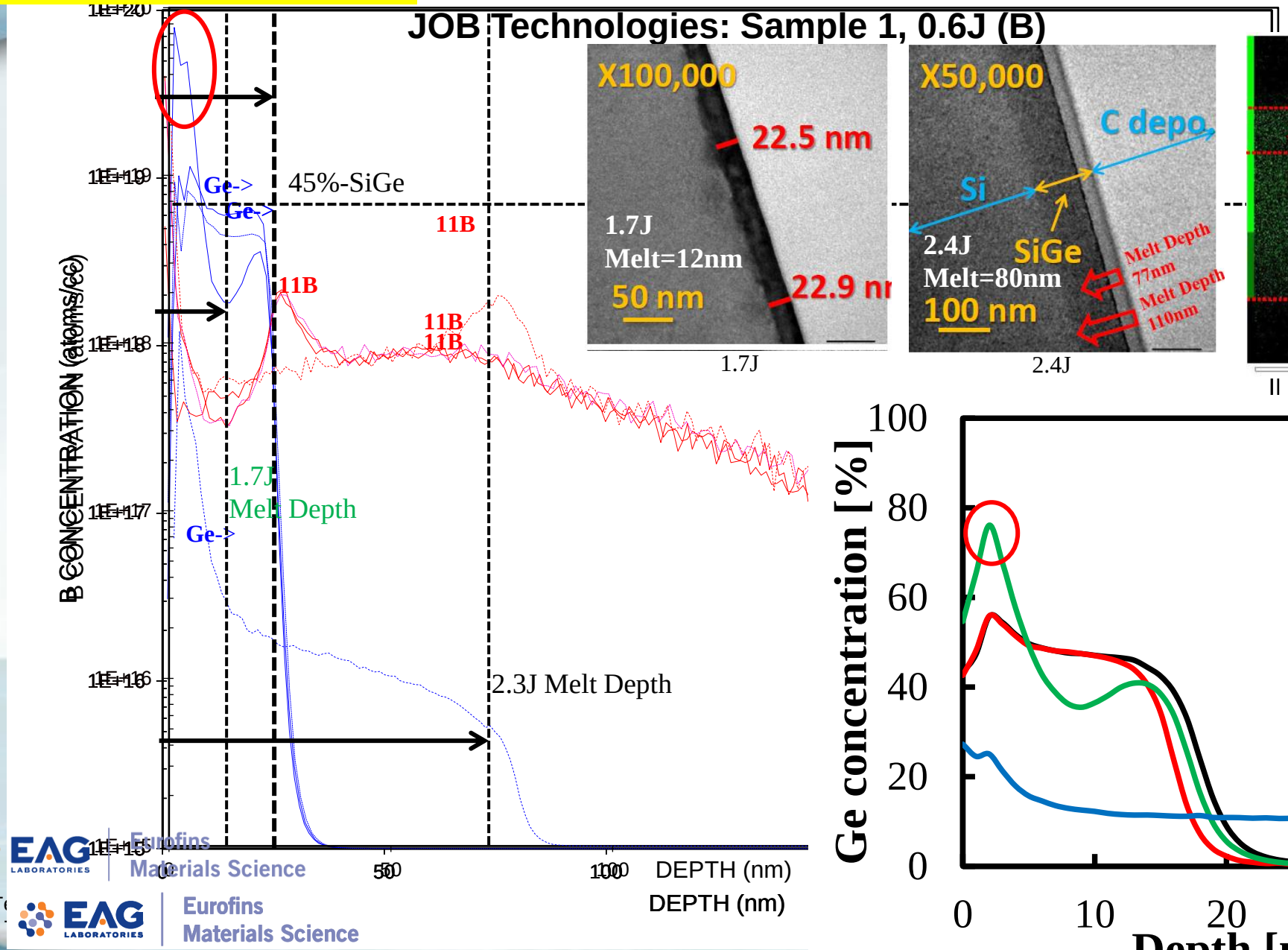

Melt Depth (A)
308nm
515nm
Excico
Innovavent
With Ge-Epi Large Variation in Melt Depth!
Sb
515nm
0% Ge
308nm
55% Ge
308nm
0% Ge
515nm
55% Ge
CNSE Ge-epi
SHI-527nm
Laser Power Level (J/cm2)
Borland et al., IWJT-2015

Outline

- Introduction: Strain Characterization
  - Chemical: SIMS → XPS → TEM-EDX
  - Strain: XRD → Raman
- Experimentation:
  - Substrate Wafer: Si-Cz wafers, SiGe-Epi, Ge-Cz wafers and Ge-Epi
  - Ion Implantation (Ge, Sn & Ge+Sn)
  - Anneals (RTA or Laser-melt)
- Results:
  - Chemical Analysis: SIMS, XPS and TEM-EDX
  - Strain: XRD and Raman
- Summary/Conclusion:
- Acknowledgements

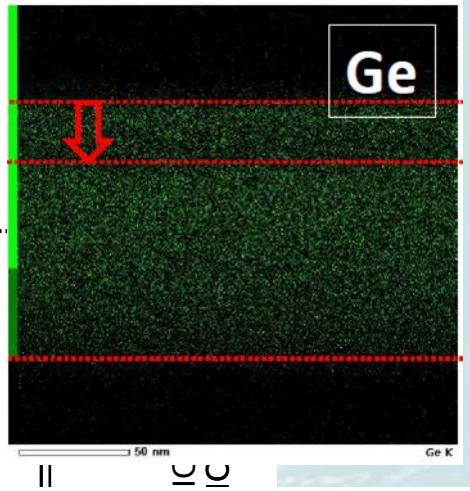
IMEC 45% SiGe Epi

PCOR-SIMS℠



1.7J

2.4J



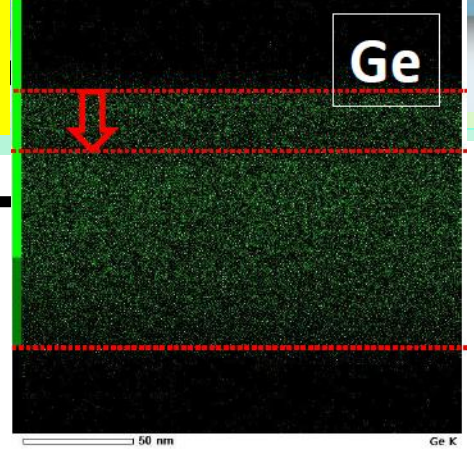
EAG LABORATORIES | Eurofins Materials Science

EAG LABORATORIES | Eurofins Materials Science

J.O.B. Te
Sales &

IMEC 45% SiGe Epi→ 1.1%

Meiji University



High Ge requires Ga or Al p+ doping and boost contact resistance!

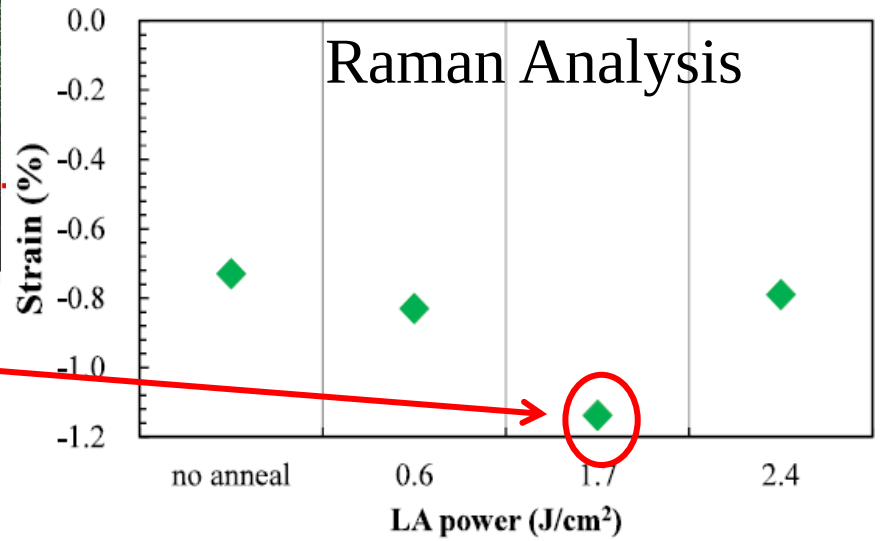
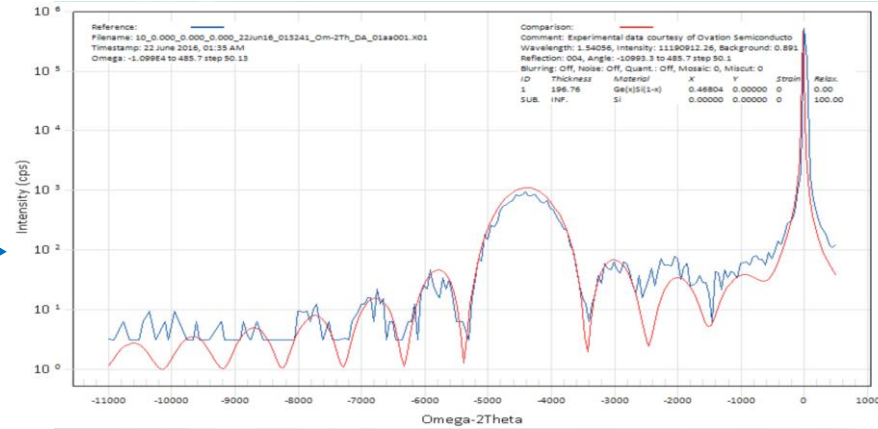


Fig. 4 Strain in SiGe without C or Ge implantation before and after LA.

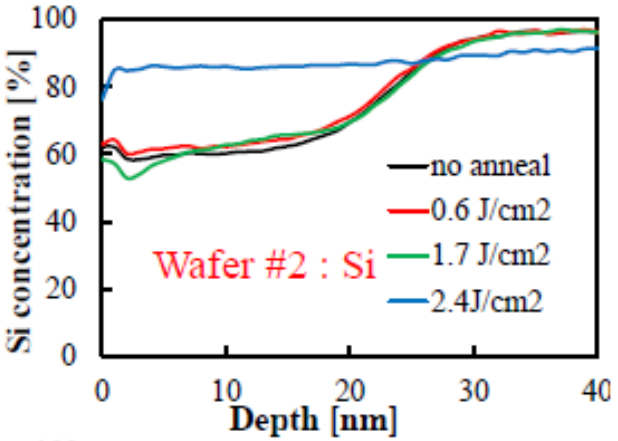


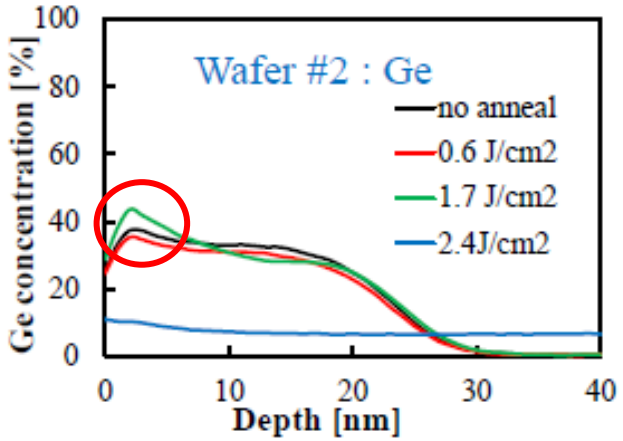
IMEC XRD Analysis
20nm 45%-SiGe Epi

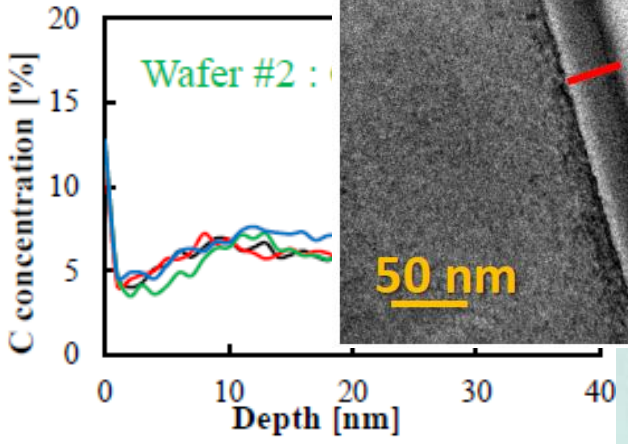
- ✓ **LA = 1.7 and 2.4 J/cm²**

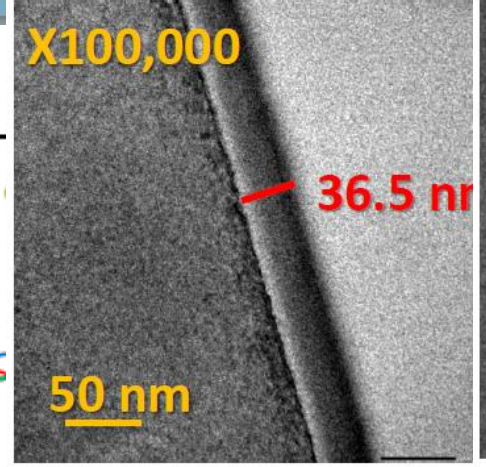
⇒The thickness of SiGe layer and Si and Ge concentration change

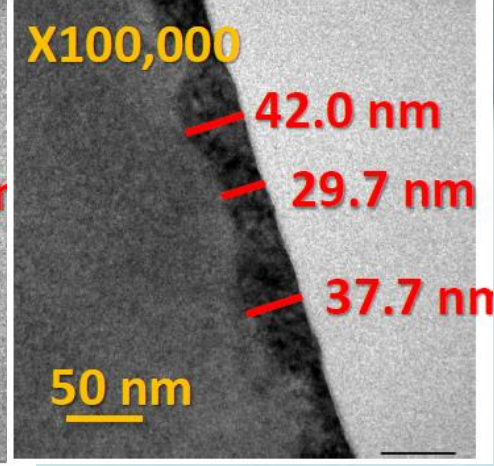
Compare #2 and #10 wafers (Si,Ge,C)

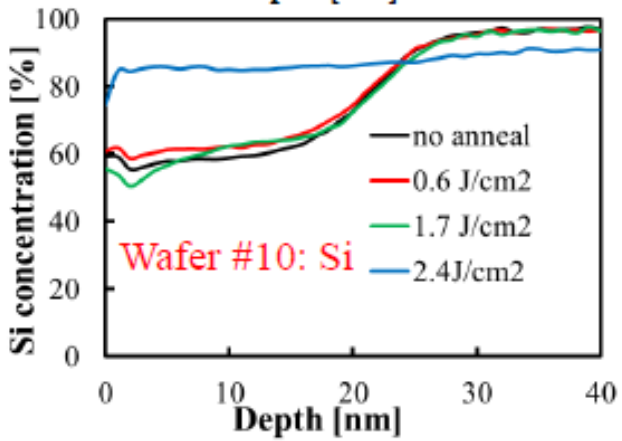


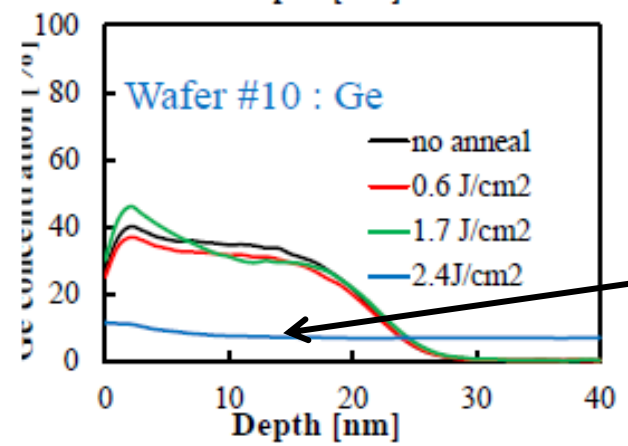


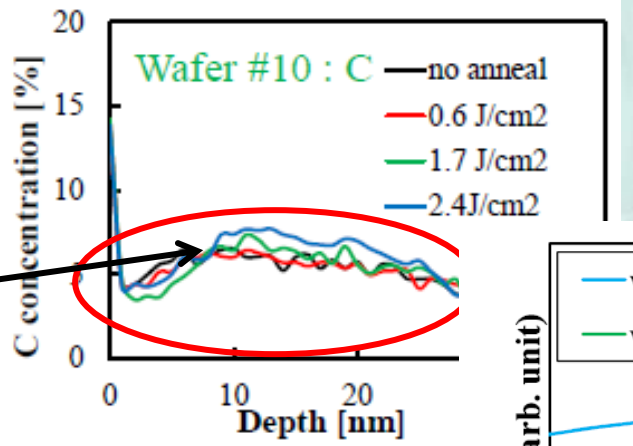












- ✓ **LA = 1.7 and 2.4 J/cm²**
  ⇒The thickness of SiGe layer and Si and Ge concentration change
- ✓ **C concentration does not change depending on LA conditions.**

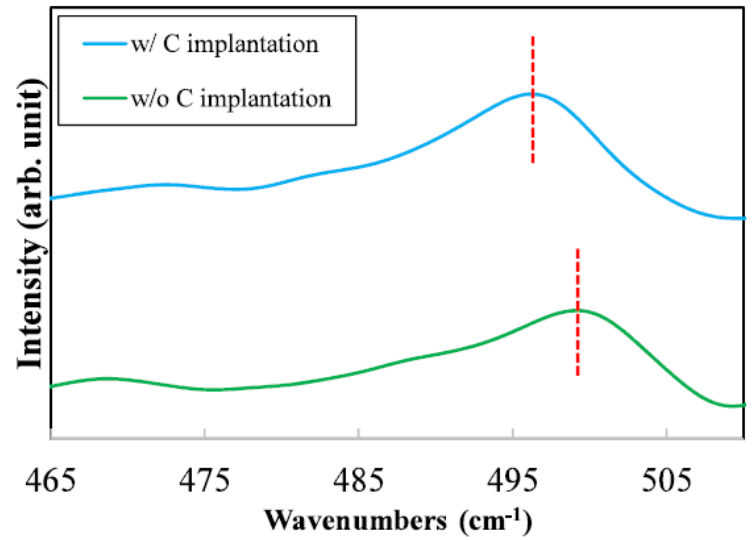


Fig. 5 Comparison of Raman peak shift with and without C implantation after LA at 1.7 J/cm².

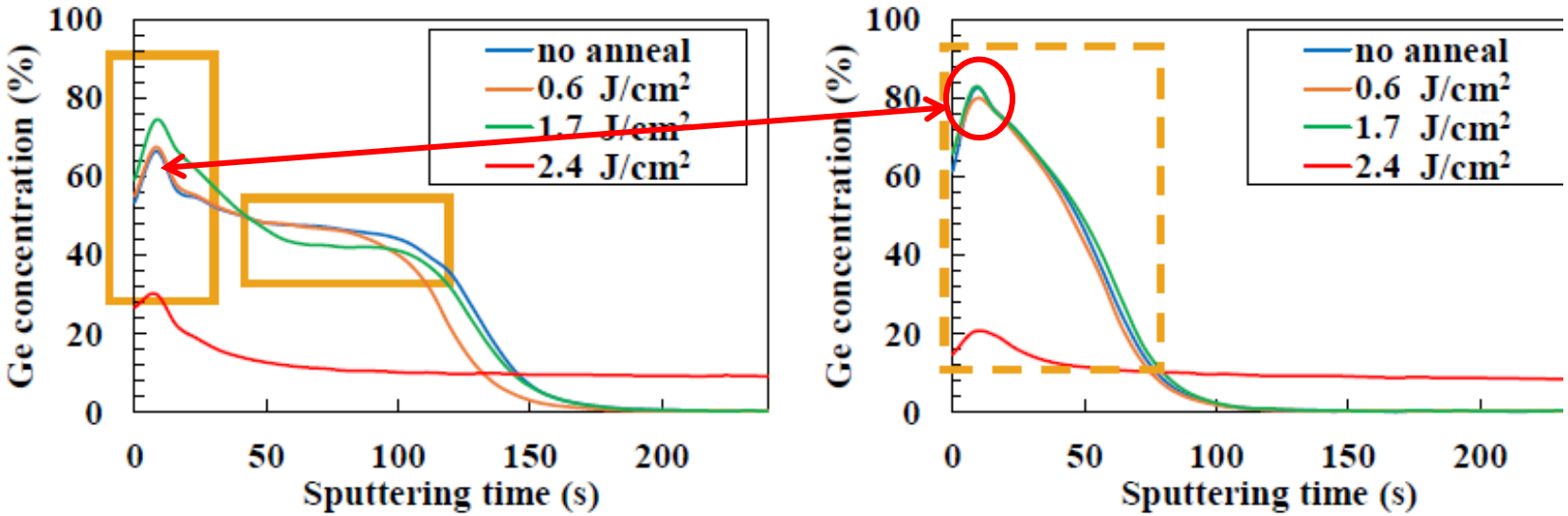
IMEC 45% SiGe Epi

IMEC 45% SiGe Epi

r vs. element distribution

Ge surface sputtering (high beam current)

✓ **Ge concentration with and without Ge implantation**



the sample without implantation (process A)

the sample with Ge implantation (process C)

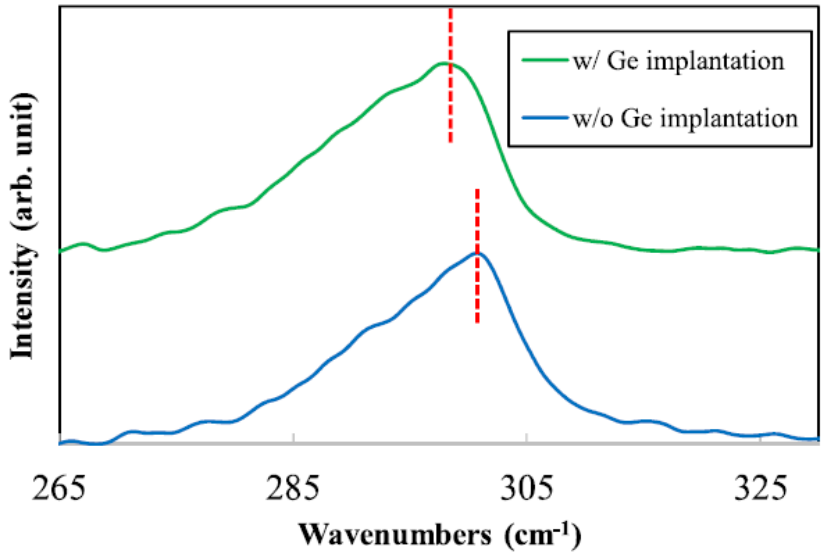
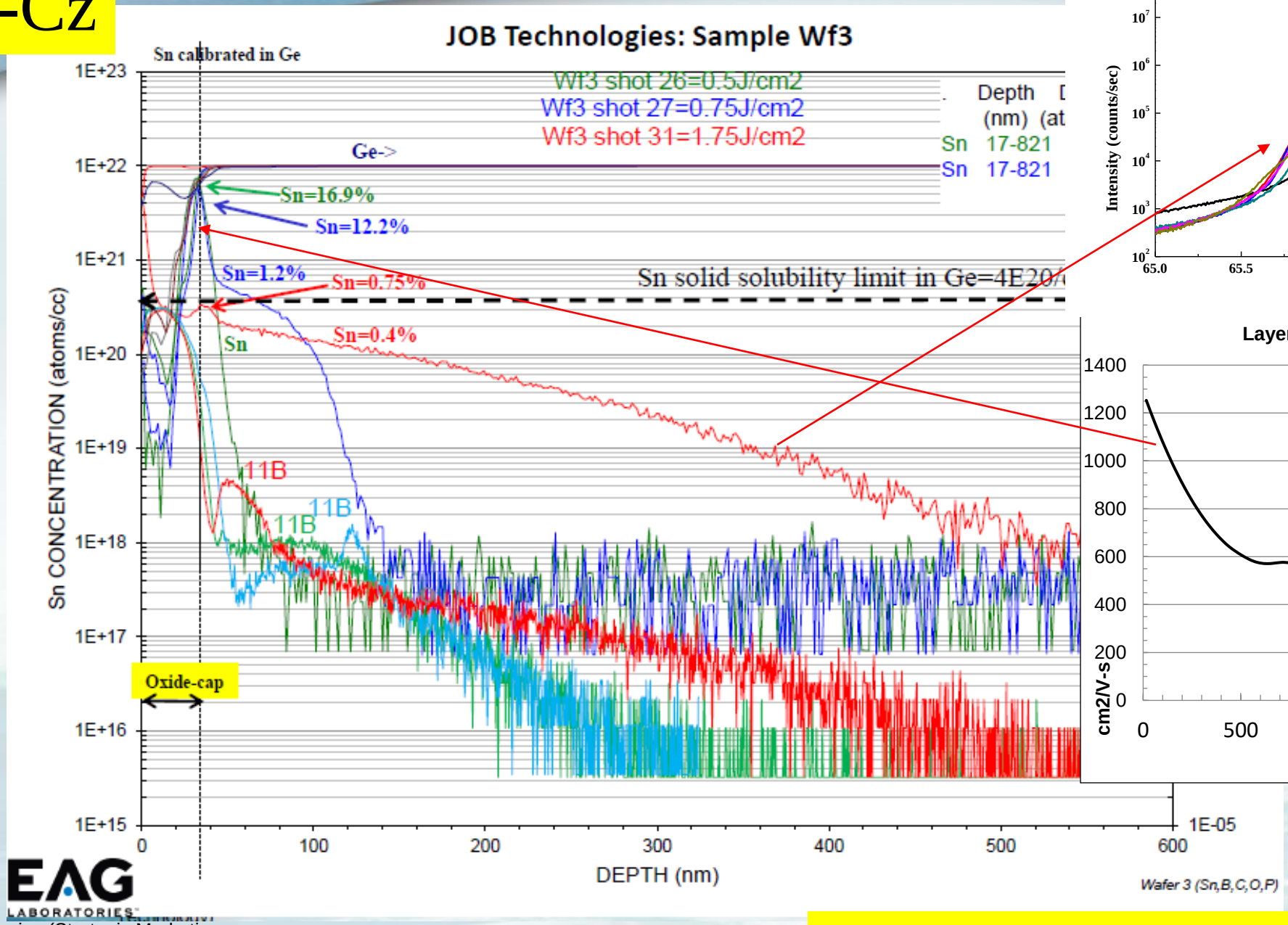


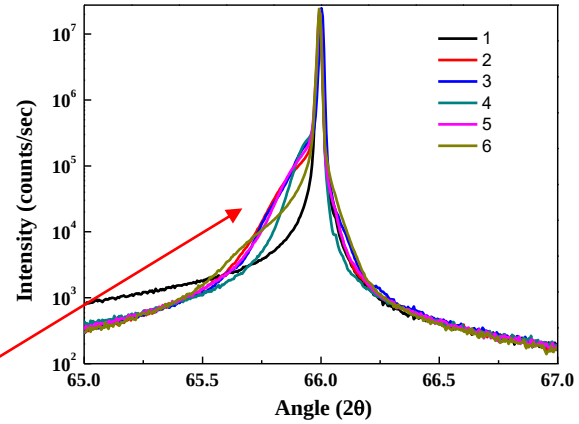
Fig. 6 Comparison of Raman peak shift with and without Ge implantation after LA at 1.7 J/cm².

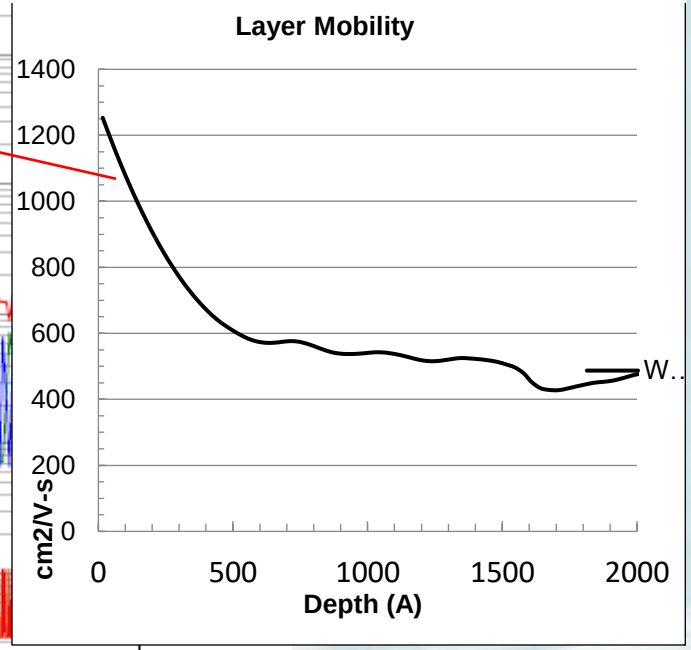
- **high Ge concentration at the surface (up to 1.7 J/cm²)**
- **Ge melted into the Si substrate from SiGe layer (at 2.4 J/cm²)**
- **Ge redistribution was suppressed by Ge implantation**

AiMES 2018

SMIT Ge-Cz





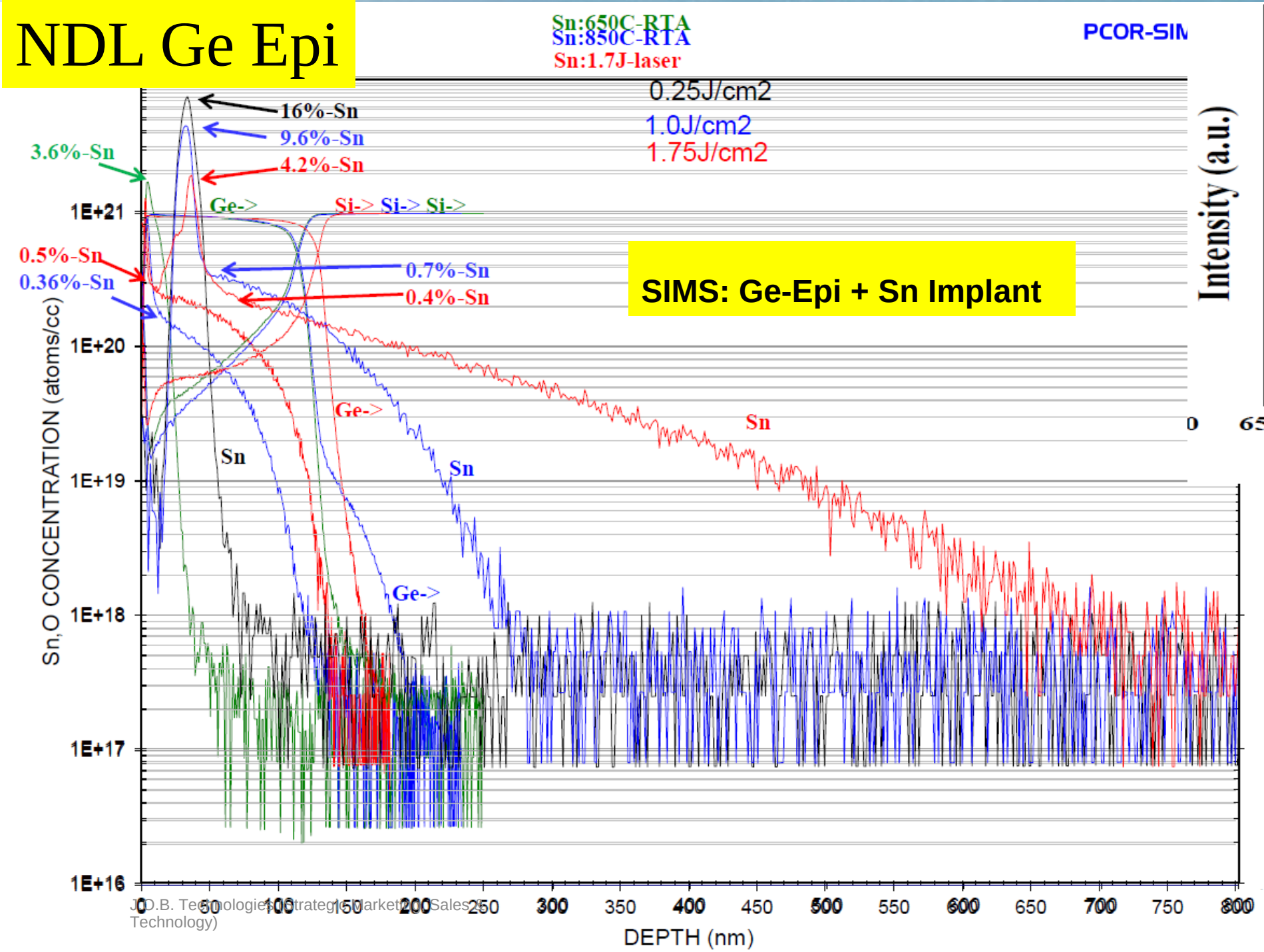


J.O.B. Technologies (Strategic Marketing, Sales & Technology)

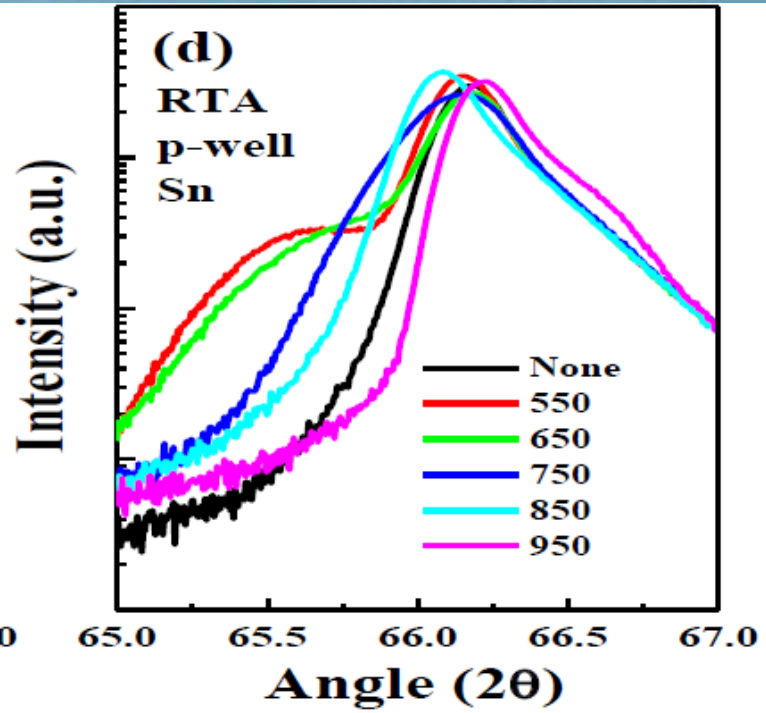
Borland et al., IIT-2016, Sept 29, 2016

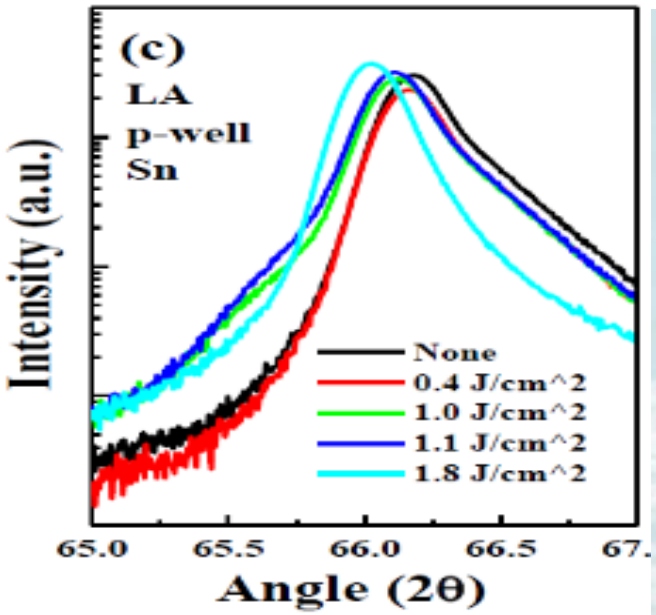
SIMS, XRD & u: Ge-Cz + Sn Implant

NDL Ge Epi

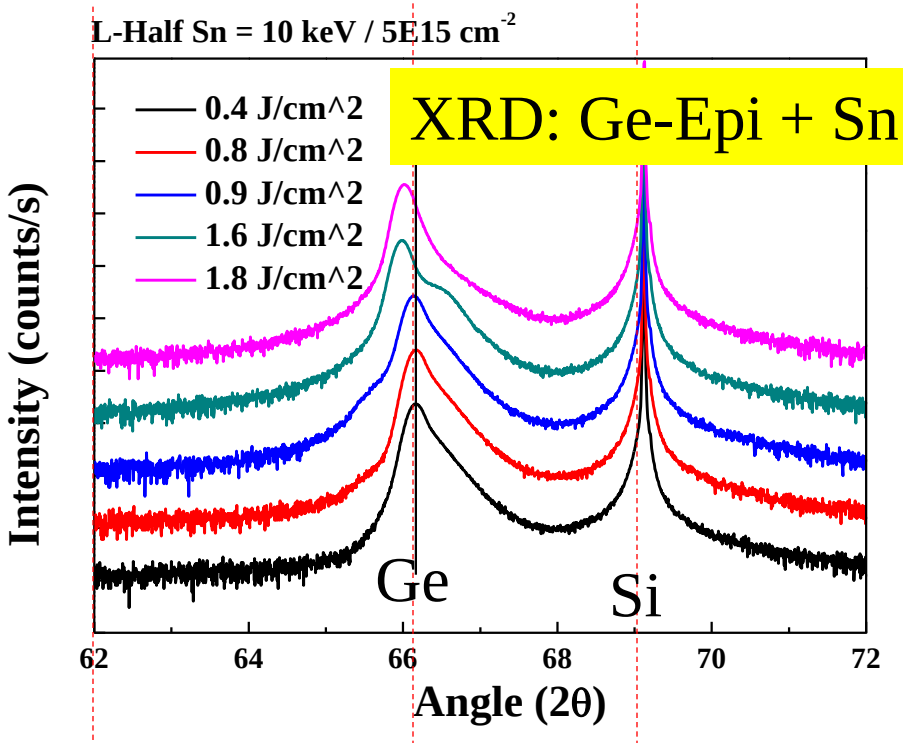


SIMS: Ge-Epi + Sn Implant

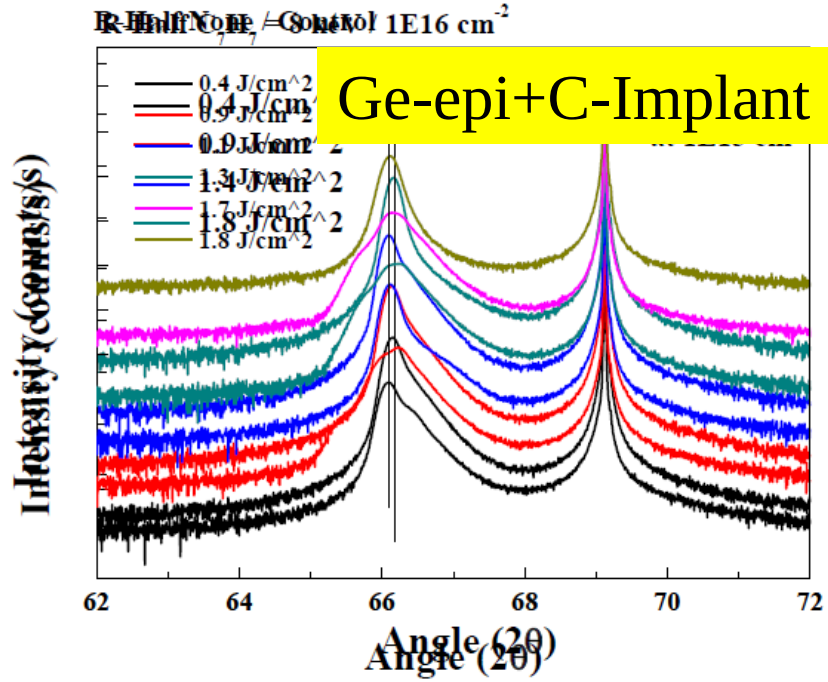




Borland et al., IIT-2018

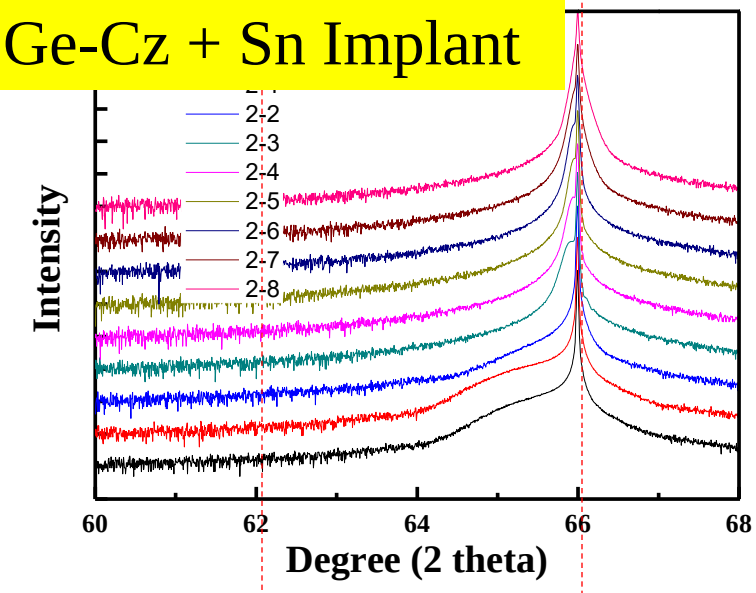


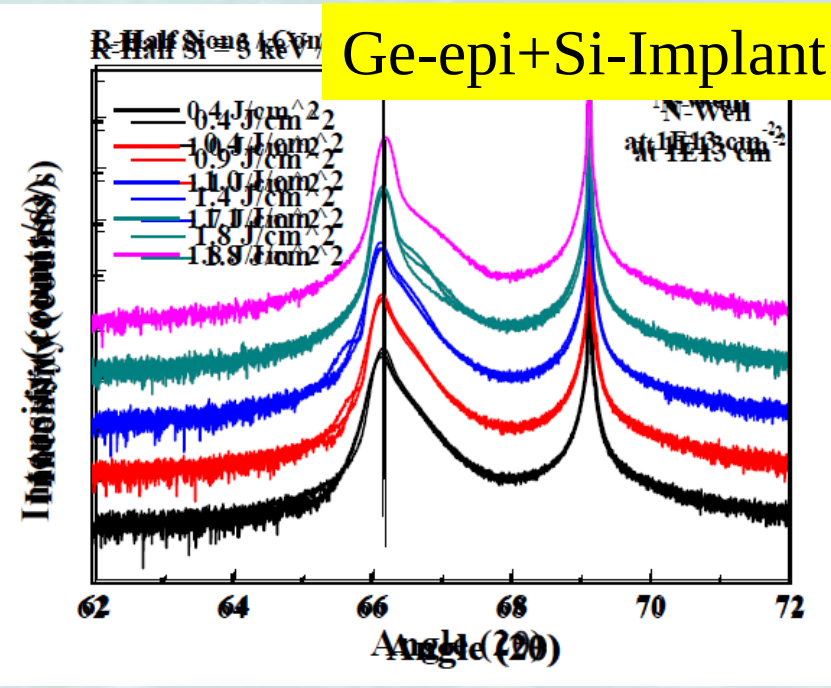
XRD: Ge-Epi + Sn Implant



Ge-epi+C-Implant

XRD: Ge-Cz + Sn Implant

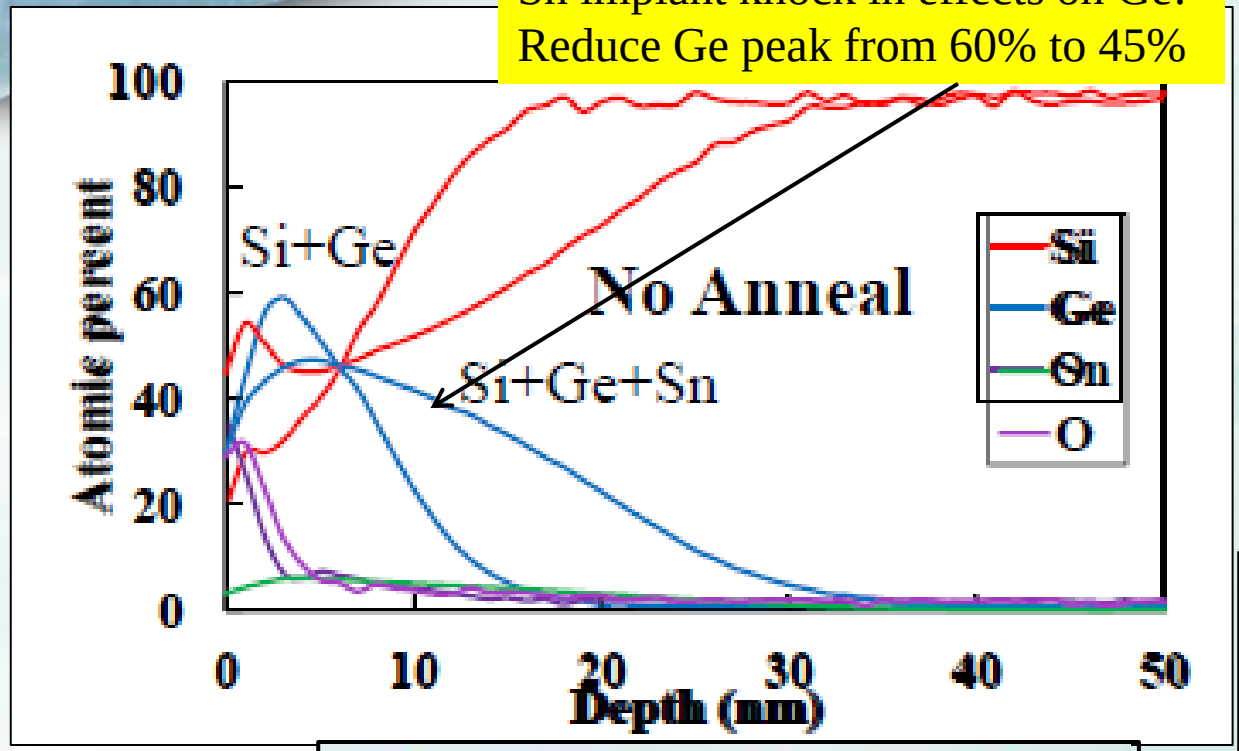


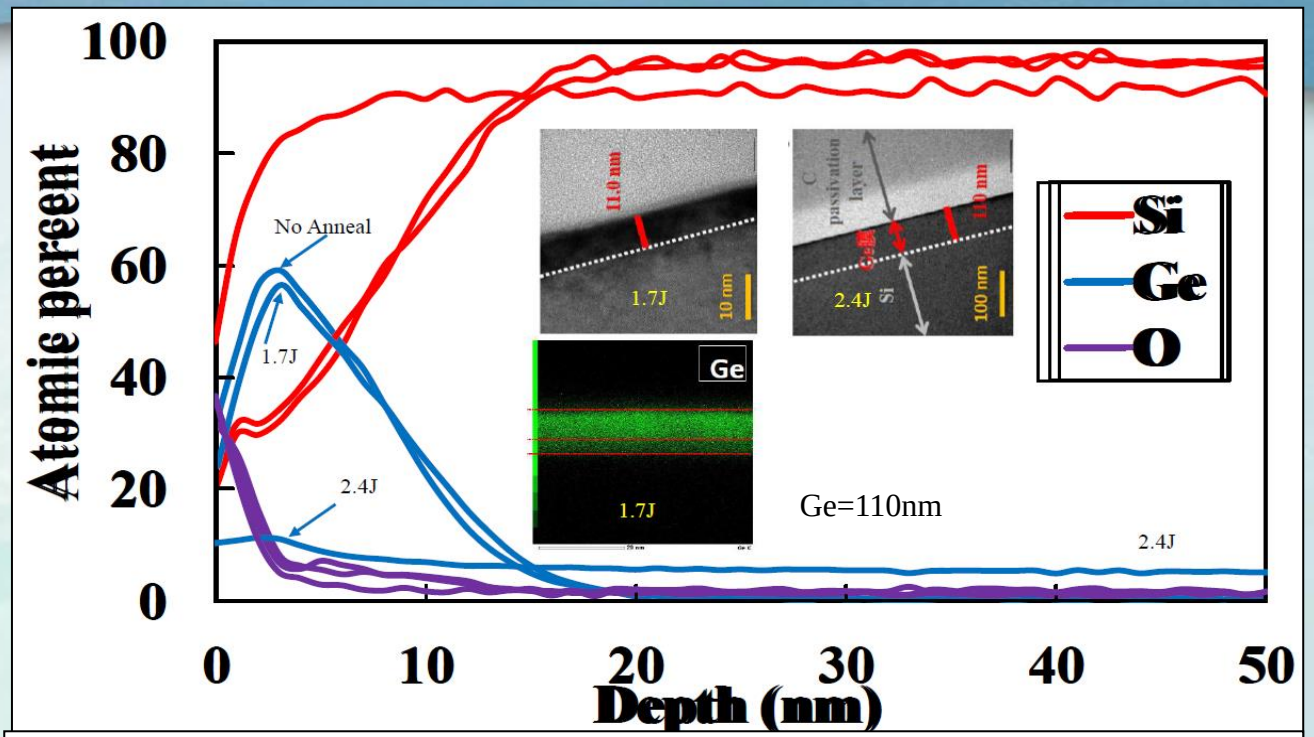


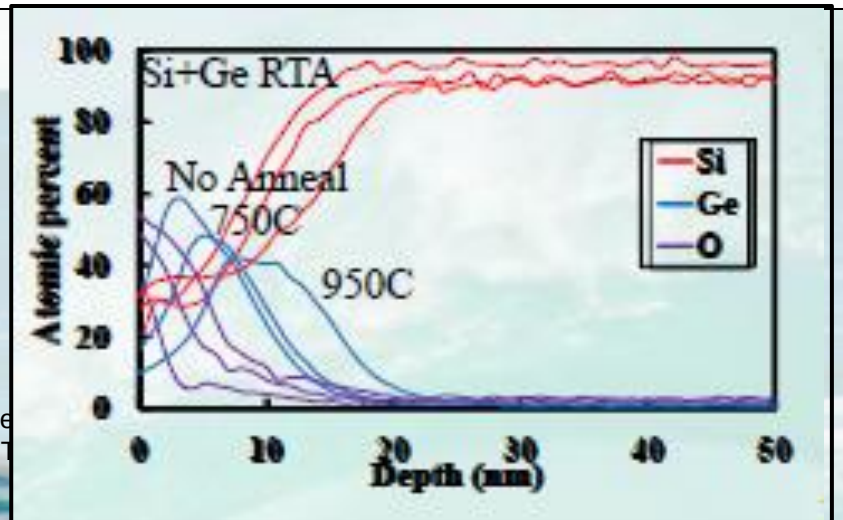
Ge-epi+Si-Implant

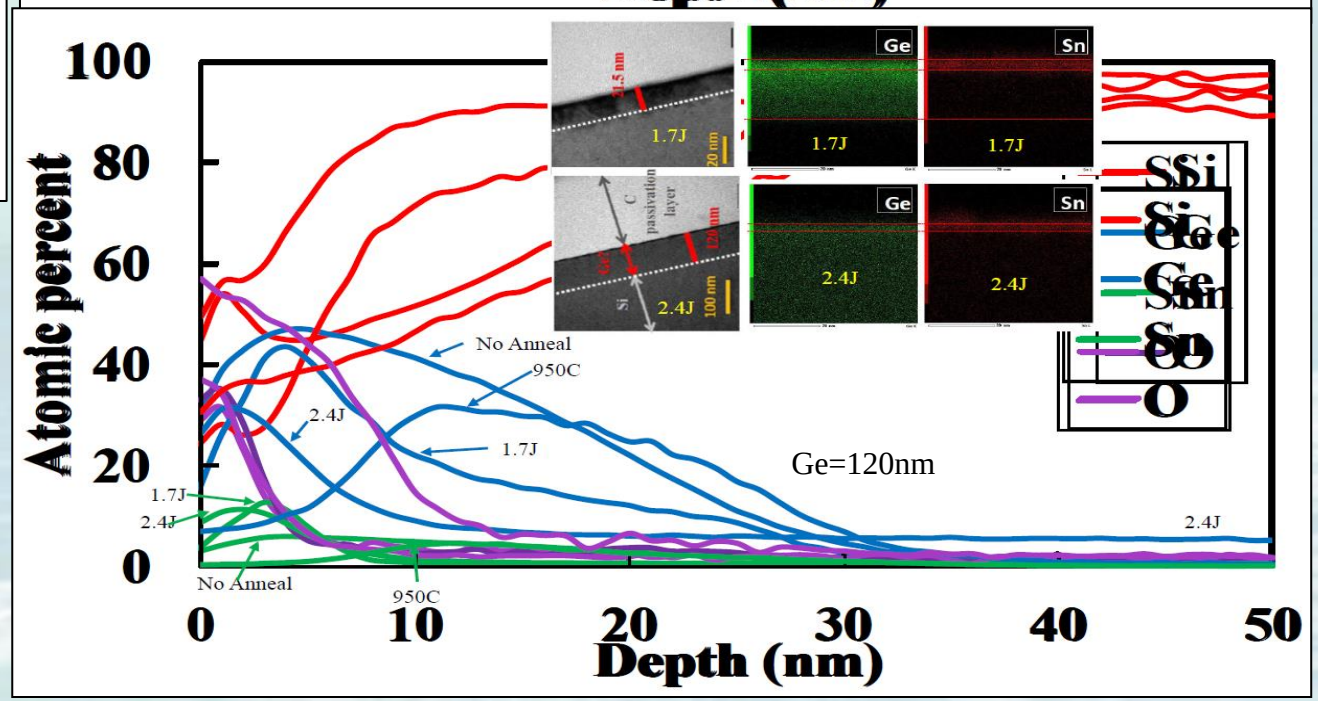
Renesas Si-Cz

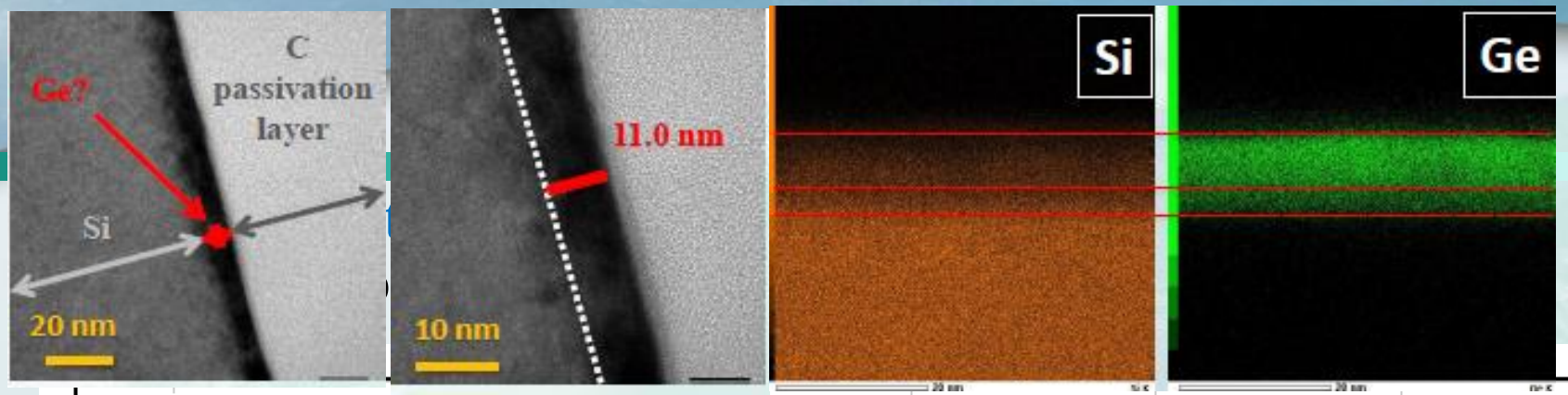
Sn implant knock in effects on Ge!
Reduce Ge peak from 60% to 45%



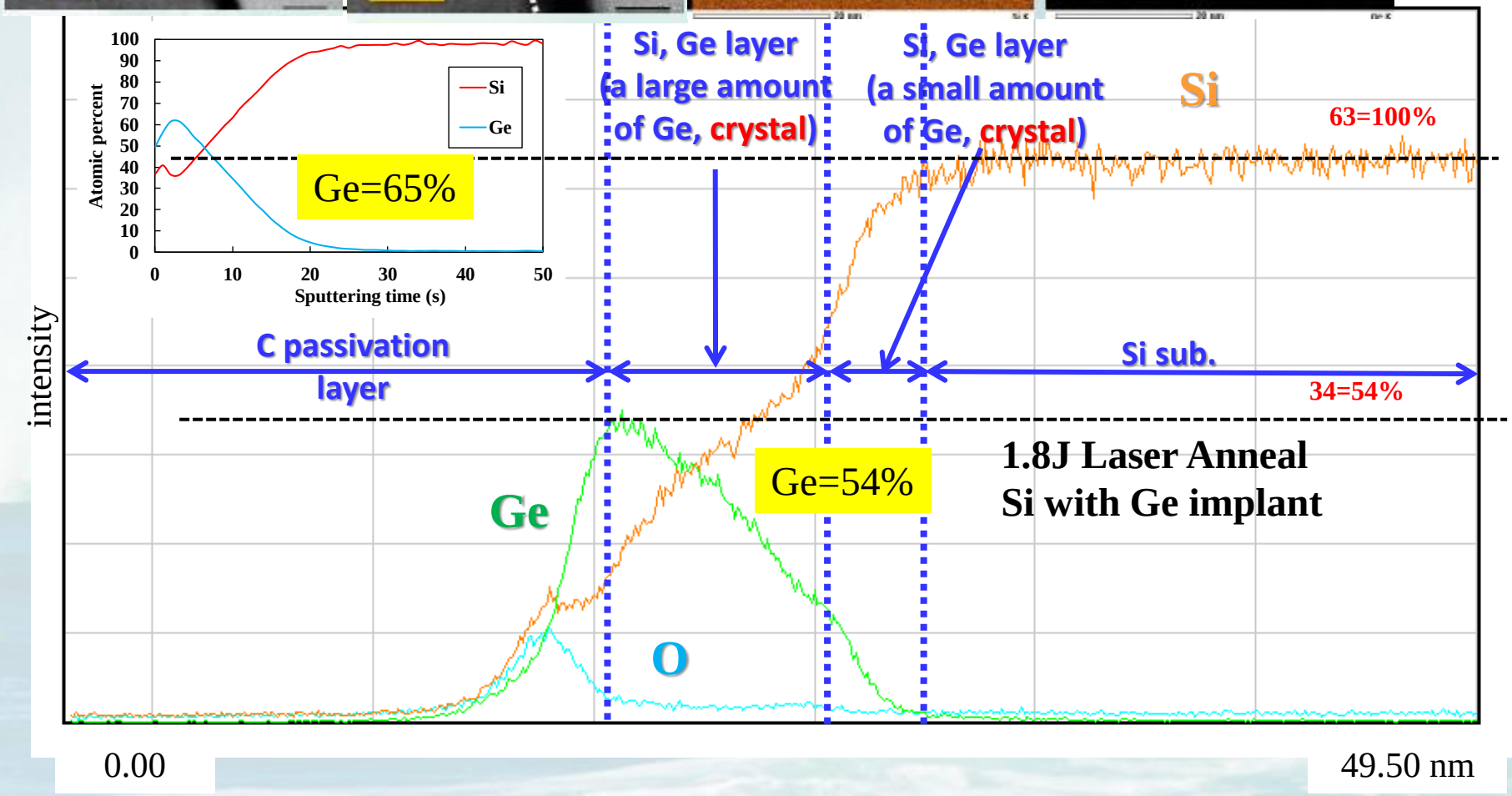


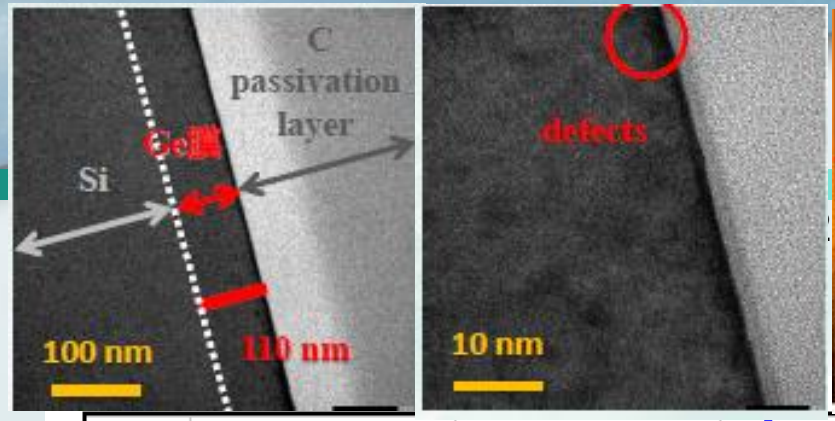


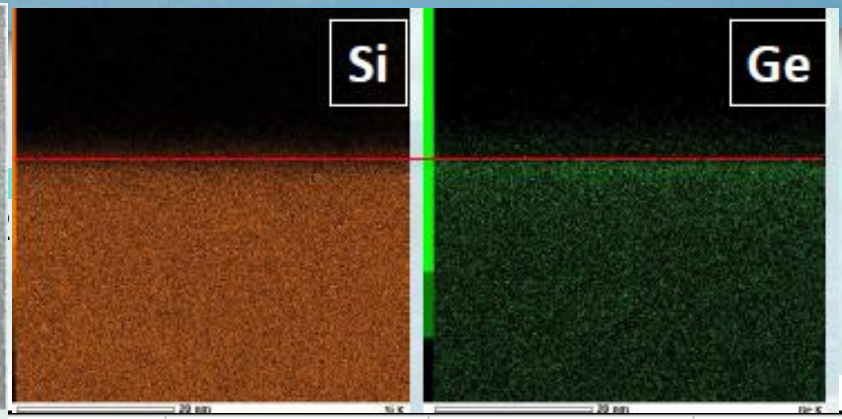



Ge?
C passivation layer
Si
20 nm
11.0 nm
10 nm
Si
Ge

Ge=65%

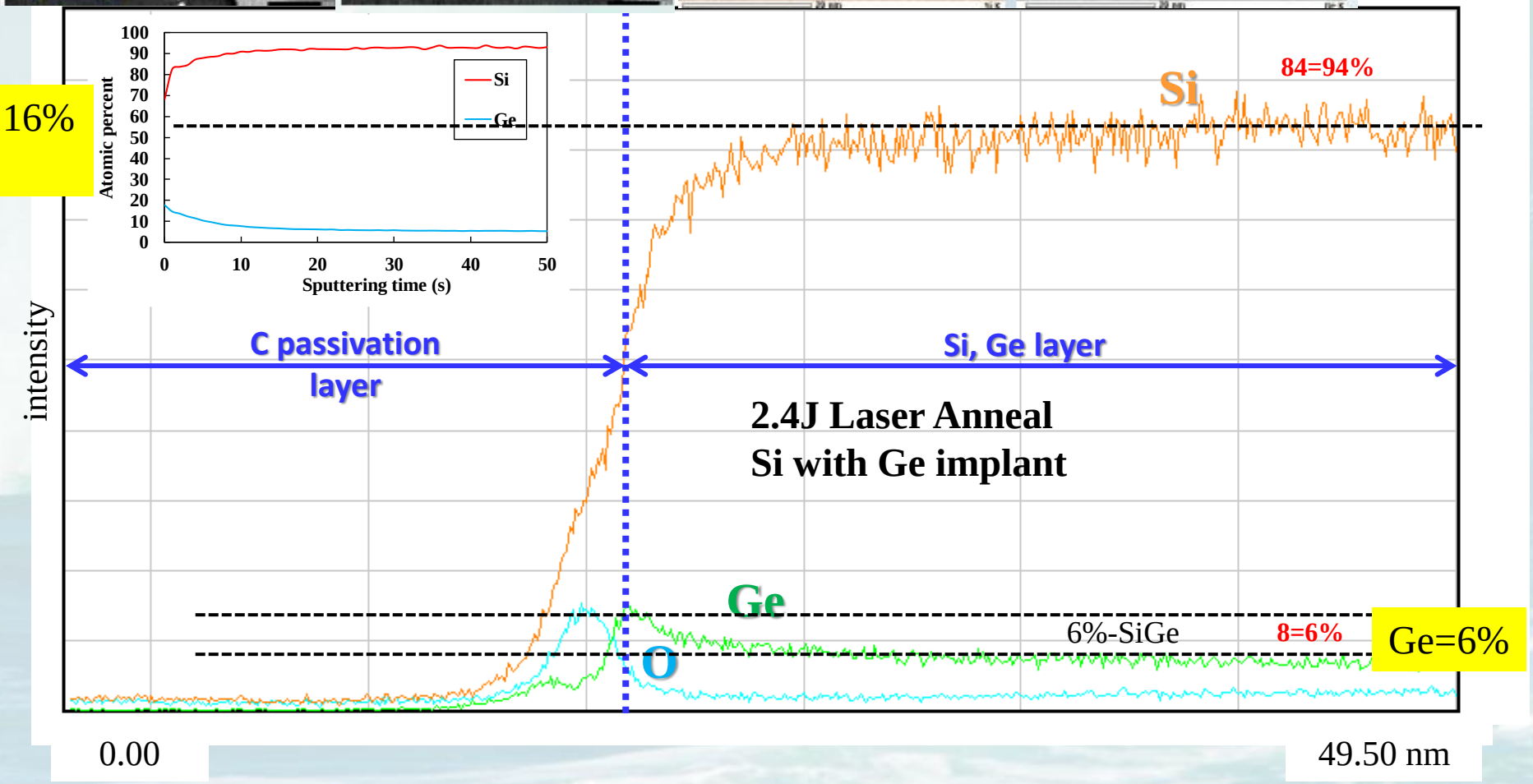

Atomic percent
Sputtering time (s)
Si
Ge
Ge=65%
Si, Ge layer (a large amount of Ge, crystal)
Si, Ge layer (a small amount of Ge, crystal)
Si
63=100%
intensity
C passivation layer
Si sub.
34=54%
Ge=54%
1.8J Laser Anneal
Si with Ge implant
Ge
O
0.00
49.50 nm

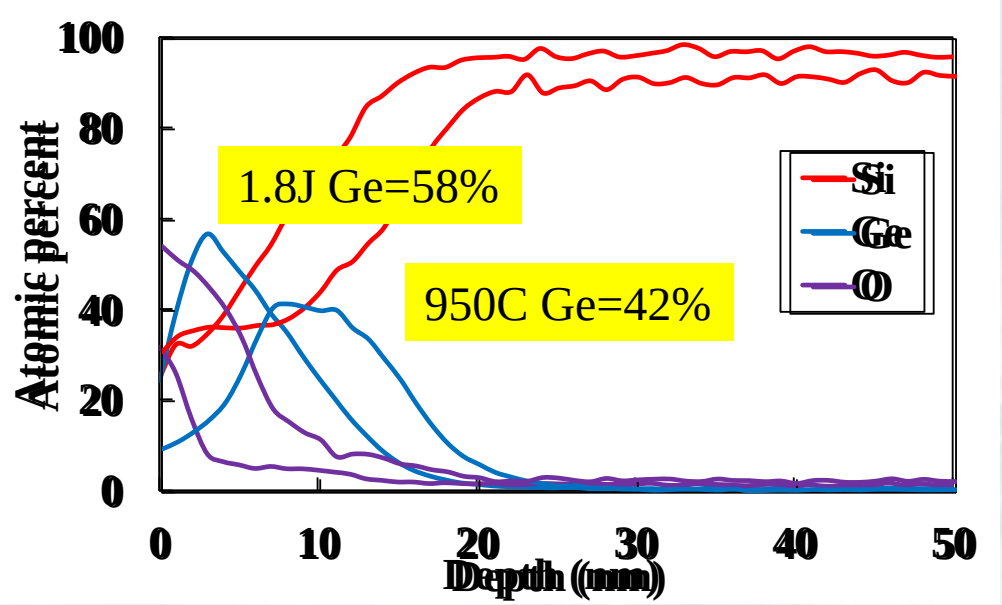


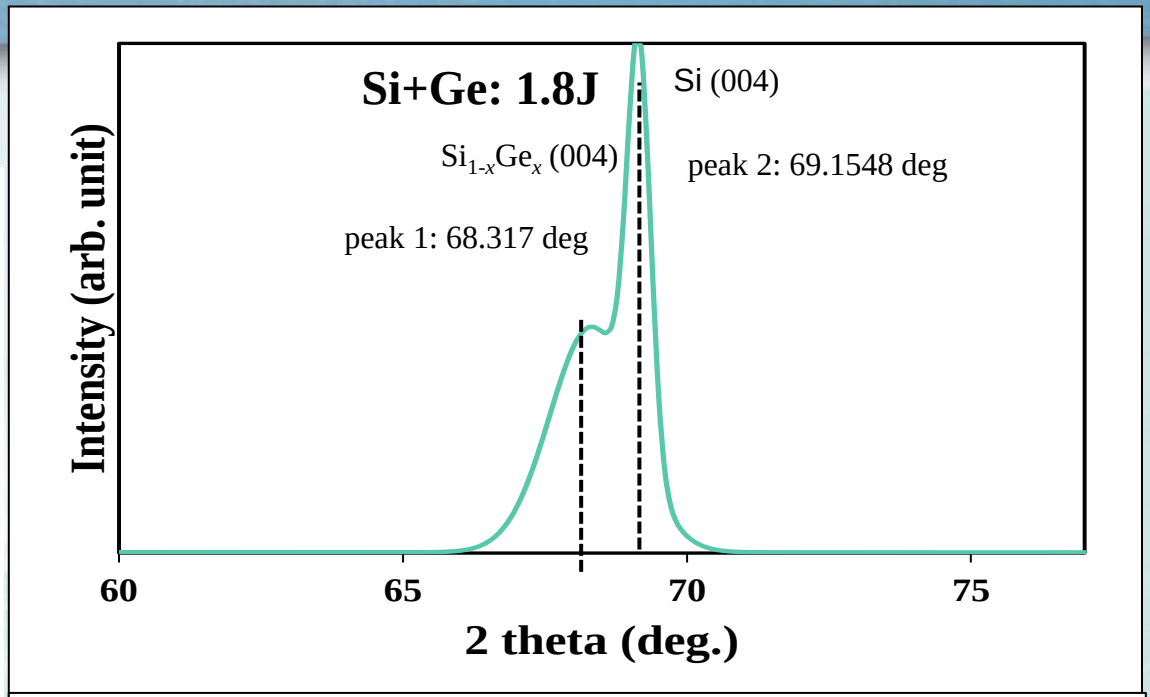


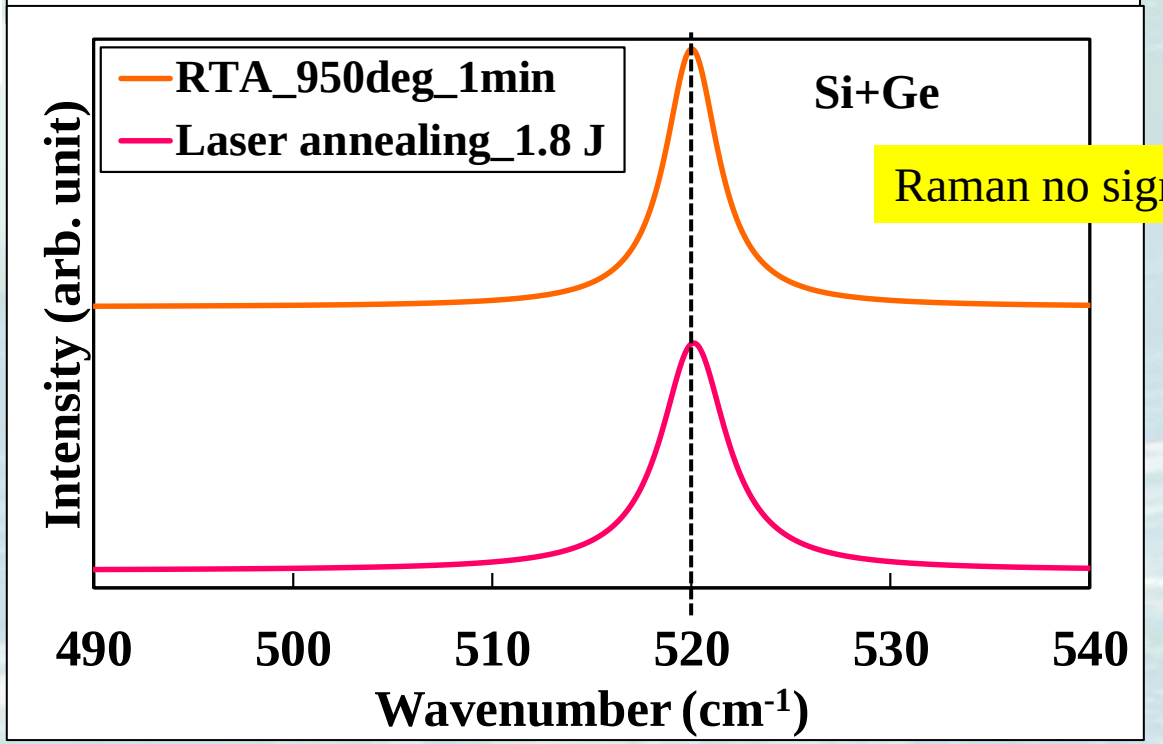
Ge=6%

Ge Peak = 16%
Bulk = 6%

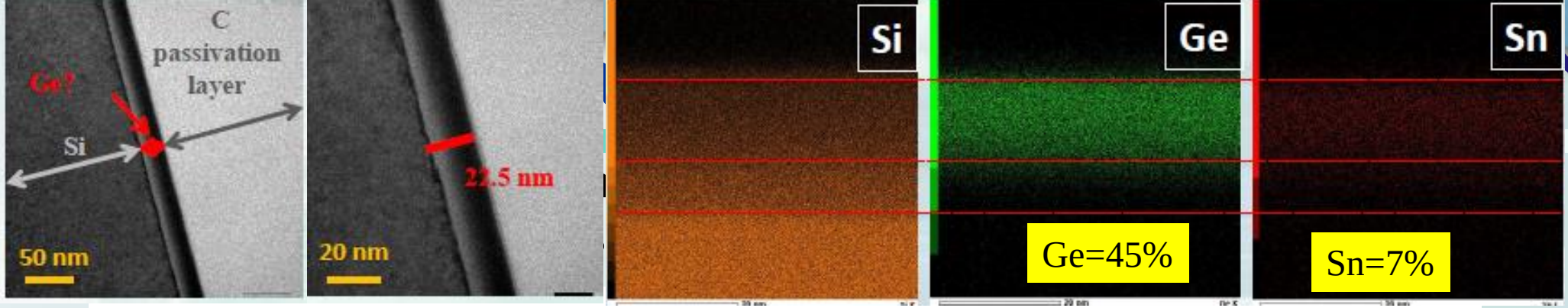


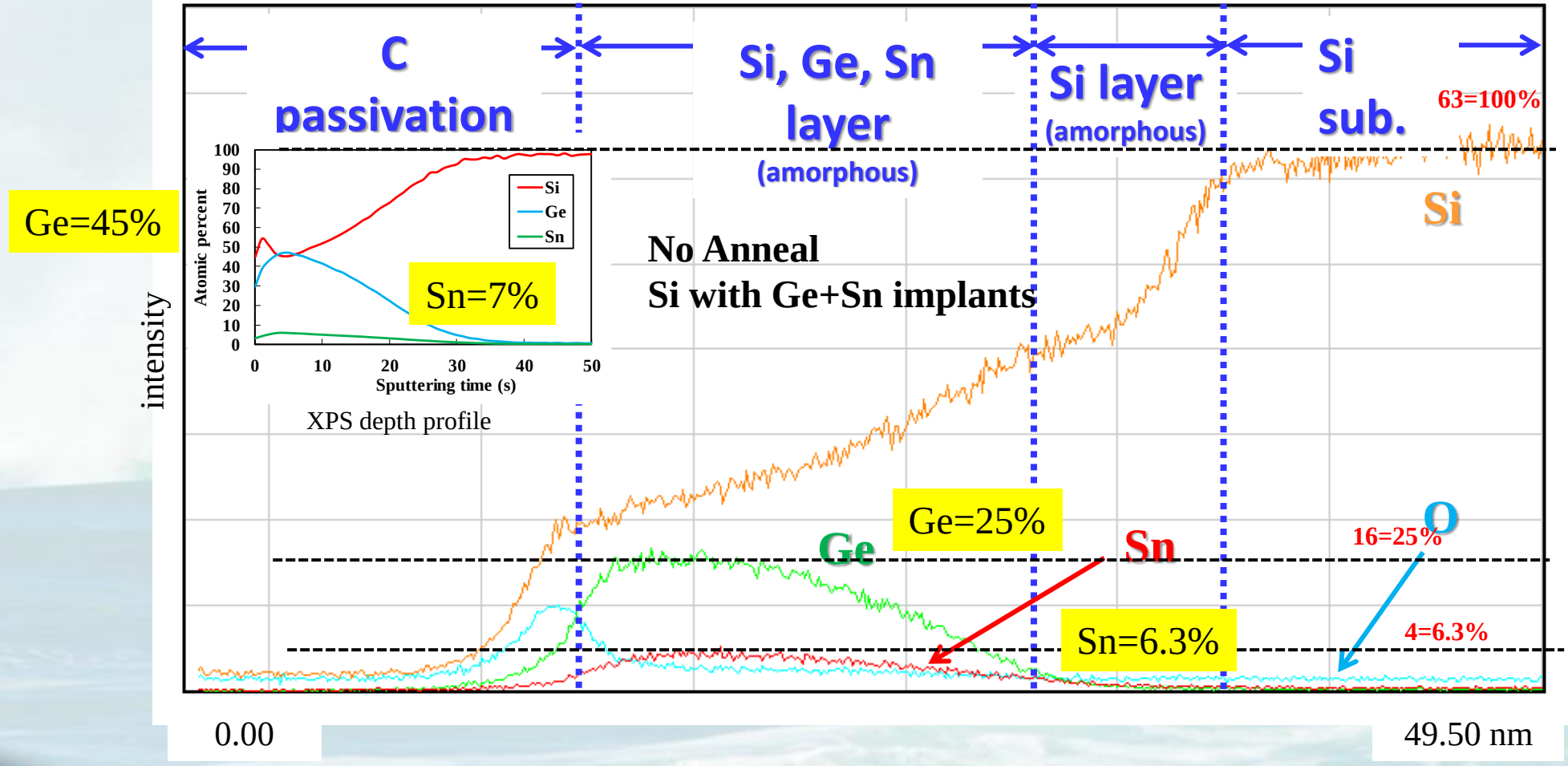


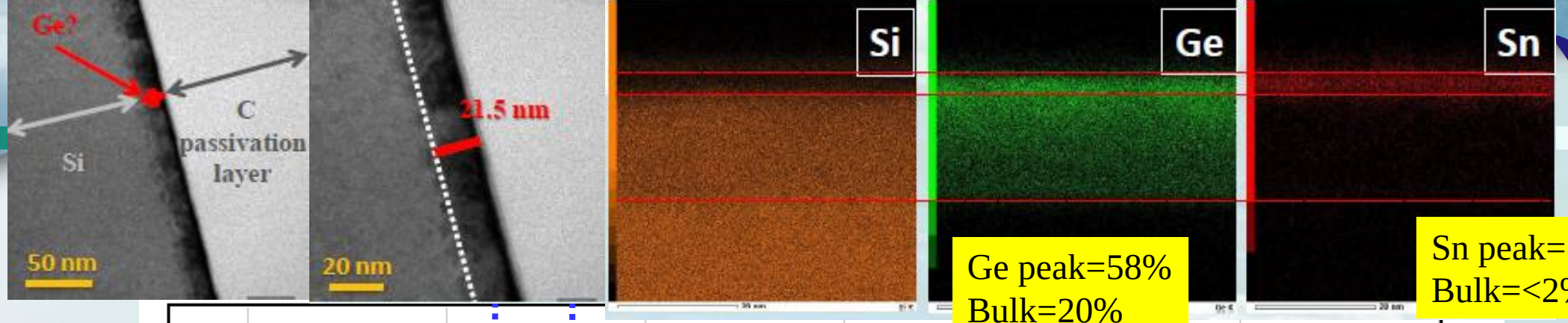




Raman no significant strain

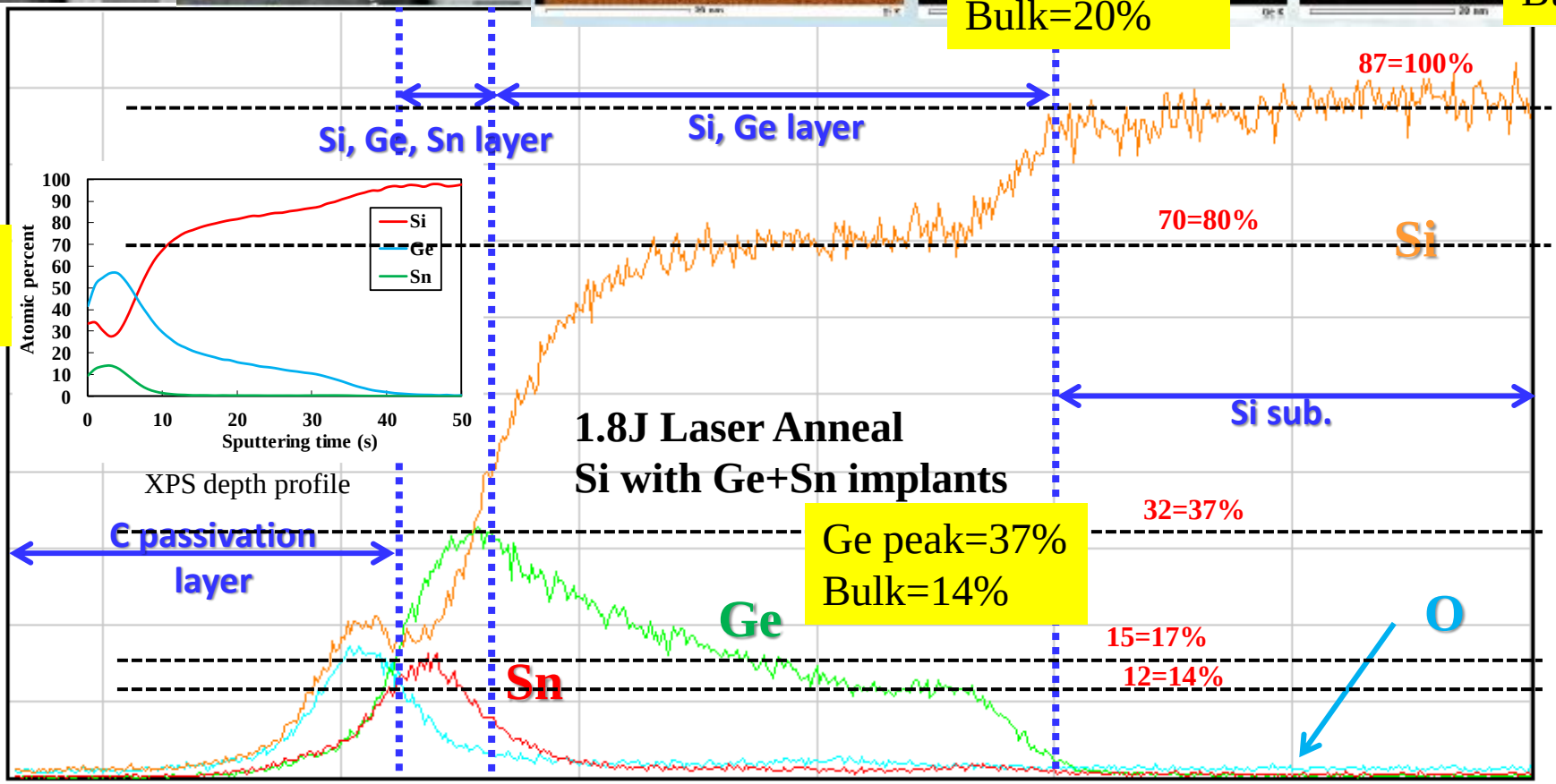

C passivation layer
Ge?
Si
50 nm
22.5 nm
20 nm
Si
Ge
Sn
Ge=45%
Sn=7%


C passivation
Si, Ge, Sn layer (amorphous)
Si layer (amorphous)
Si sub.
63=100%
Si
Ge=45%
intensity
No Anneal
Si with Ge+Sn implants
Atomic percent
Sputtering time (s)
Si
Ge
Sn
Sn=7%
XPS depth profile
Ge=25%
Ge
Sn
O
16=25%
Sn=6.3%
4=6.3%
0.00
49.50 nm



Ge peak=58%
Bulk=20%

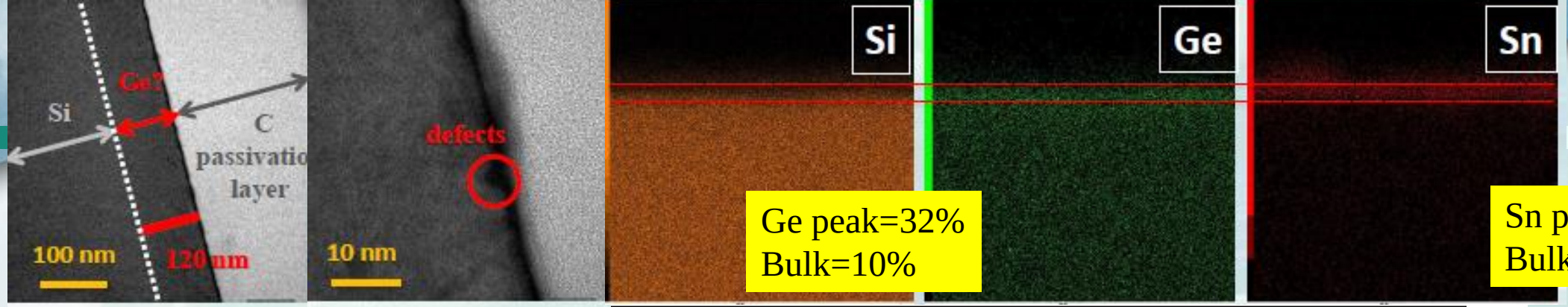
Sn peak=15%
Bulk=<2%



Ge peak=58%
Bulk=20%

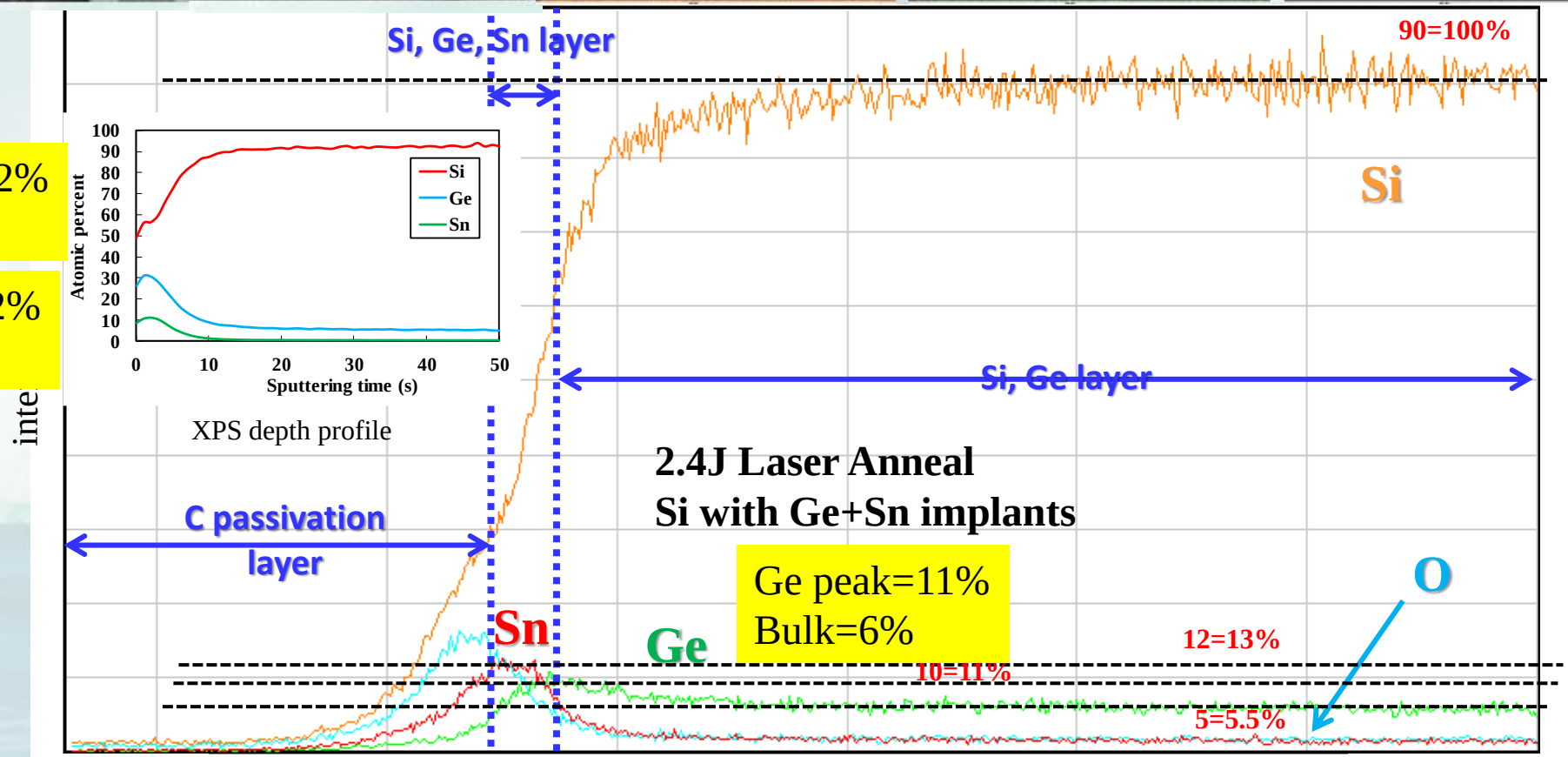
Sn peak=15%
Bulk=<2%

Sn peak=17%
Bulk=<2%



Ge peak=32%
Bulk=10%

Sn peak=12%
Bulk=<2%



Sn peak=13%
Bulk=<2%

Si with Ge+Sn implantation **0.54%** compressive strain after 1.8J laser and **1.80%** after 950C RTA

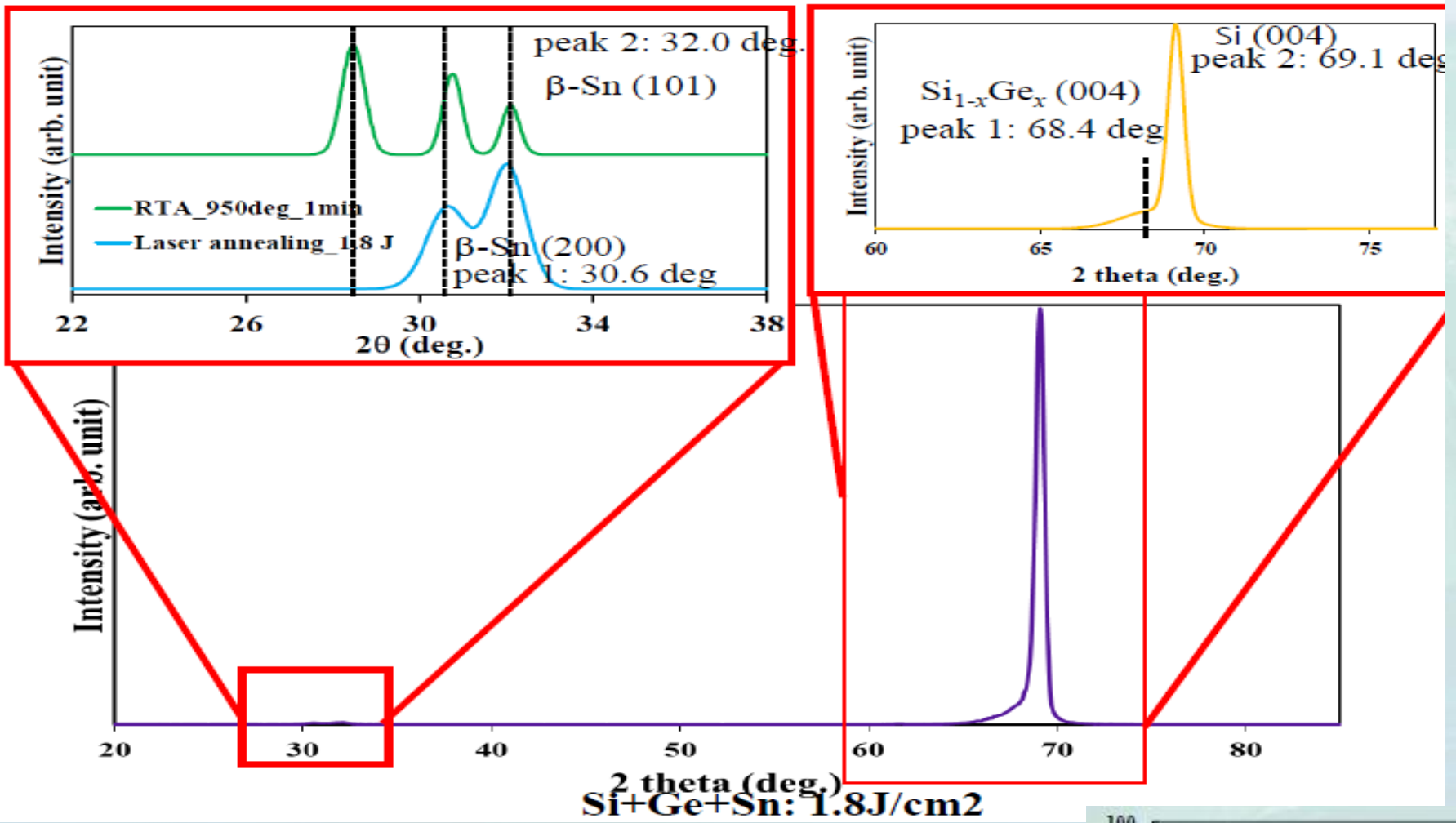


Fig.4: XRD analysis after RTA and melt laser anneal.

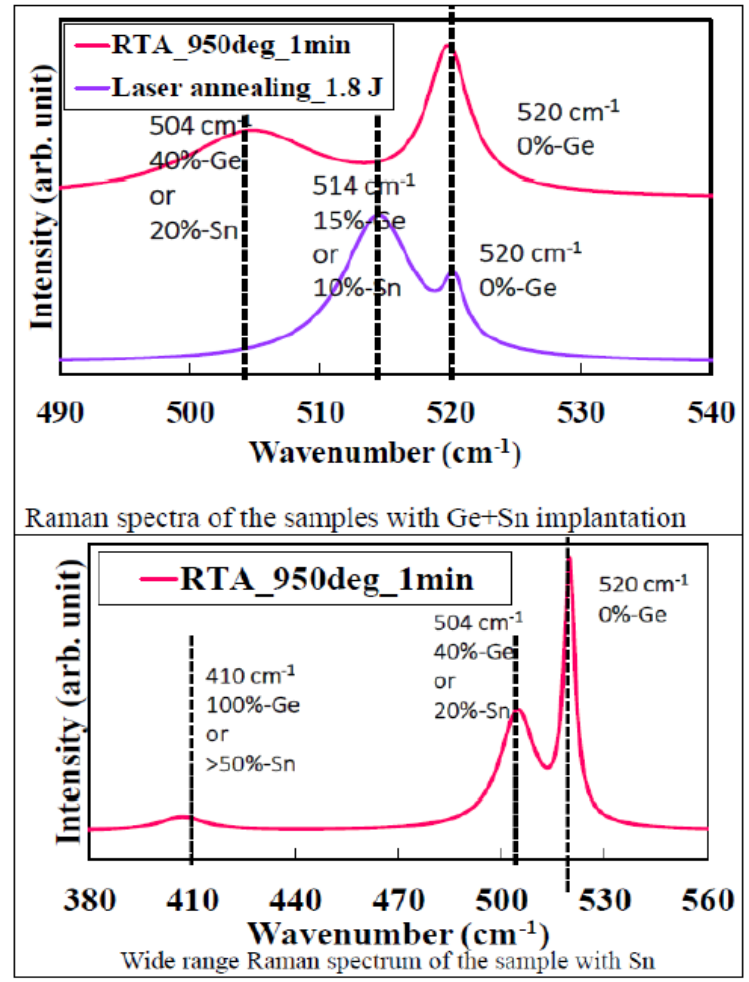
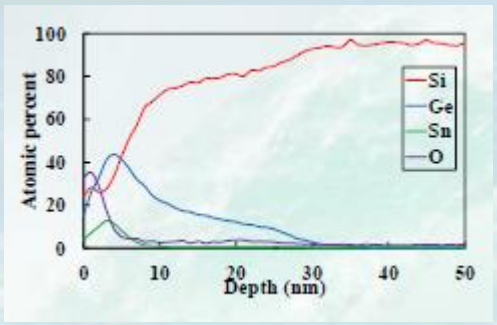
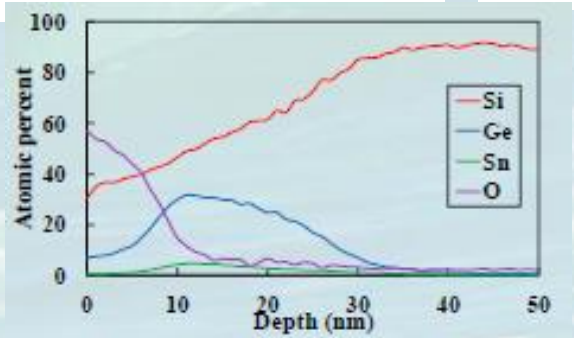


Fig.5: Raman Spectra analysis.



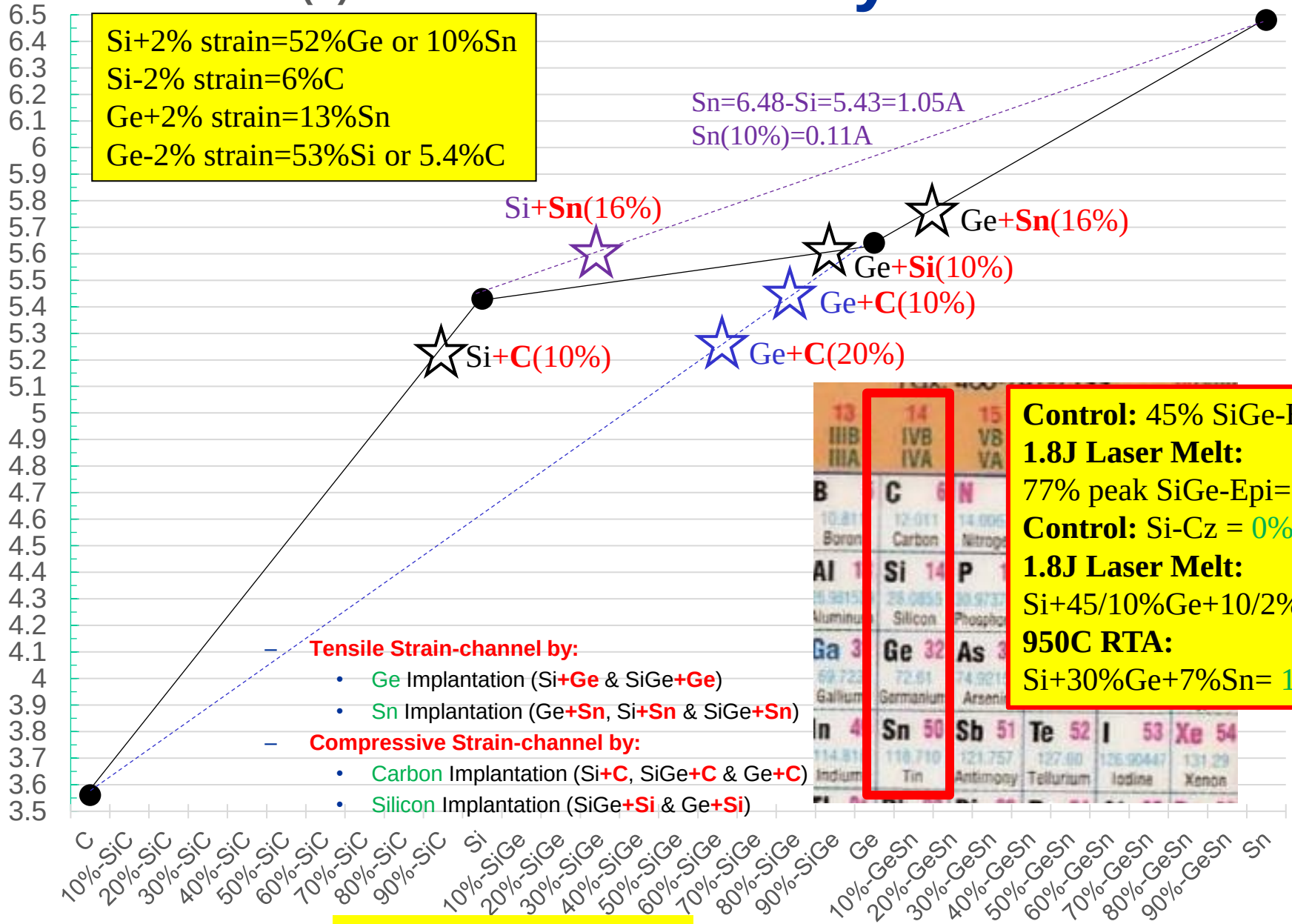


Ge peak=45%
Bulk=10%

Sn peak=10%
Bulk=<2%

Ge = 35%
Sn = 6%

Summary



Control: 45% SiGe-Epi = 0.7% strain
1.8J Laser Melt:
77% peak SiGe-Epi= 1.15% strain
Control: Si-Cz = 0% strain
1.8J Laser Melt:
Si+45/10%Ge+10/2%Sn= 0.54% strain
950C RTA:
Si+30%Ge+7%Sn= 1.8% strain

J. Borland, ECS Oct 2016

Acknowledgements

- Si-Cz wafers from Renesas
- 45%-SiGe Epi wafers from IMEC
- Ge-Epi wafers from NDL
- Ge-Cz wafers from SMIT
- Sn, Ge, C & Si implantations from Nissin and SMIT
- Laser Anneals by LASSE-Screen in France
- RTA anneals by NDL and Meiji University
- SIMS analysis by EAG
- Raman analysis by Meiji University
- TEM-EDX analysis by Meiji University
- XRD analysis by Meiji University