SYNOPSYS®
Silicon to Software™

Materials Modeling in Design/System Technology Co-Optimization (DTCO/STCO)

Shela Aboud, PMM

December 8, 2022

CONFIDENTIAL INFORMATION

The information contained in this presentation is the confidential and proprietary information of Synopsys. You are not permitted to disseminate or use any of the information provided to you in this presentation outside of Synopsys without prior written authorization.

IMPORTANT NOTICE

In the event information in this presentation reflects Synopsys' future plans, such plans are as of the date of this presentation and are subject to change. Synopsys is not obligated to update this presentation or develop the products with the features and functionality discussed in this presentation. Additionally, Synopsys' services and products may only be offered and purchased pursuant to an authorized quote and purchase order or a mutually agreed upon written contract with Synopsys.

Outline

- Technology Roadmap
- Advanced Logic Roadmap and DTCO
- Materials Modeling in DTCO
- DTCO for Power Electronics Applications
- QuantumATK: Defects and Diffusion Analyzer
- Materials Modeling in STCO

Technology Roadmap

Transformational Applications Continue to Motivate and Drive Semiconductor Industry and Technology Growth

Application Drivers


5G


Internet of Things


AR / VR / MR


Autonomous Driving

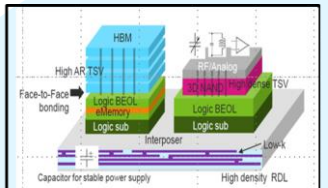

Vehicle Electrification


Artificial Intelligence


Cloud / Datacenter

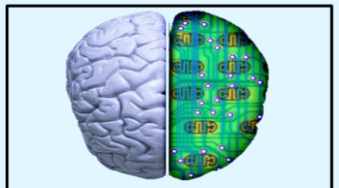
Power Electronics

Technology Enablers

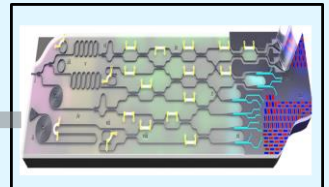


System Integration / 3DIC

AI Specific Hardware


Neuromorphic Computing

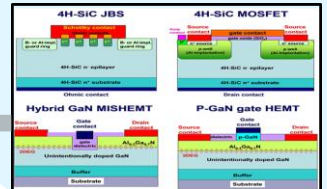
Data Center Communication Bandwidth


Photonics

Data Security / Encryption

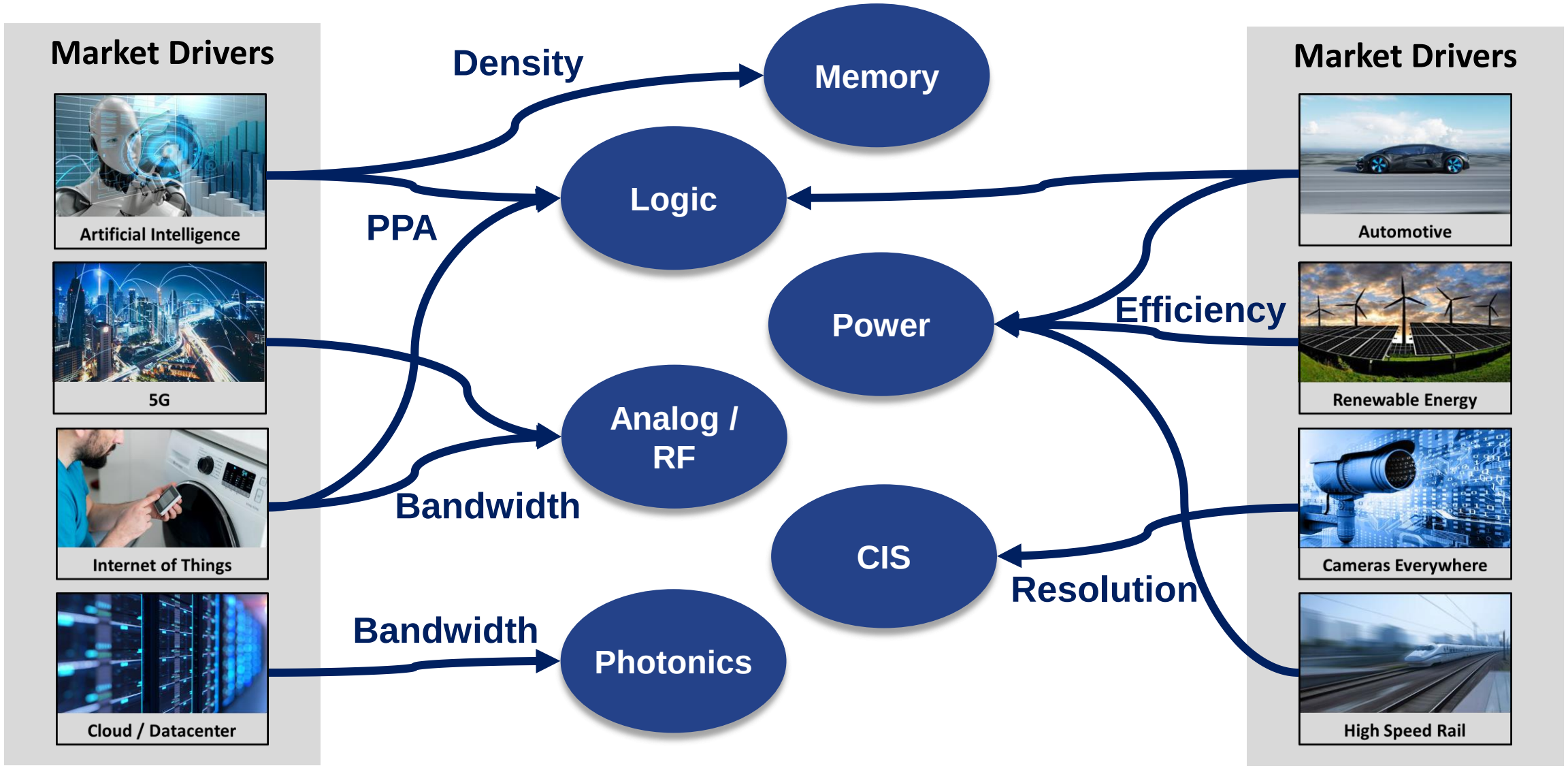
Quantum Computing

System Efficiency



Novel Power Devices

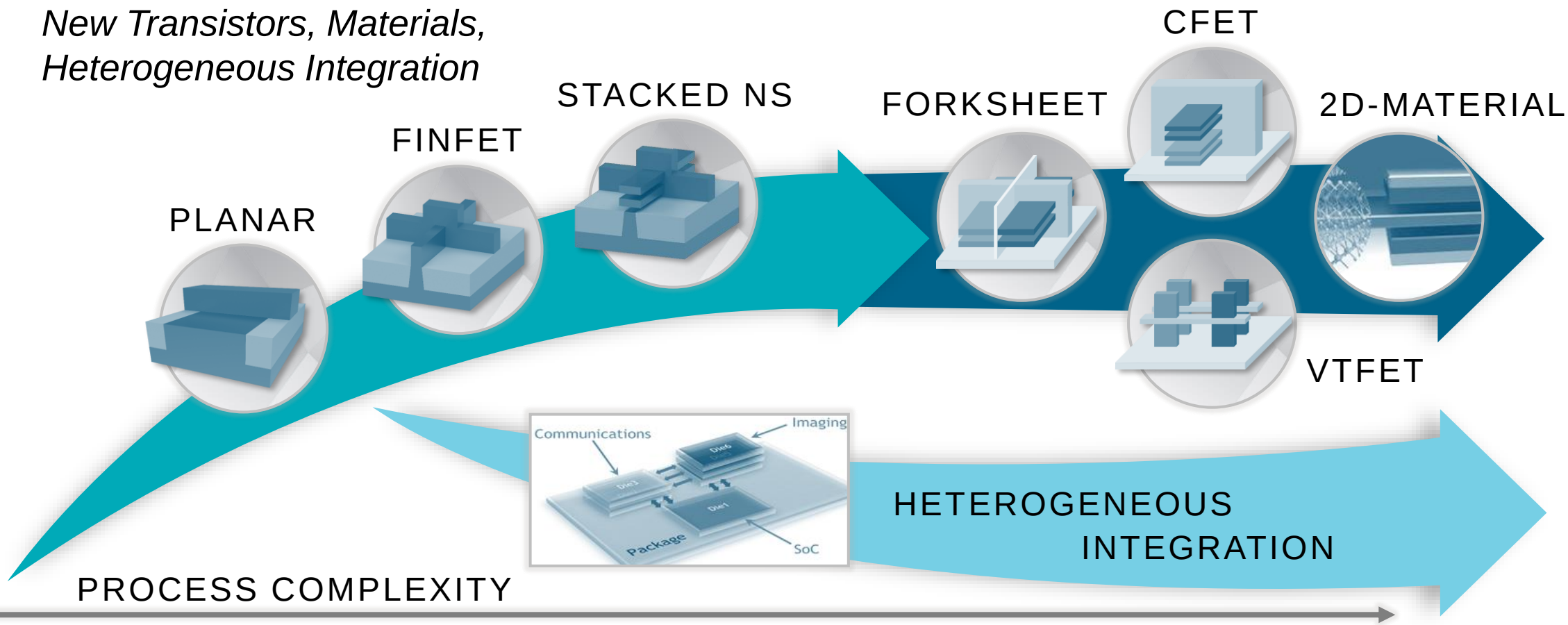
Market Drivers Provide Key Direction for Semiconductor Technology Development



Advanced Logic Roadmap and DTCO

Industry Logic Roadmap Drives Significant Process Complexity, Development Cost and Risk: High Value Problem

New Transistors, Materials, Heterogeneous Integration



Considerable development cost and risk in evaluating and selecting the right logic technology, and in manufacturing it with high yield

Evaluation of Technology Options Requires Design-Level Metrics: Design-Technology Co-Optimization (DTCO)

TECHNOLOGY

- Process Assumptions
- Design Rules
- Process Innovations

DESIGN

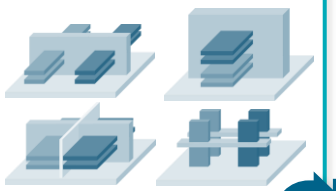
- Std Cell Architecture
- Ring Oscillator
- Block-Level Designs

- Transistor Architecture
- SPICE Models
- MOL / BEOL Stack
- Integration Scheme

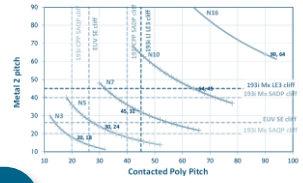
Feedback to Technology

- Downselection of options
- Optimization of options

TRANSISTOR

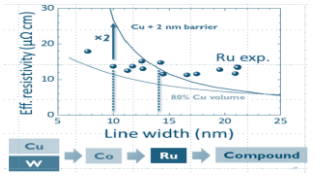


PATTERNING



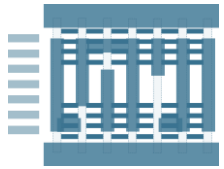
INTEGRATION

NEW MATERIALS

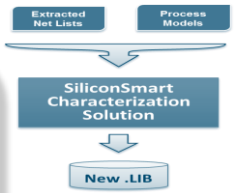


SCALING BOOSTERS MOL / BEOL STACK

STANDARD CELL DESIGN

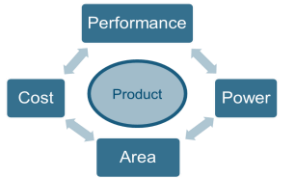


LIB CHARACTERIZATION



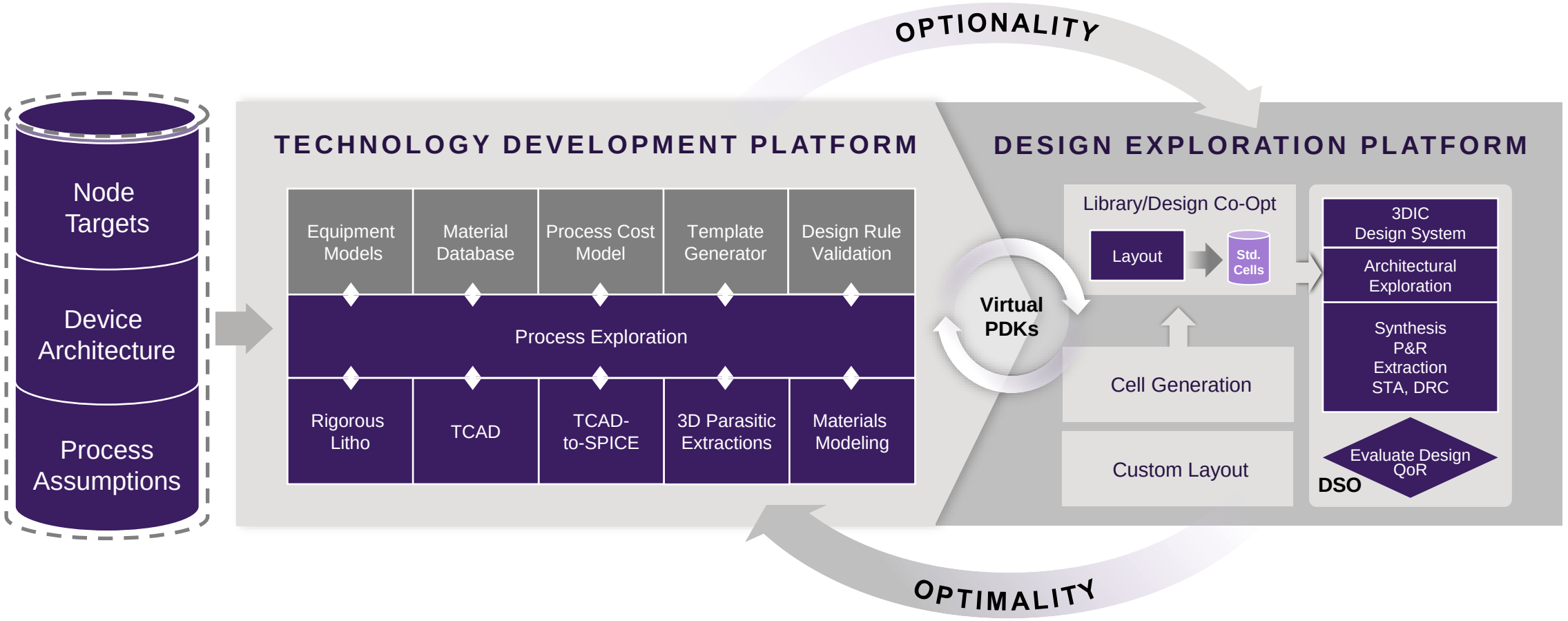
INTEGRATION

PPAC

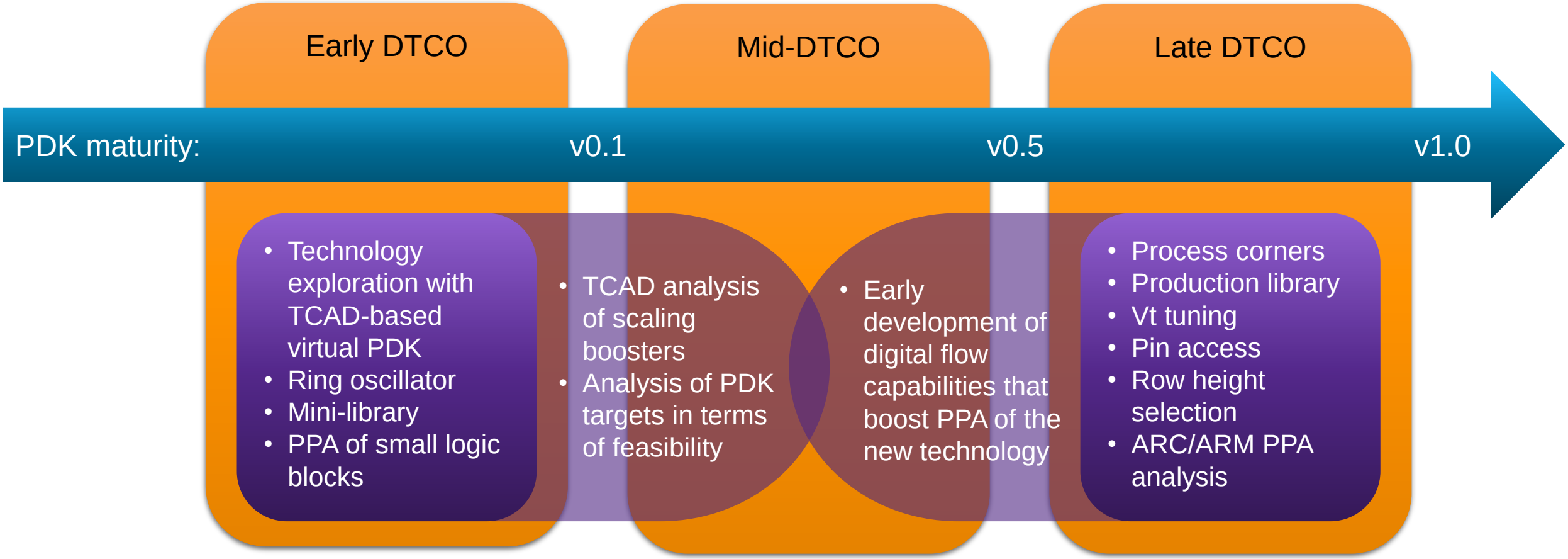


DESIGN

DTCO Platform: *Optionality* in Technology Exploration, *Optimality* in Technology Refinement and Integration



Various Phases of DTCO



Recent DTCO Projects at Leading Logic and Memory Companies

Customers	DTCO Projects
Customer A	Benchmarking logic block PPA for FinFET, CFET, and VFET
Customer A	Quantifying the impact of EUV patterning on logic block PPA
Customer A	Exploring different process integration schemes for BS PDN
Customer A	RO switching in S-Device for FinFETs with fin deformation/bending
Customer B	Benchmarking ring oscillator PPA for FinFET and GAA
Customer B	Optimizing M0 and M1 as a trade-off between logic block and SRAM array
Customer B	Tuning FinFET technology for cryogenic operation at 77 K
Customer C	Optimizing Sense Amplifier for the memory periphery
Customer C	Inserting QuantumATK analysis into logic PPA DTCO flow
Customer C	Pathfinding transistor architecture and process integration for RO on 2D materials
Customer D	Benchmarking GAA and CFET at a logic block PPA
Customer D	Optimizing number of stacked GAA channels at a logic block PPA
Customer D	Inserting QuantumATK analysis into logic PPA DTCO flow
Customer E	Tuning FDSOI technology for cryogenic operation at 4 K
Customer F	Optimizing 3D NAND bitcell for multi-bit storage
Customer G	Optimizing FinFET MOL design rules for specific chip design

Synopsys Publications Demonstrate DTCO Applications in Advanced Logic and Memory

Logic Block Level Design-Technology Co-Optimization is the New Moore's Law (Invited)

Victor Moroz, Xi-Wei Lin, and Thuc Dam
Synopsys, Inc., Mountain View, CA 94043, USA
e-mail: victorm@synopsys.com; phone: 650-584-5458

IEEE EDTM 2020

Invited Paper

***Ab Initio* for Design-Technology Co-Optimization**

Shela J. Aboud*, Joanne Huang, Jonathan Cobb, Tue Gunst, Plamen Asenov, Thuc Dam, Ricardo Borges
Synopsys Inc., Mountain View, CA, USA,

SPIE Adv Litho 2021

Heterogeneous Integration Enabled by the State-of-the-Art 3DIC and CMOS Technologies: Design, Cost, and Modeling

X.-W. Lin[1], V. Moroz[1], X. Xu[1], Y. Gao[1], D. Rennie[2], P. Asenov[3], S. Smidstrup[4], D. Sherlekar[1], Z. Qin[1], T. Fang[5], J. Lee[3], M. Choi[1], and S. Jones[6]
[1]Synopsys, Inc., Mountain View, CA, USA, [2]Synopsys Canada, Mississauga, Canada, [3]Synopsys Northern Europe, Glasgow, UK, [4]Synopsys Denmark ApS, Copenhagen, Denmark, [5]Synopsys Taiwan, Hsinchu, Taiwan, [6]IC Knowledge LLC, Georgetown, MA, USA, email: xiwei@synopsys.com

IEDM 2021

DTCO Launches Moore's Law Over the Feature Scaling Wall

V. Moroz[1], X.-W. Lin[1], P. Asenov[2], D. Sherlekar[1], M. Choi[1], L. Sponton[3], L. S. Melvin III[4], J. Lee[2], B. Cheng[2], A. Nannipieri[3], J. Huang[1], and S. Jones[5]
[1]Synopsys, Inc., Mountain View, CA, USA, [2]Synopsys Northern Europe, Glasgow, UK, [3]Synopsys Switzerland LLC, Zurich, Switzerland, [4]Synopsys, Inc., Hillsboro, OR, USA, [5]IC Knowledge LLC, Georgetown, MA, USA, email: victor.moroz@synopsys.com

IEDM 2020

Simulation-based DRAM Design Technology Co-Optimization: Why Random Dopant Fluctuations Matter

Salvatore Maria Amoroso, Plamen Asenov, Jaehyun Lee, Andrew R. Brown
Synopsys Northern Europe Ltd., Glasgow, G3 8HB, Scotland, UK

Xi-Wei Lin, Victor Moroz
Synopsys Inc, Mountain View, CA 94043, USA

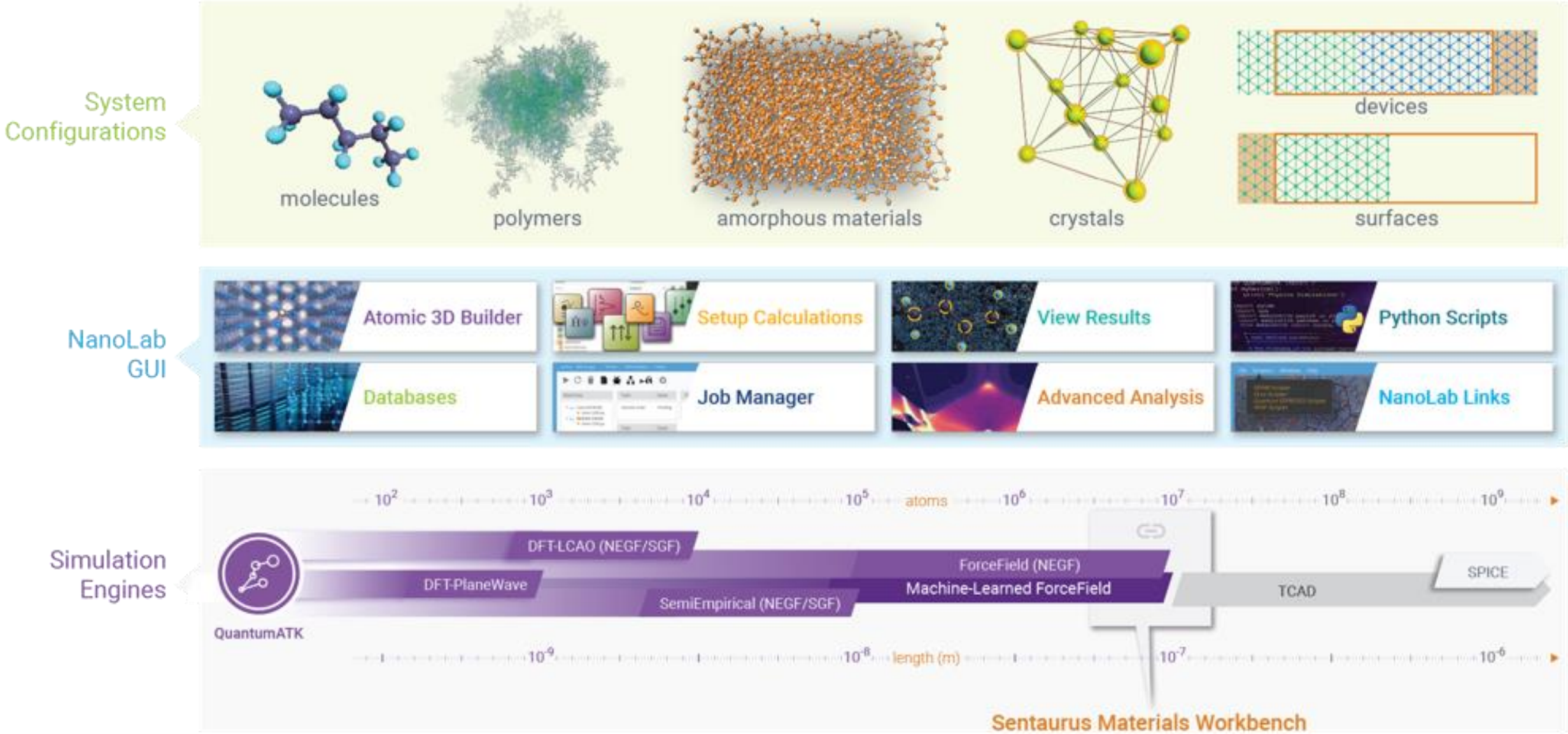
Ethan Kao
Synopsys Taiwan Ltd., Hsinchu, Taiwan

SISPAD 2021

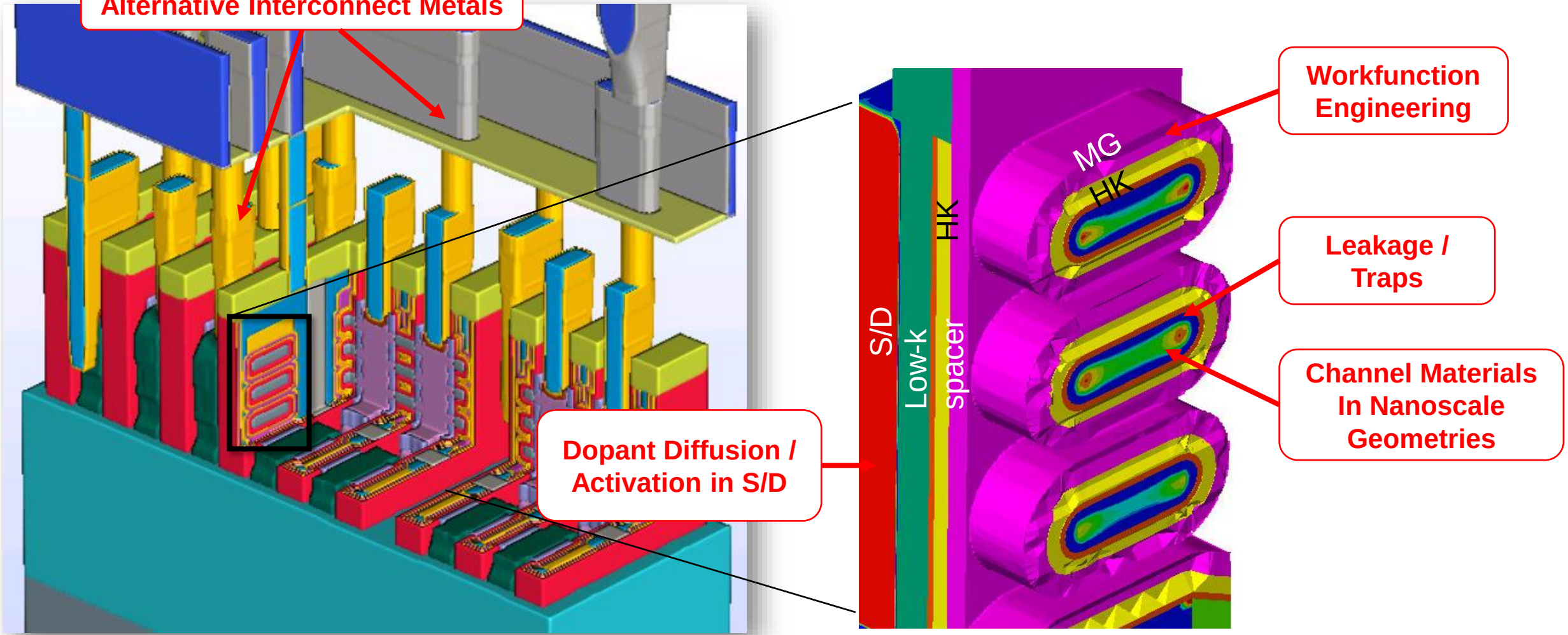
Materials Modeling in DTCO

QuantumATK

Atomistic Simulation Tool

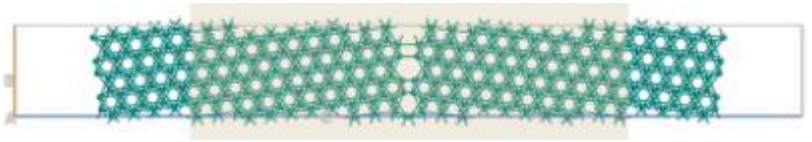


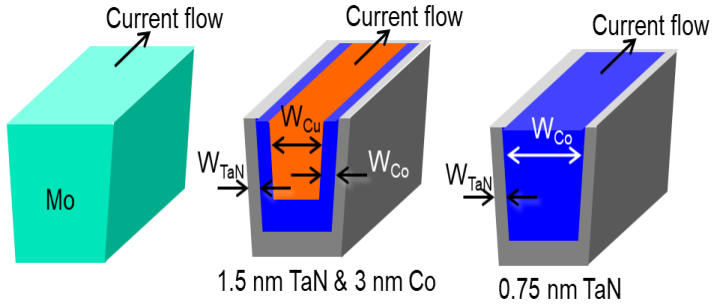
Materials Modeling: Many Opportunities for Integration and Optimization in Advanced Semiconductor Development

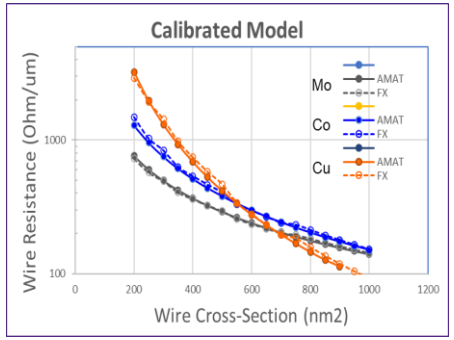


Ab initio Material Engineering

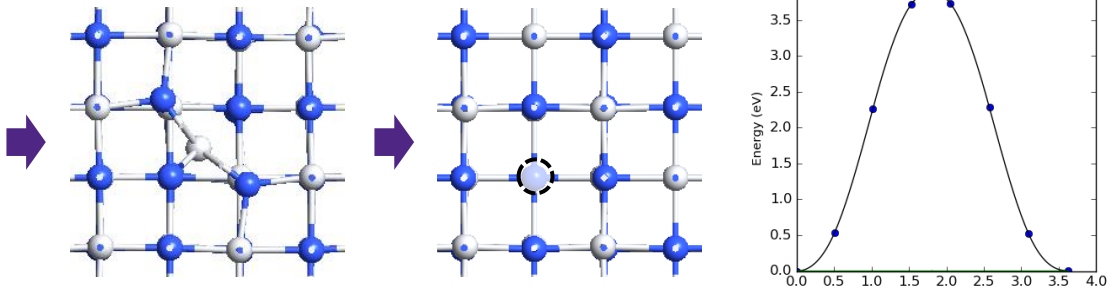
Electron scattering at grain boundaries in narrow wires

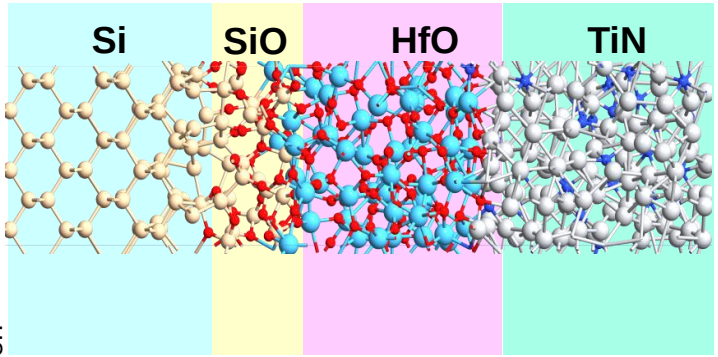


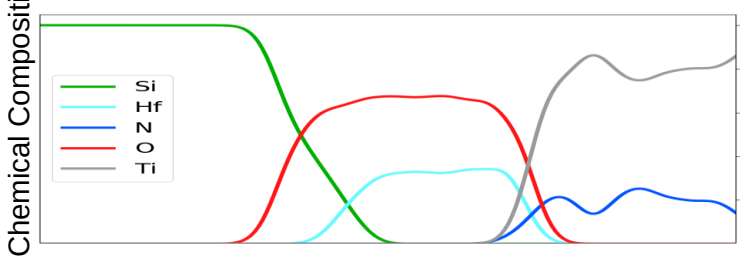


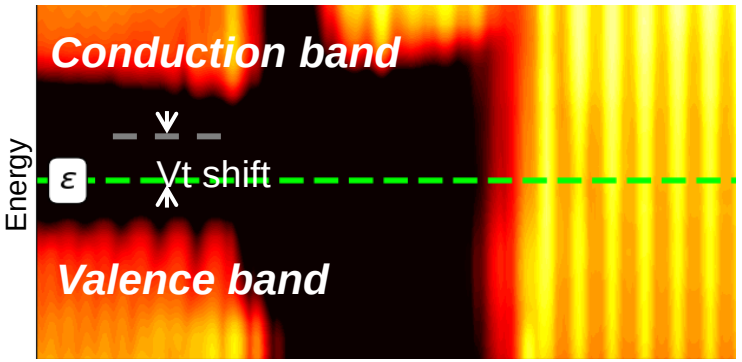


Defect Diffusion







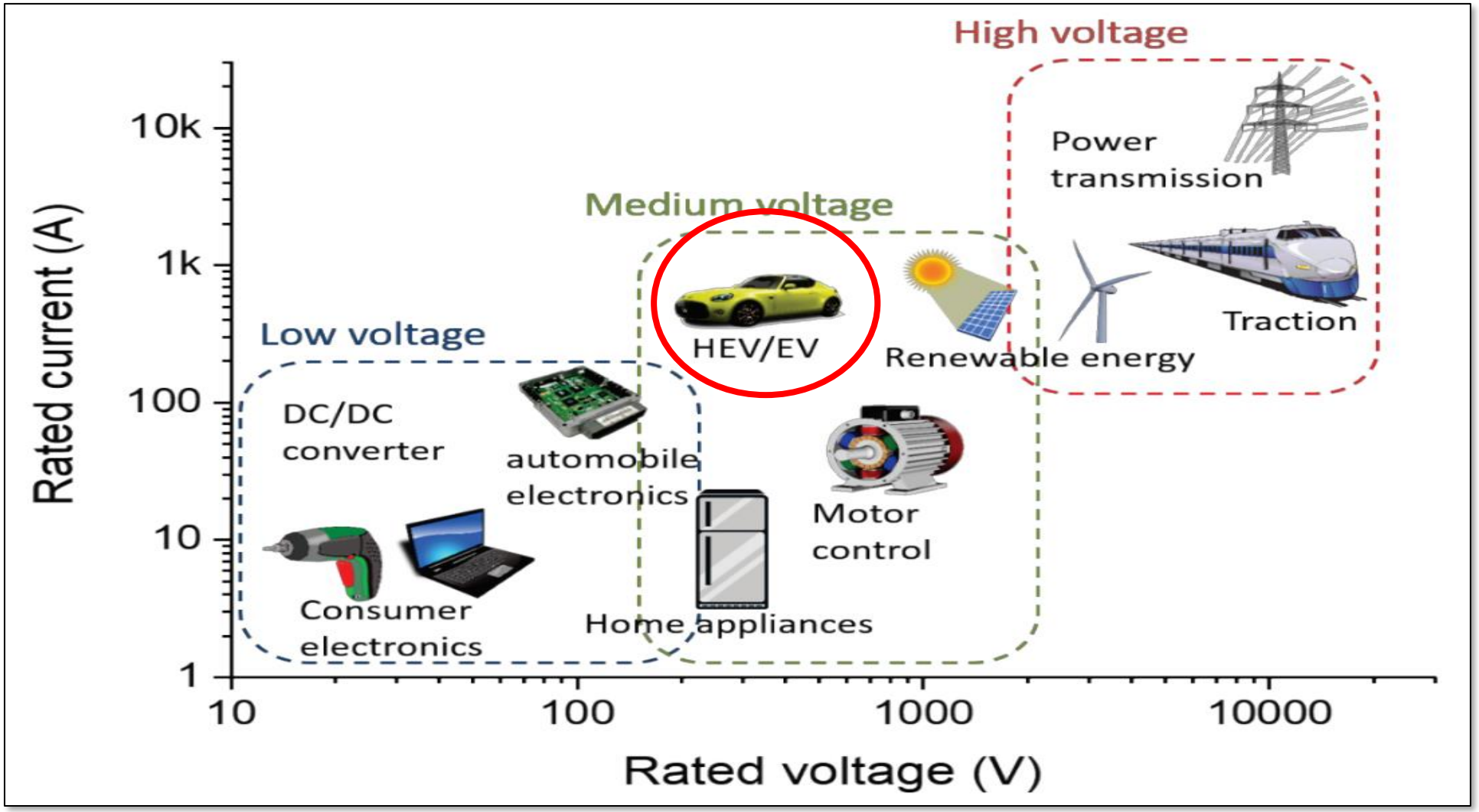


HKMG stack engineering:

- Threshold Voltage
- Leakage
- Remote Coulomb scattering

DTCO for Power Electronics Application

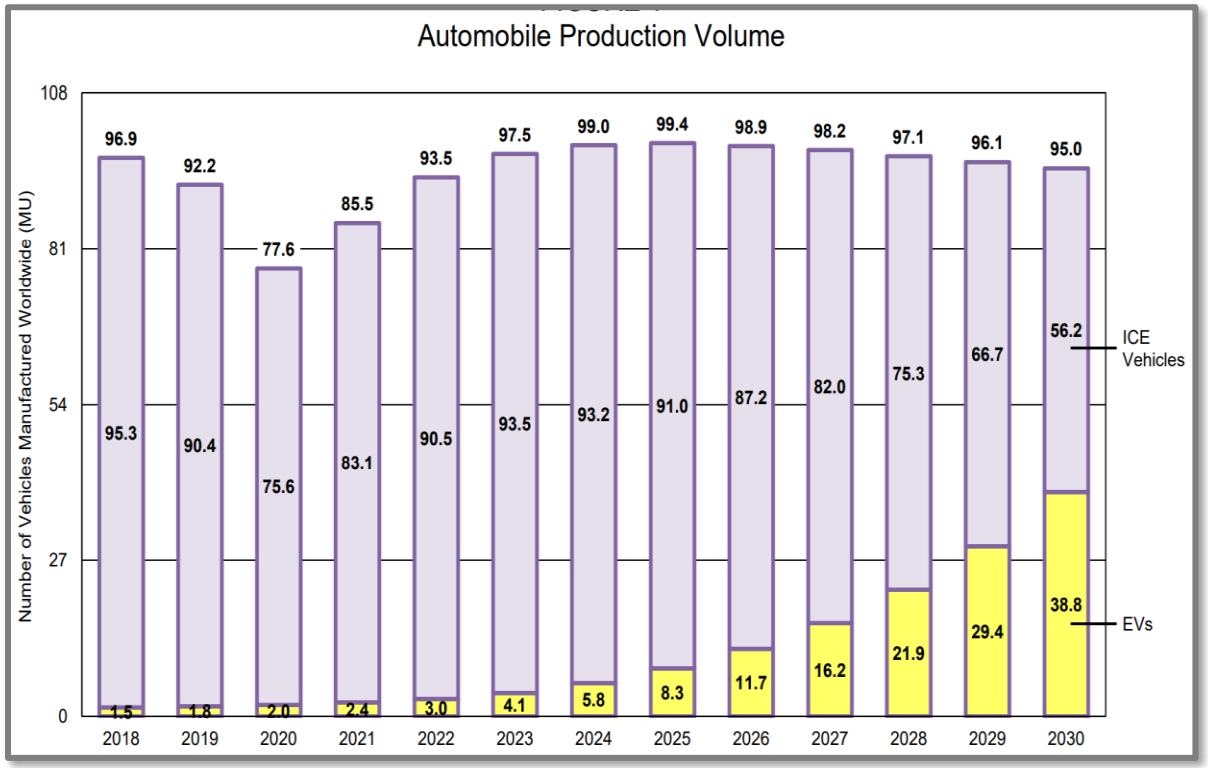
Power Electronics Applications Cover A Wide Range of Voltage and Current Ratings Across Many Applications



Source: Victor Soler Dissertation, Universitat Politecnica de Catalunya, 2019

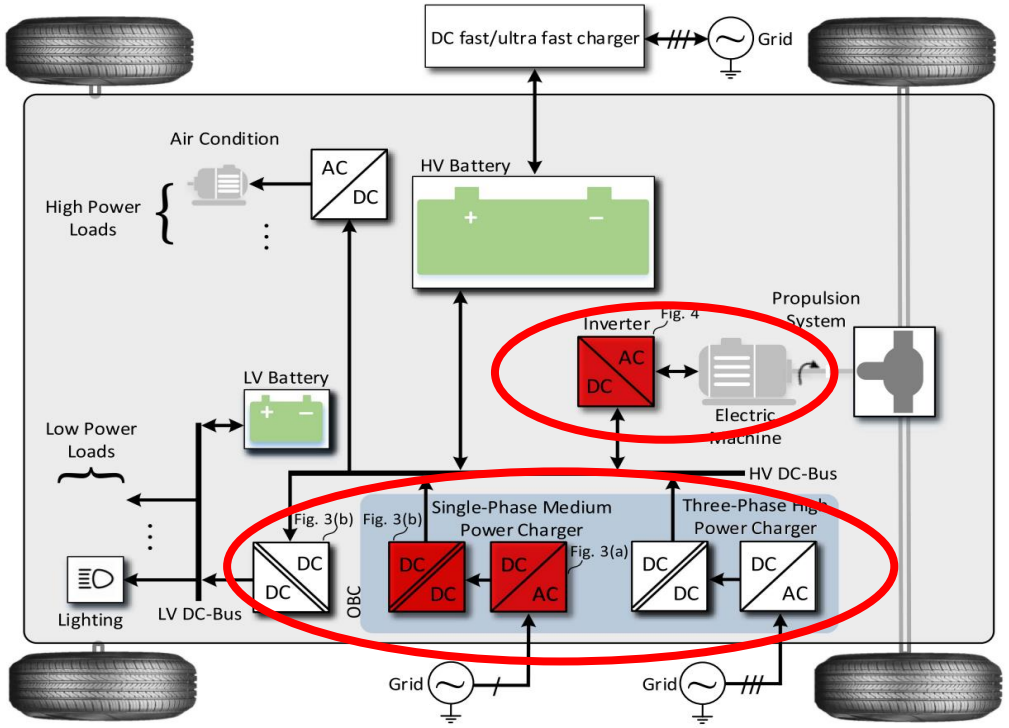
EV Deployments Drive Growth in Power Electronics Sub-Systems: DC/DC Converters, DC/AC Inverters

Electric Vehicles Are Projected to Comprise 38% of Automotive Fleet by 2030



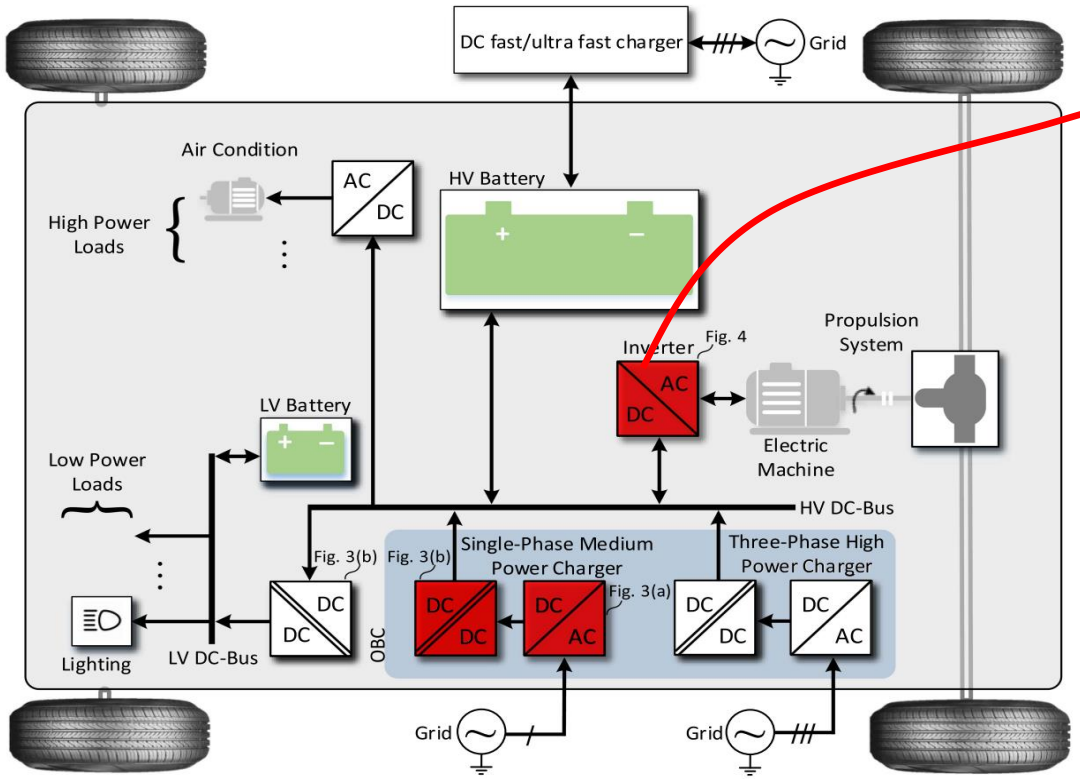
Source: IBS Global Semiconductor Industry Service Report, Automotive Electronics

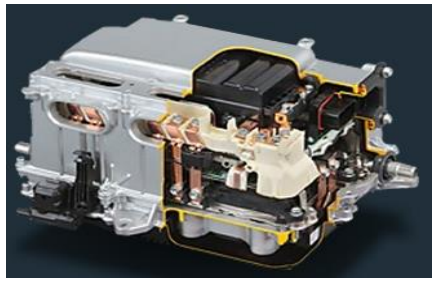
High Efficiency Power Conversion Sub-Systems Are Critical for EV Performance



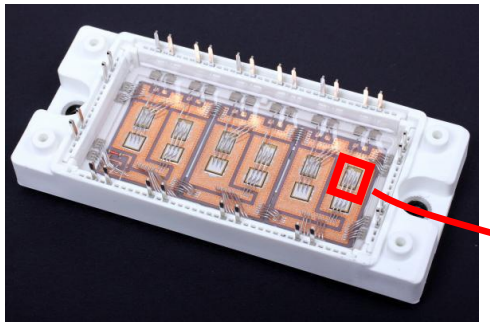
Source: Blaabjerg et al, Proc IEEE, **109**, No 6, June 2021

SiC and GaN Power Transistors Are an Enabling Technology for Electric Vehicle Sub-Systems



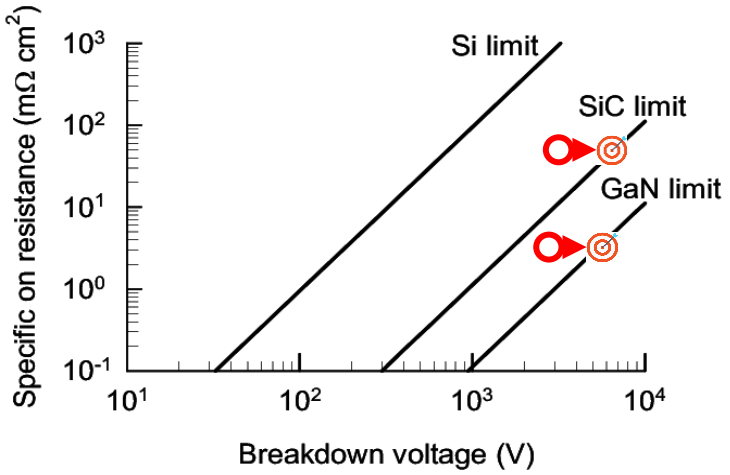


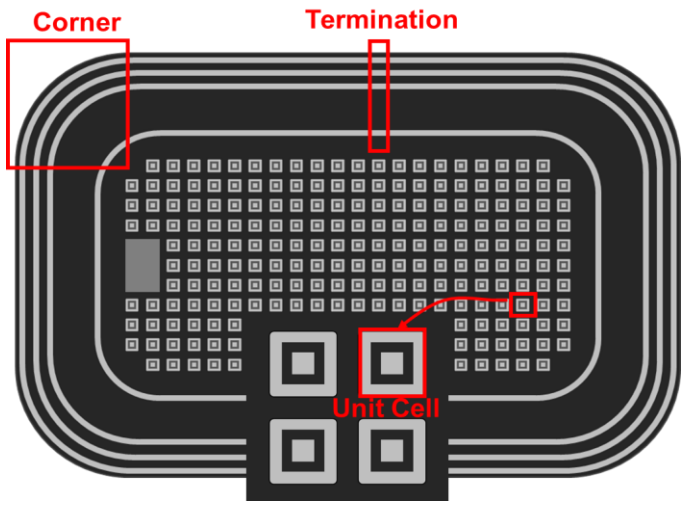
Sub-system (Inverter, Converter)



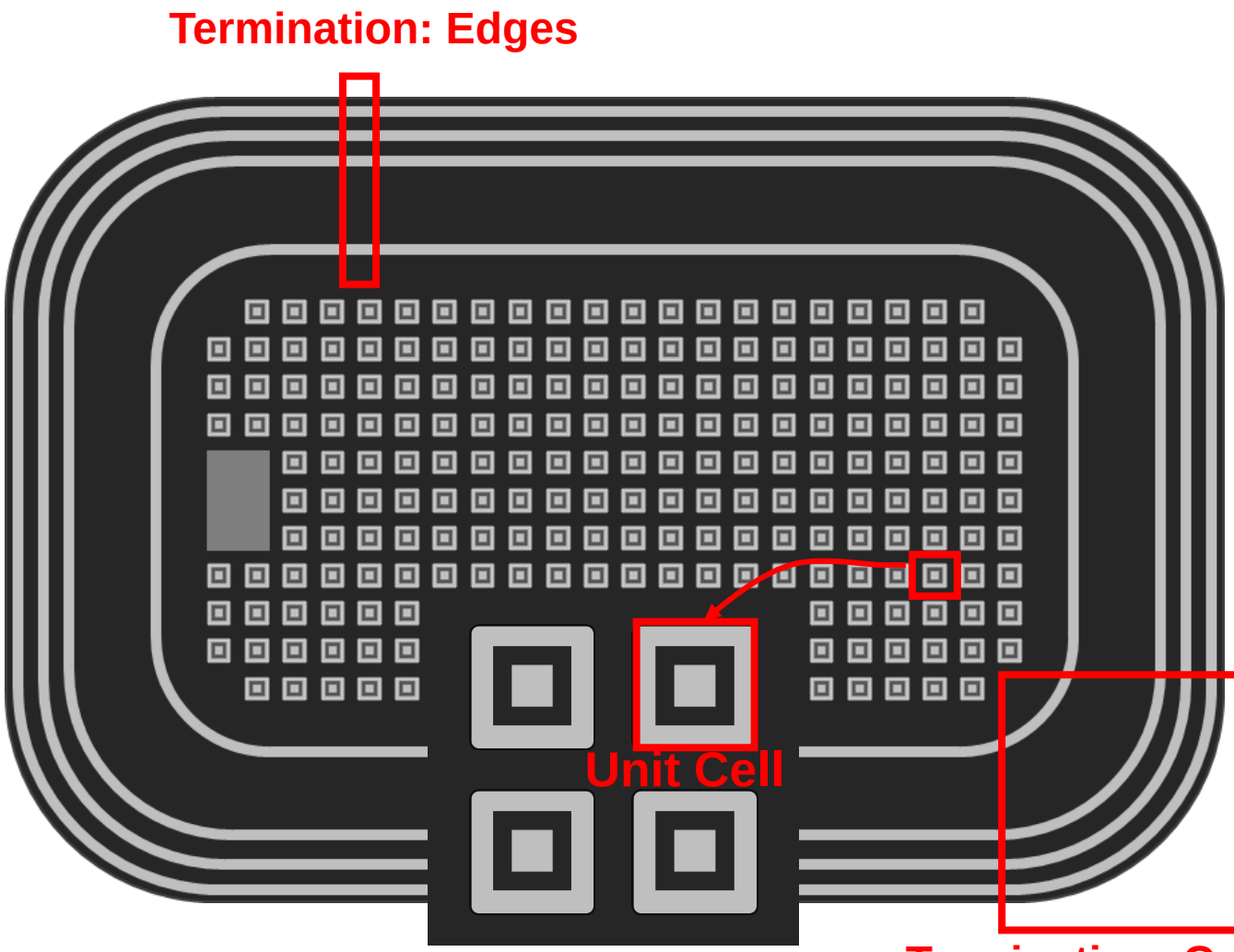
Power Module

SiC and GaN power transistors have not yet achieved full potential





Power Transistors Are Made Up of Thousands of Unit Cells With Termination Structures in the Periphery

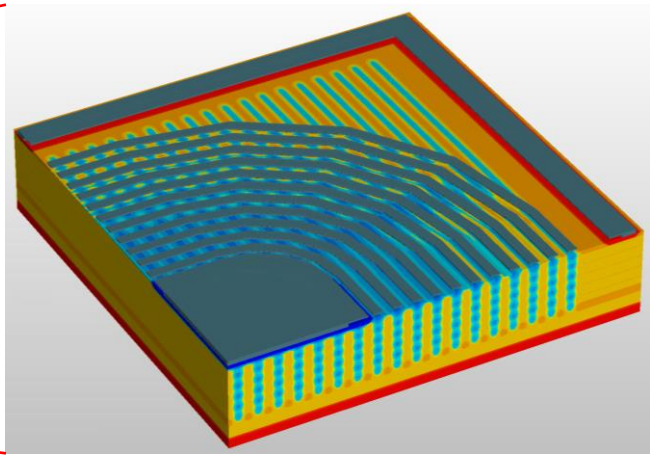


Optimization of Power Transistor performance metrics:

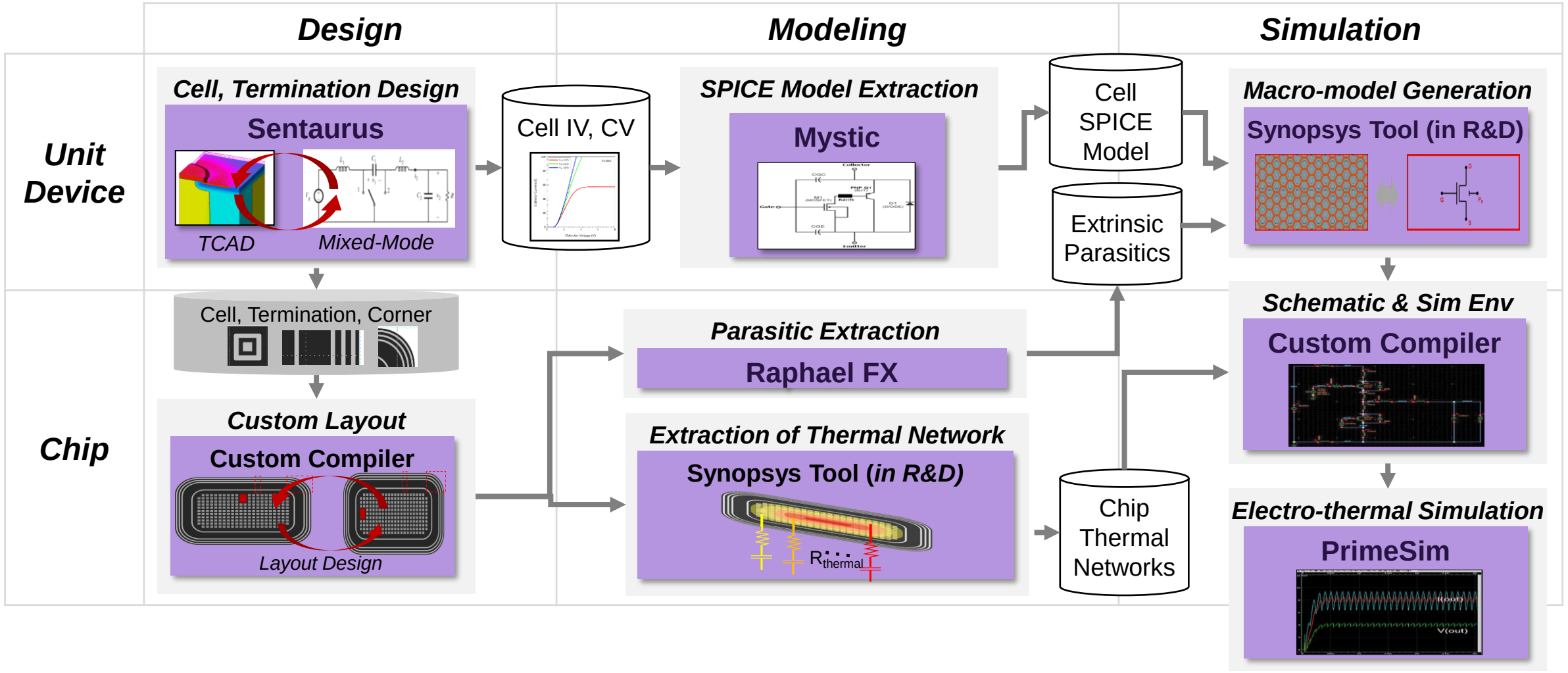
- High blocking voltage
- Low on-state loss
- High current
- High reliability

requires co-design and optimization of **Unit Cell**, **Termination, Corner** and **Layout** of the components

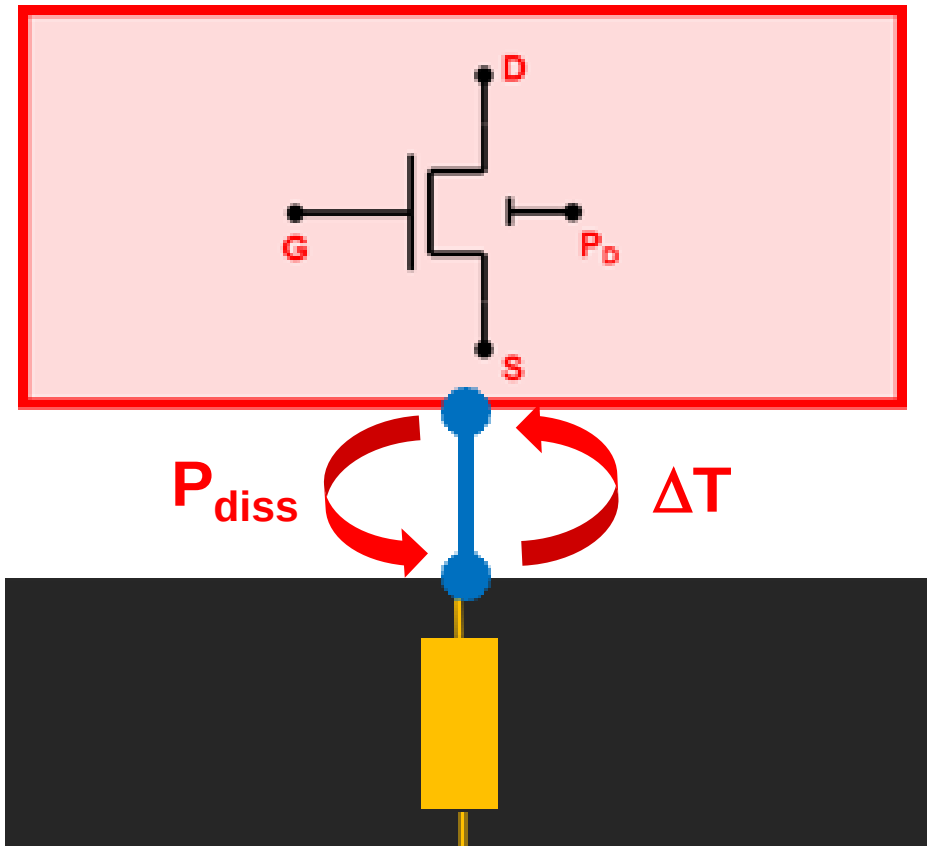
Termination design requires large scale TCAD simulations

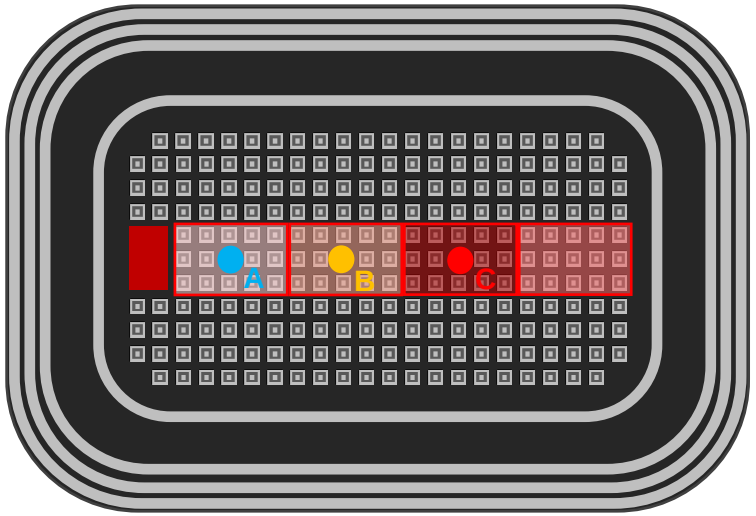


Synopsys Power Chip Design Flow



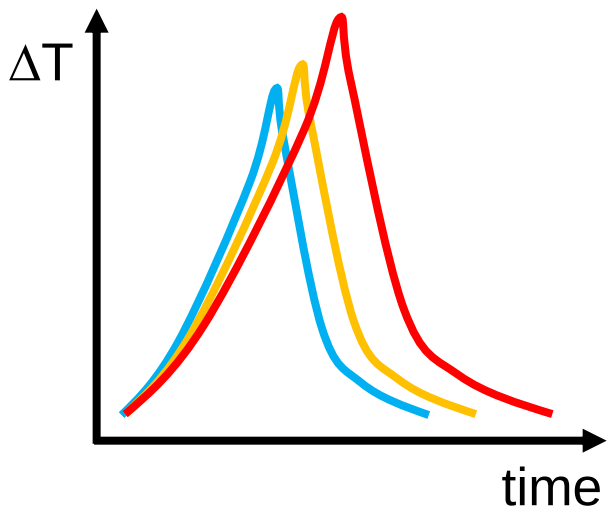
Electro-thermal Simulation is Solved Self-Consistently and Generates Data for Visualization of Power Chip Performance

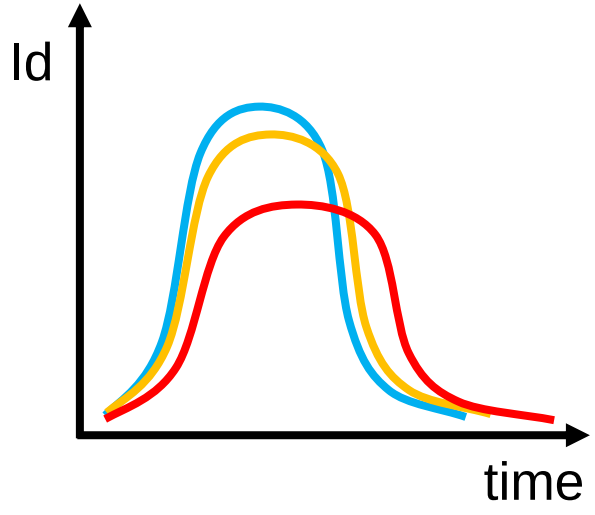




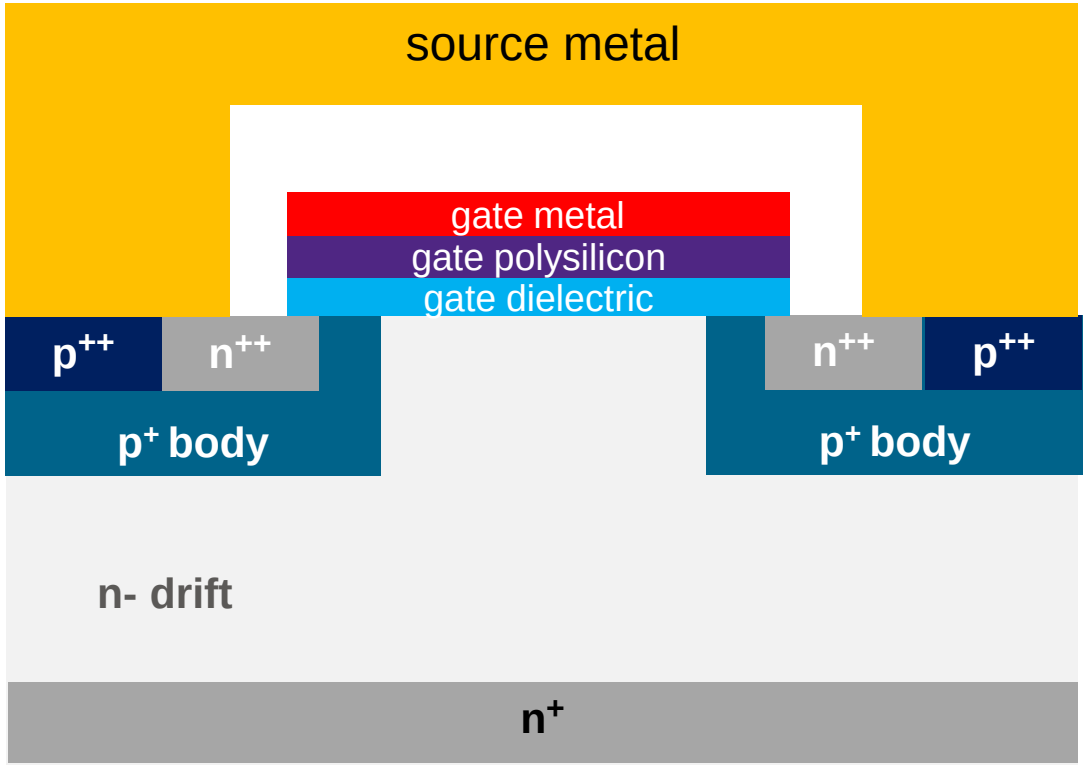
Chip Maps:
- Temperature
- Current Density
- …

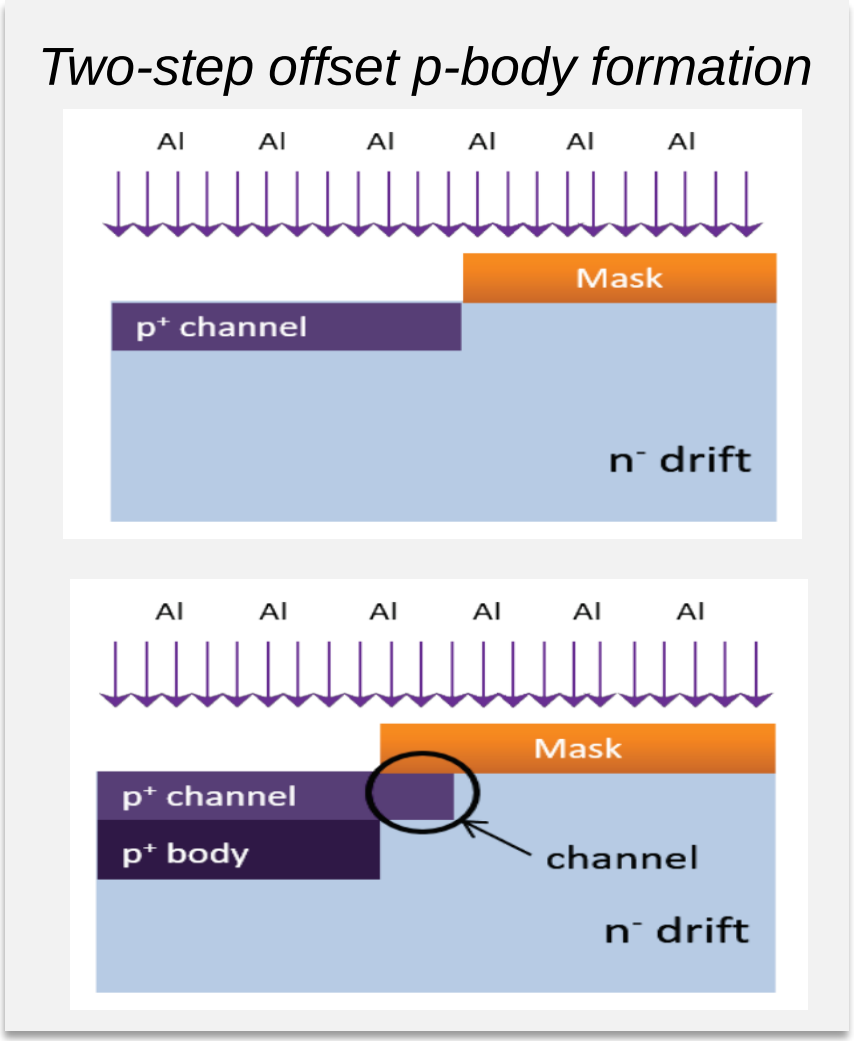
Probing of user-defined locations within chip





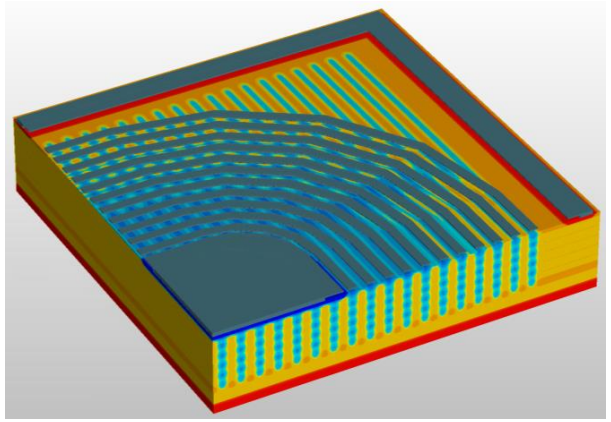
Al Implantation in SiC is Used to Form the p+ Body and Channel Regions in Modern SiC MOSFETs



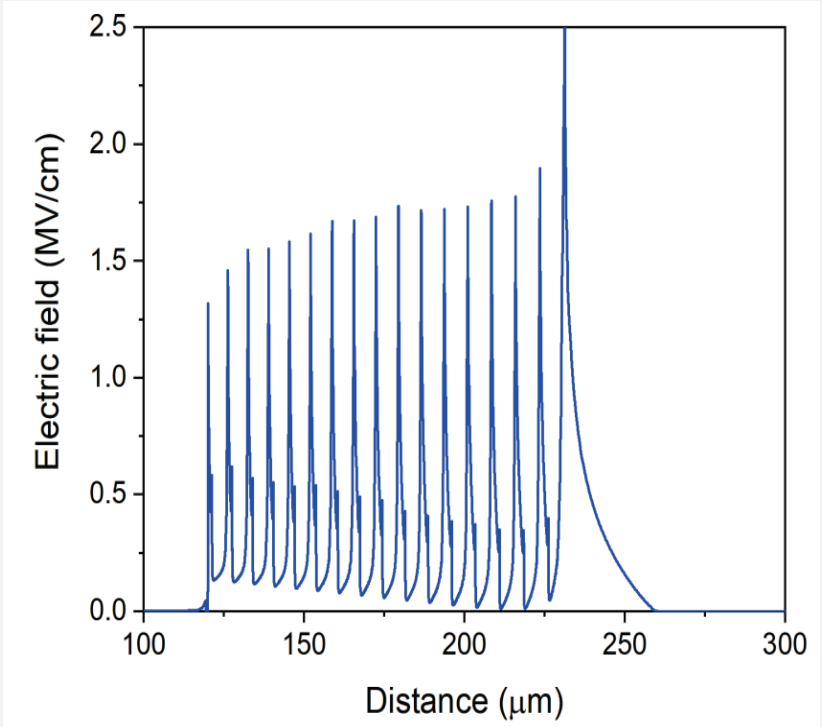


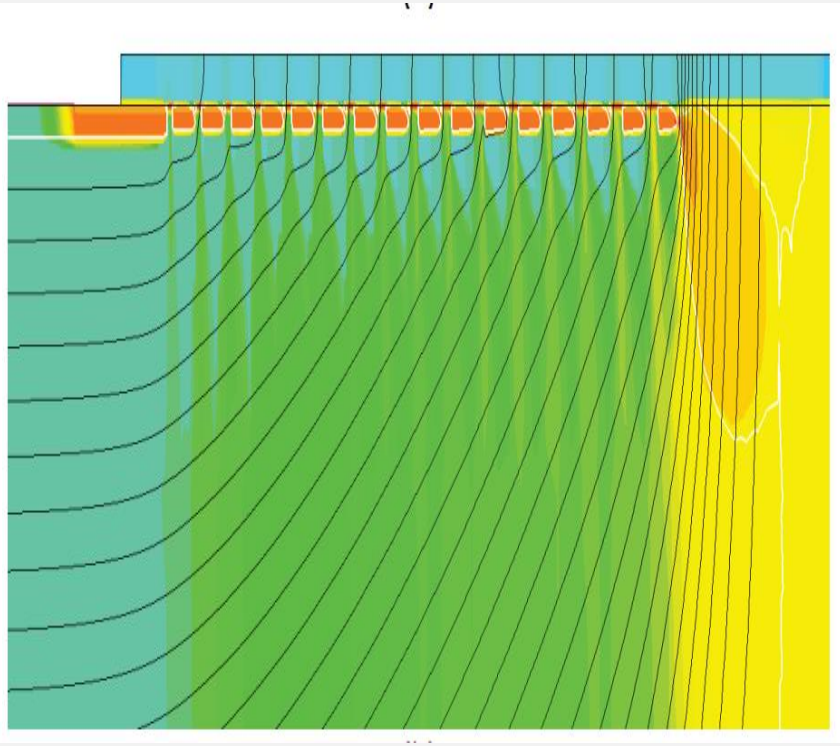
Source: Victor Soler Dissertation, Universitat Politecnica de Catalunya, 2019

… Increasingly Al Implantation in SiC is Also Used in Termination Structures Targeting Very High Blocking Voltage Devices



Simulation of Edge Termination Scheme with 16 Rings, Targeting 6.5 kV-rated SiC Power Devices





Source: Victor Soler Dissertation, Universitat Politecnica de Catalunya, 2019

GaN RF and Power Electronics Devices Require Mg Implantation for Termination Design

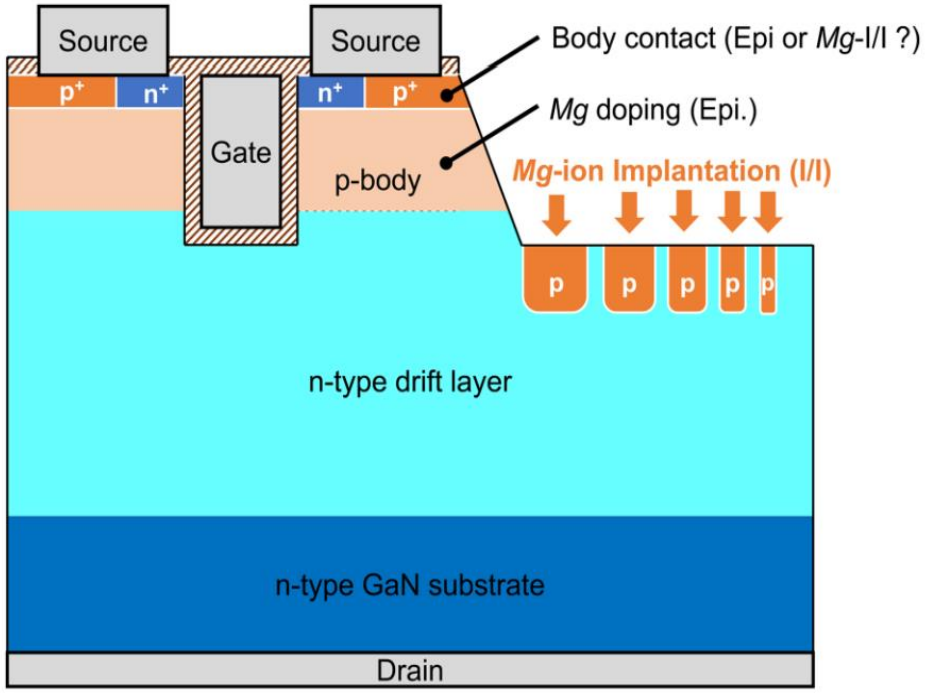


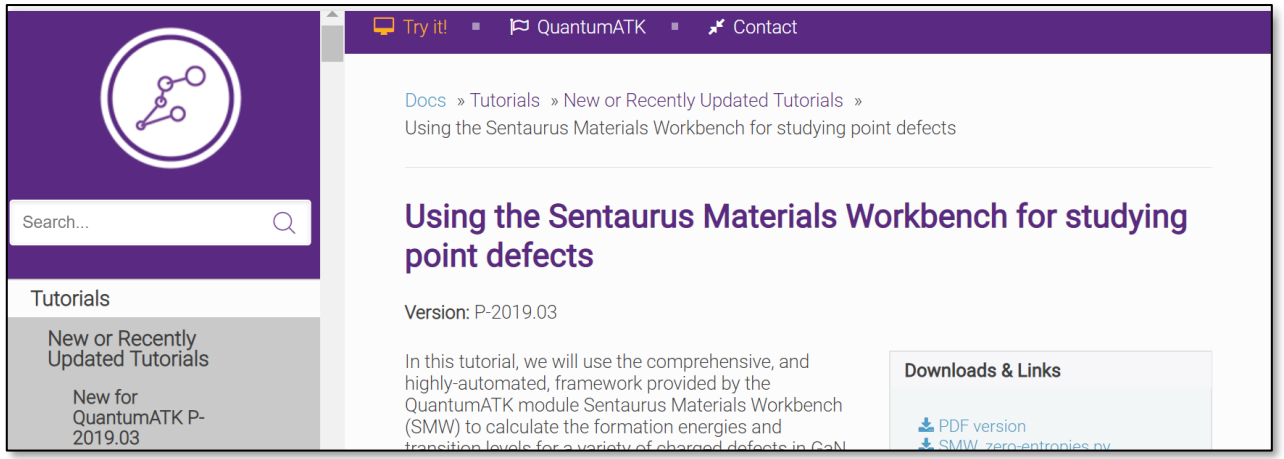
FIG. 1. Cross-sectional schematic of a T-MOSFET. A p-type body layer uniformly doped with Mg below 10^{18} cm^{-3} can be formed by the MOVPE method. Selective-area doping for the edge termination will be achieved by Mg ion implantation. The p^+ body contact can be formed by either MOVPE growth or Mg ion implantation.

Progress on and challenges of p-type formation for GaN power devices

Cite as: J. Appl. Phys. **128**, 090901 (2020); https://doi.org/10.1063/5.0022198
Submitted: 20 July 2020 • Accepted: 14 August 2020 • Published Online: 02 September 2020

Tetsuo Narita, Hikaru Yoshida, Kazuyoshi Tomita, et al.

https://docs.quantumwise.com/tutorials/smw_defects/smw_defects.html



QuantumATK: Defects and Diffusion Analyzer

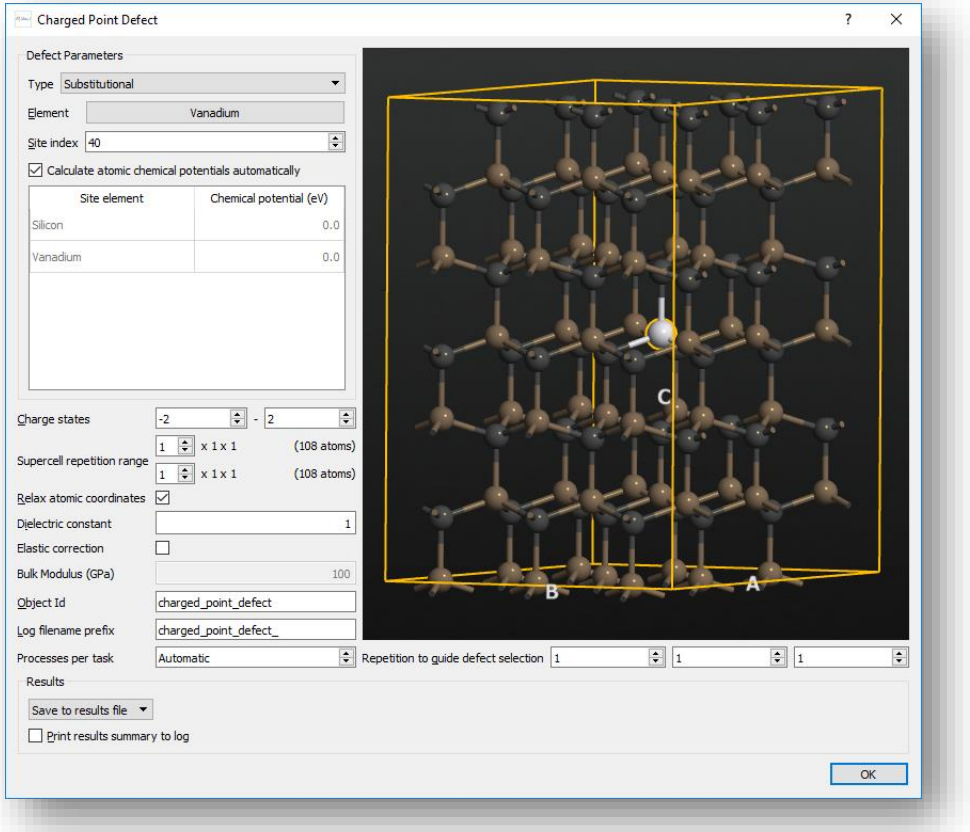
Defect and Dopant Simulations with QuantumATK

Types of defects/dopants

- Vacancies
- Substitutional
- Interstitials
- Pairs
- Complex clusters
- Bulk and interfaces
- Crystal and amorphous
- Large systems

Defect/Dopant properties

- Defect formation energies/entropies
- Defect trap levels
- Dopant-defect binding energies
- Defect migration energies/entropies
- Dominant charge states for diffusion
- Diffusivity

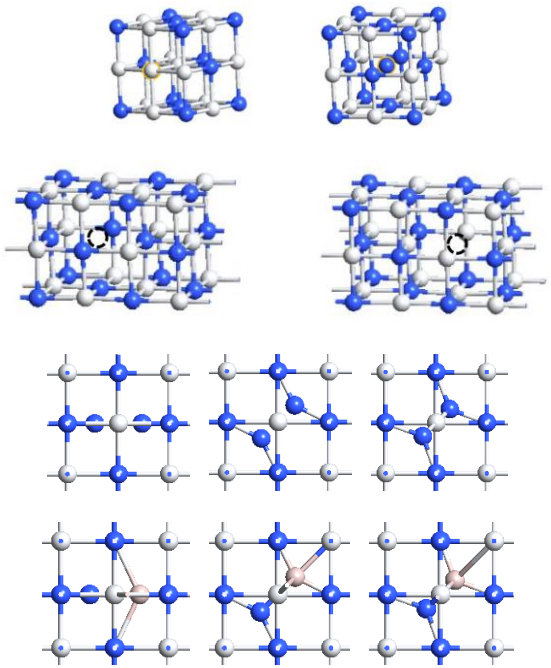


Simulation set-up and result analysis using
GUI and Python scripting

Simulation Flow of Sentaurus Materials Workbench

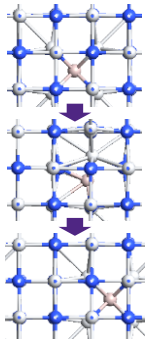
Defect Structure Generations

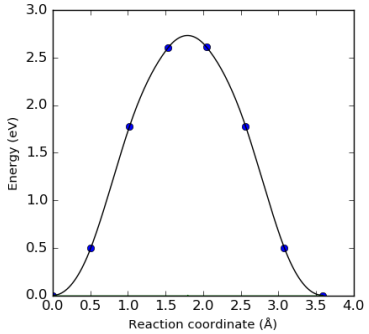
- Generate neutral or charged defects



Diffusion Parameter Calculations

- Defect formation energies/entropies
- Defect migration energies/entropies
- Dopant-defect binding energies
- Dominant charge states for diffusion

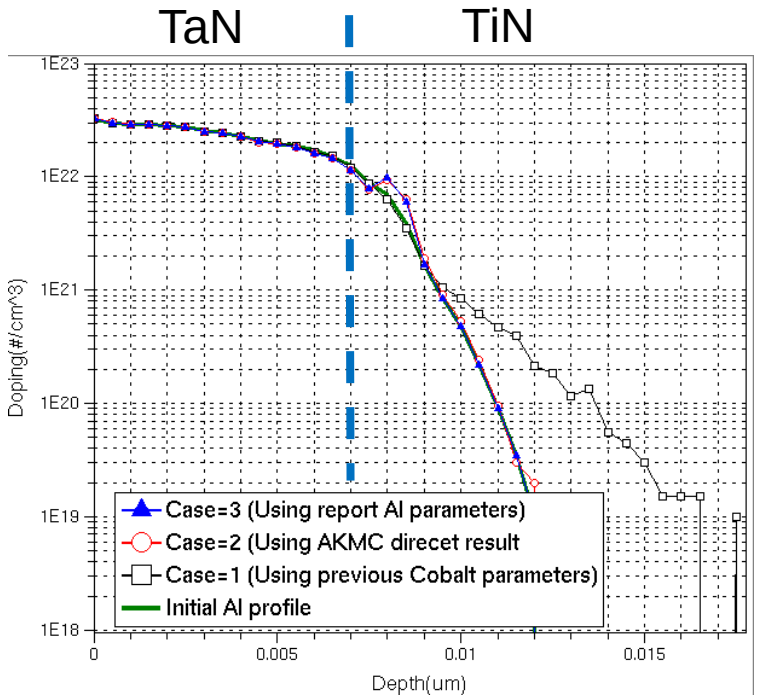





```
# Generated by Sentaurus Materials Workbench
pdbSet TitaniumNitride KMC Int Ef   5.49949
pdbSet TitaniumNitride KMC Int D0FS 0.305367
pdbSet TitaniumNitride KMC Vac Ef   0.635662
pdbSet TitaniumNitride KMC Vac D0FS 0.672997
pdbSetDoubleArray TitaniumNitride KMC Vac Em {
            V  3.61063
}
```

S-Process Simulations

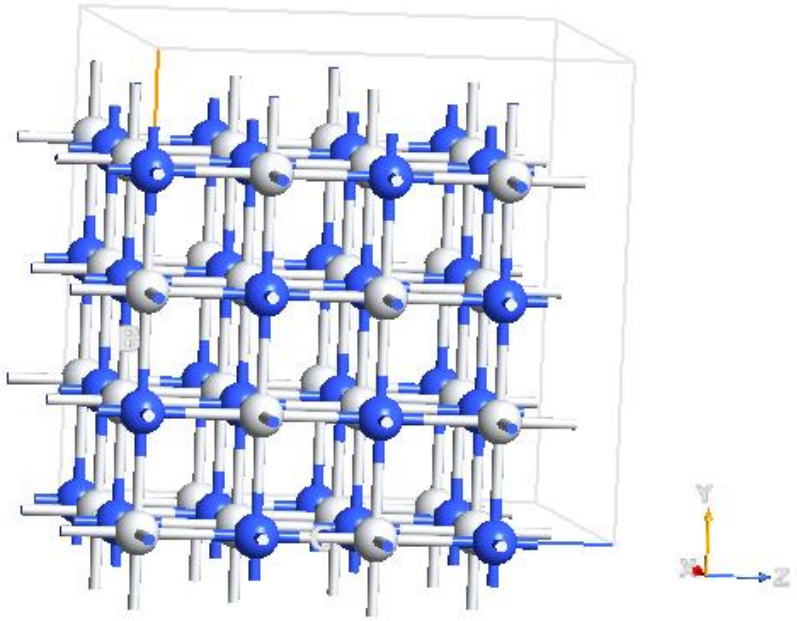
- Dopant concentration profile simulated with S-process KMC



An automatic process with QuantumATK's Sentaurus Materials Workbench

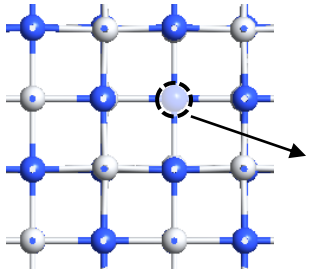
Defect Diffusion Example

- TiN Structure

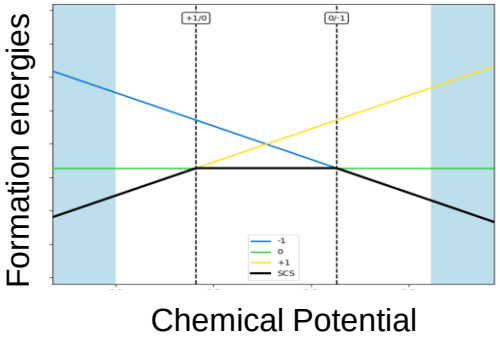


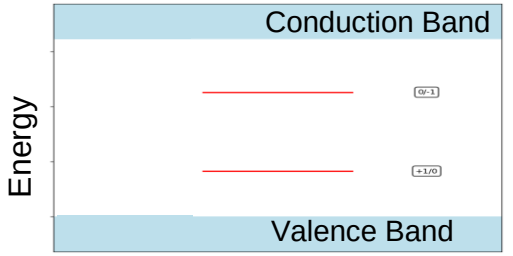
2x2x2 unit cells (64 atoms)
Rock salt structure (space group: 225)

- Diffusion Process
  - Defect formation

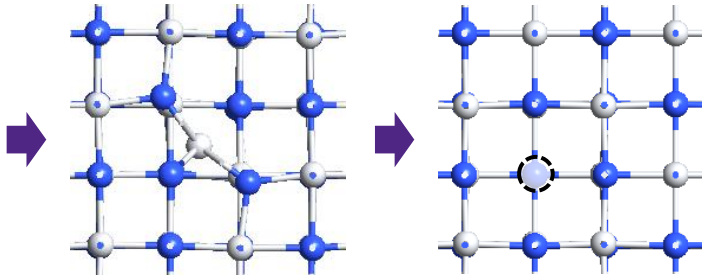


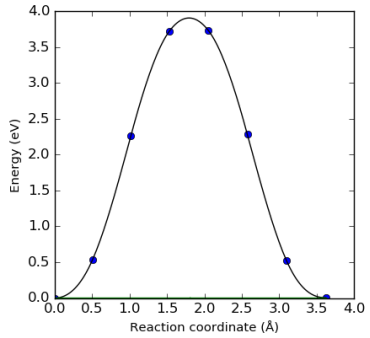
Ti vacancy





  - Defect migration

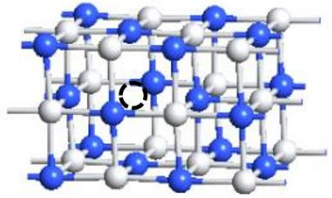




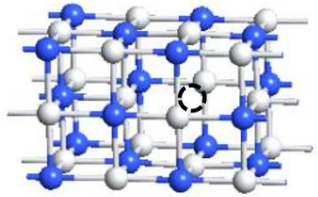
Defects in SMW

- Vacancy

Ti vacancy

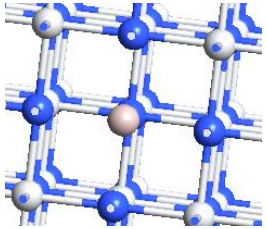


N vacancy

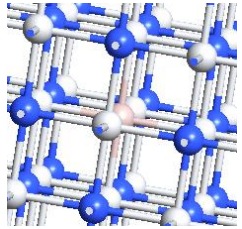


- Substitutional

Al_{Ti}

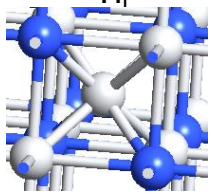


Al_N

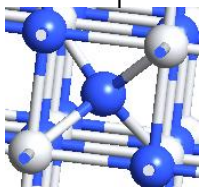


- Interstitial

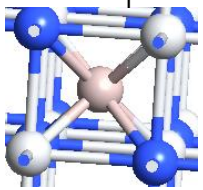
Ti_i



N_i

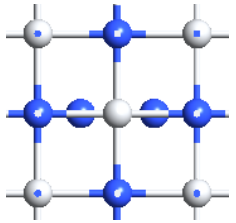


Al_i

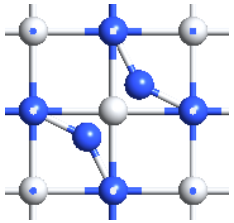


- Split interstitial

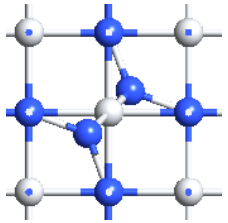
NN S100



NN S110

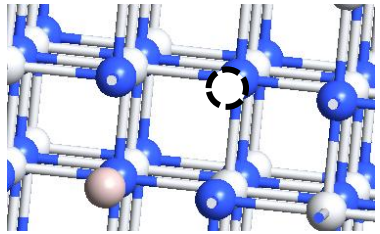


NN S111

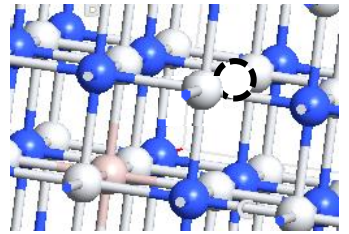


- Defect pair

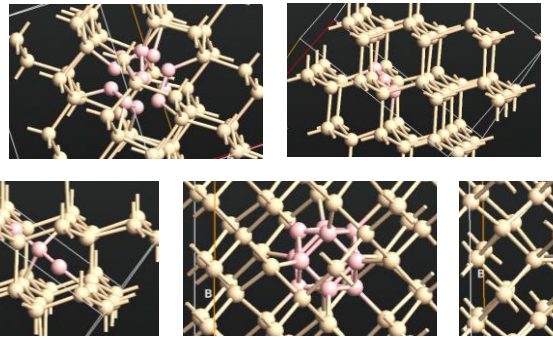
$Al_{Ti} + V_{Ti}$



$Al_N + V_N$



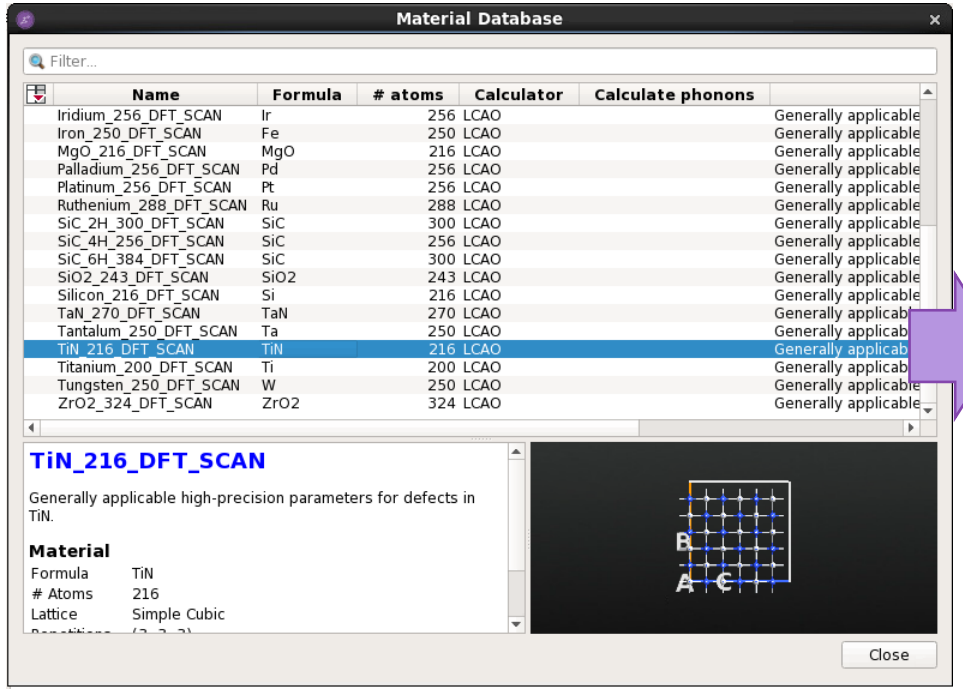
- Cluster

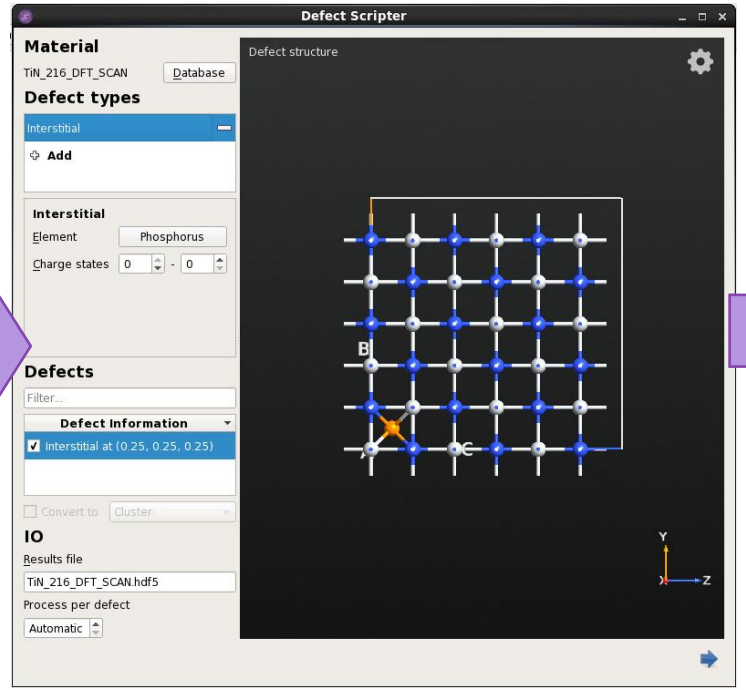


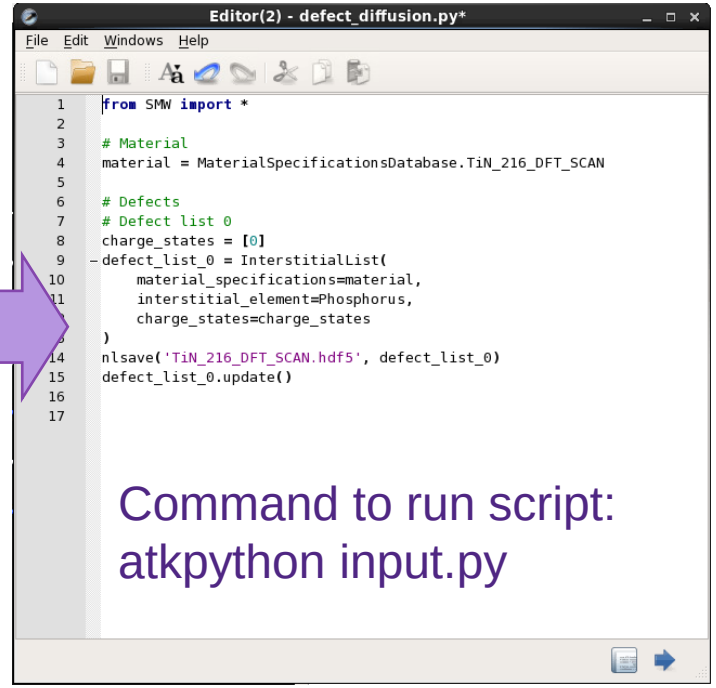
Define Reference Structure

From MaterialDatabase

- Select a reference material from Material Database, define the defects with Defect/Diffusion Scripter, and then run the script.



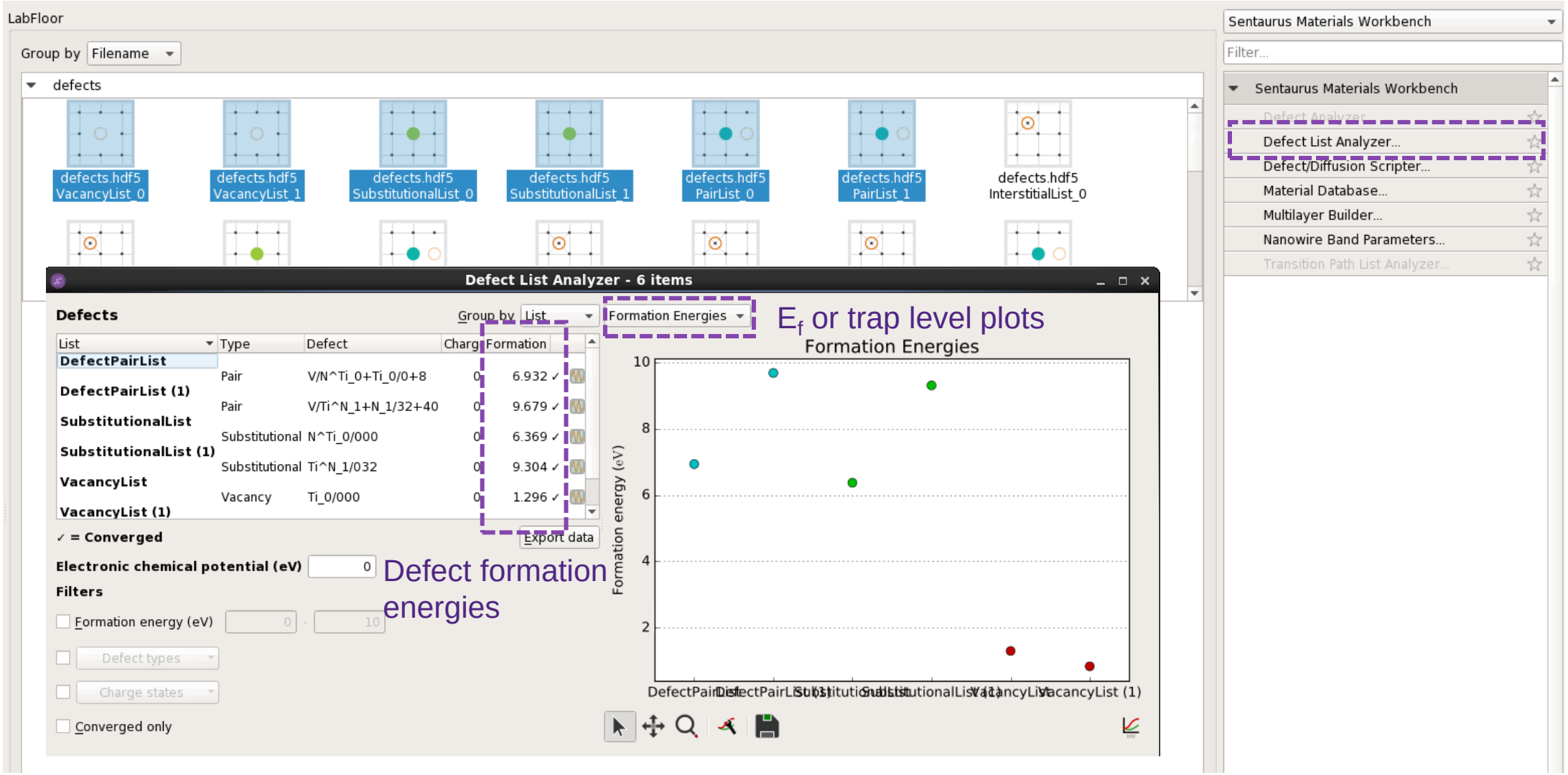




Command to run script:
atkpython input.py

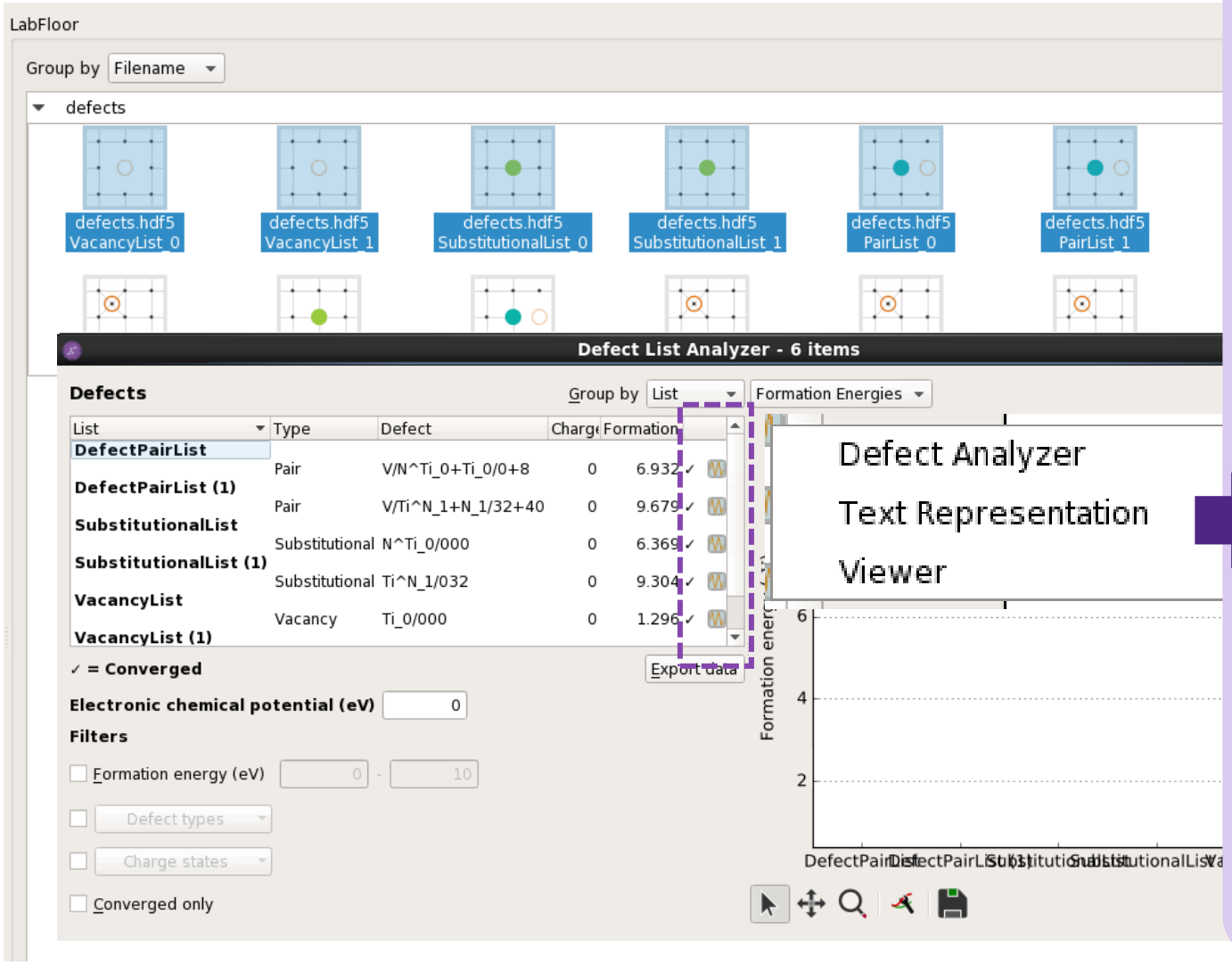
Visualize Defect Information with Defect List Analyzer

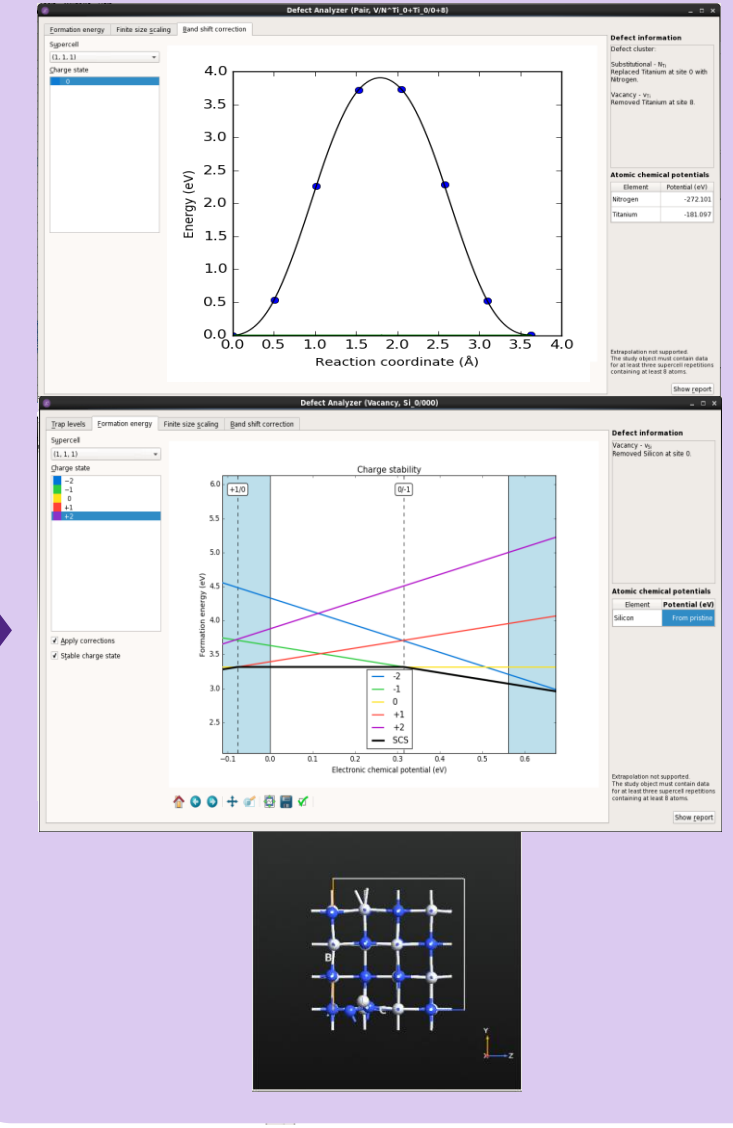
- Open defect list with Defect List Analyzer



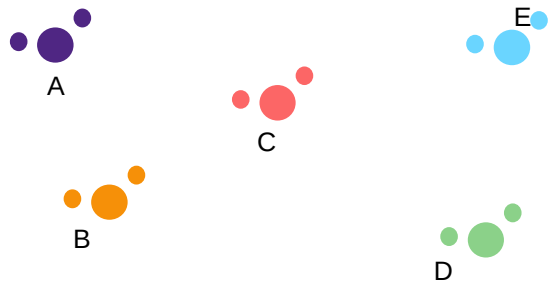
Visualize Defect Information with Defect List Analyzer

- Open defect list with Defect List Analyzer

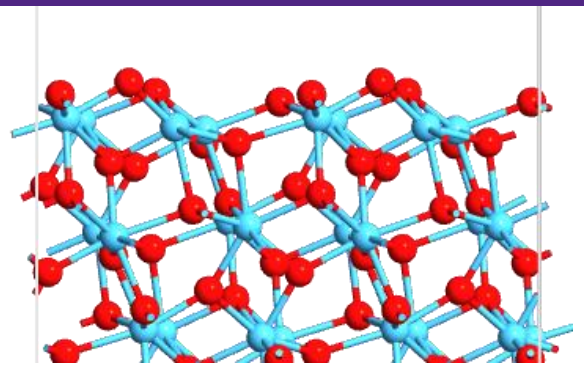




QuantumATK for Surface Reactions: Thermodynamics and Kinetics

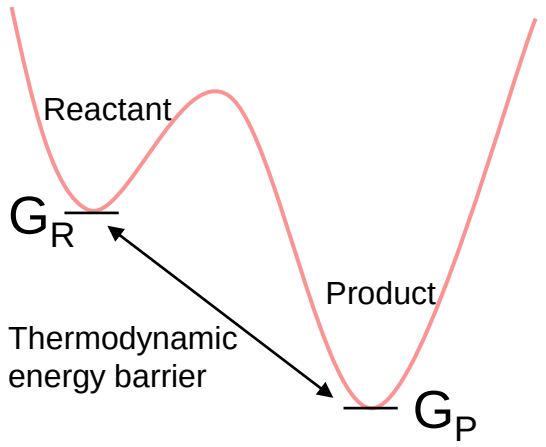


Which reactants and process conditions to



Substrate

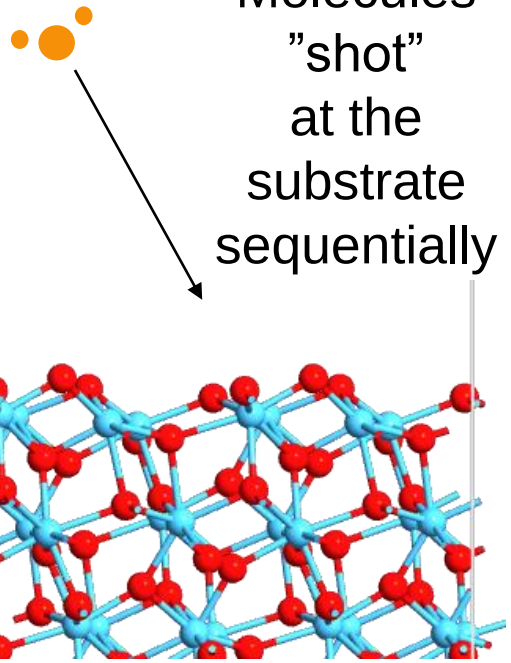
Thermochemistry Analyzer: Thermodynamics



Compare G_P-G_R for all combinations to find the best molecule

Ab Initio based

Surface Process Simulations: Kinetics



MD (FF) based

Thermochemistry Analyzer: Screen for Most Favorable Reactions as a Function of Temperature and Pressure

- Functionality:

  Compare multiple possible reactions in a process and find the most favorable ones at given conditions (screening reactions)

R1: $A_{surface} + B1_{gas} \rightarrow AB1_{gas}$

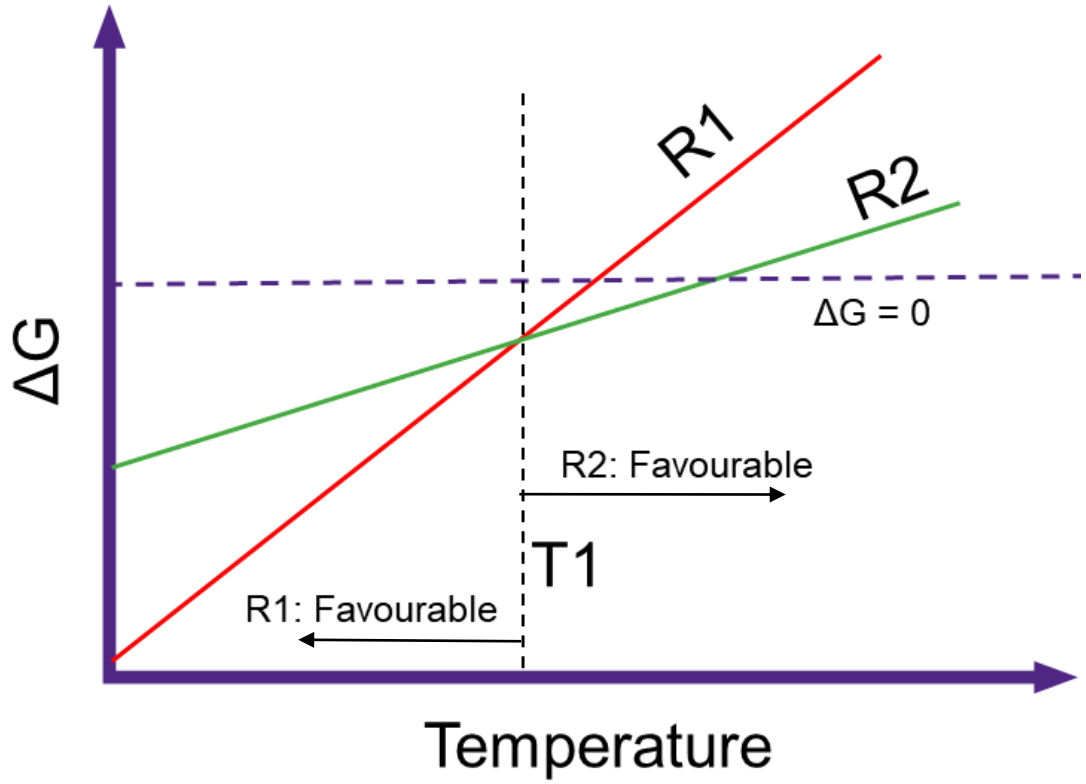
R2: $A_{surface} + B2_{gas} \rightarrow AB2_{gas}$

- At T=T1, both reactions are equally probable, subject to kinetic barriers
- Below T=T1, R1 is more favorable than R2 (lower ΔG), VV
- Gas B1 is favorable at low T and gas B2 at high T

Free energy difference:

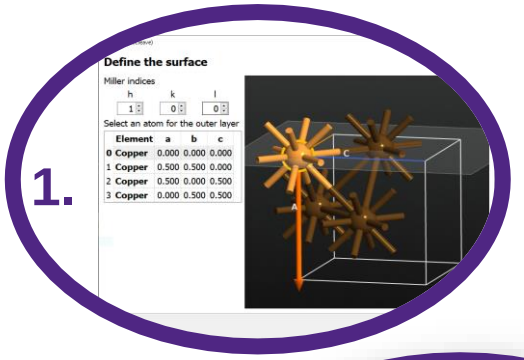
$\Delta G = G_{products} - G_{reactants}$

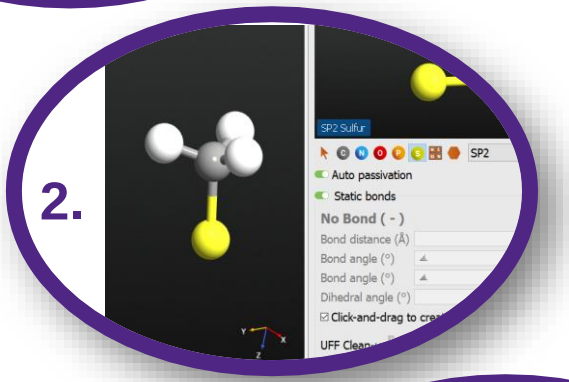
Low ΔG = more favorable

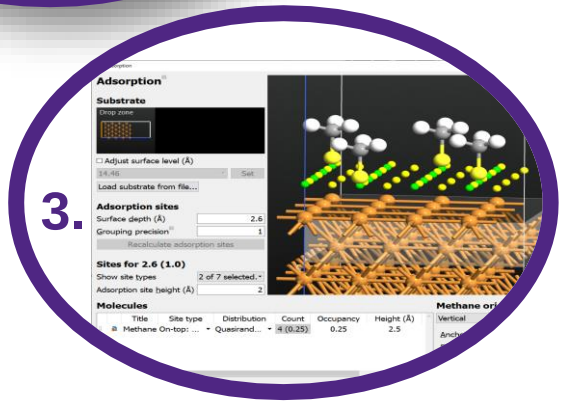


QuantumATK Steps for Thermochemistry Analyzer

1. Build surface slab
   - Choose bulk crystal material
   - Cleave surface
   - (“Melt and quench” if amorphous)
   - (Functionalize dangling bonds)
   - (Optimize slab)
2. Choose reactant molecule
   - Choose molecule stoichiometry (GUI or Z-matrix)
   - (Optimize initial configuration)
3. Adsorb reactant on surface
   - Choose surface coverage
   - Choose ordered vs random
   - Find binding sites (fixed atomic coord.)
   - Find height (fixed atomic coord.)
   - Optimize slab+molecule

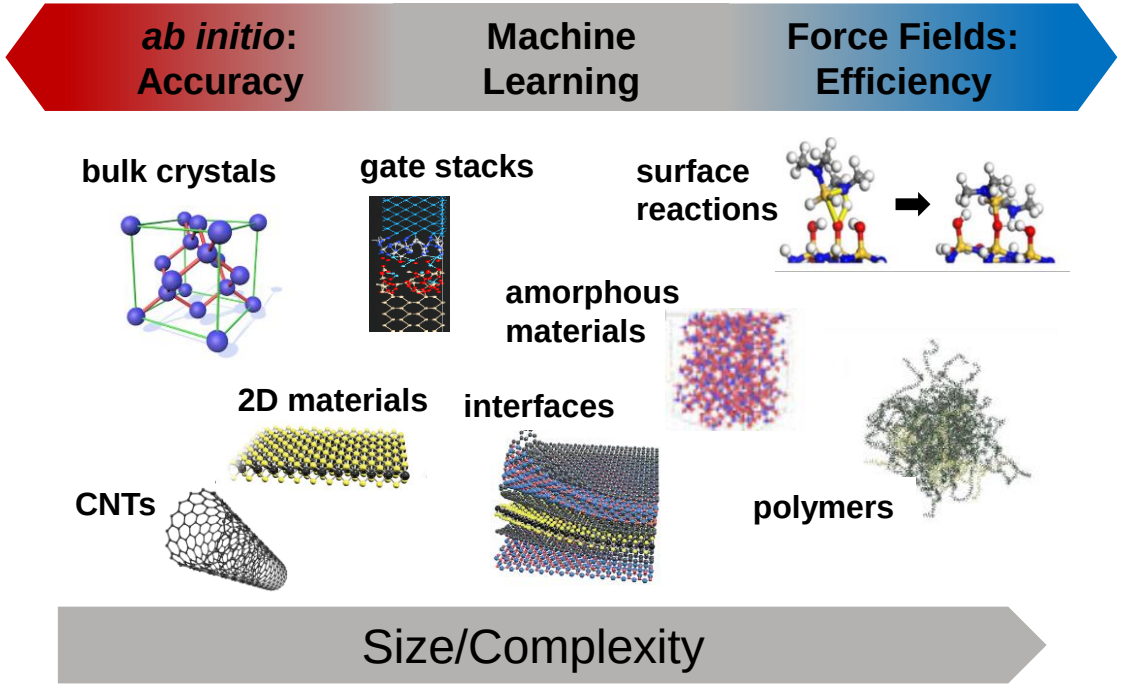






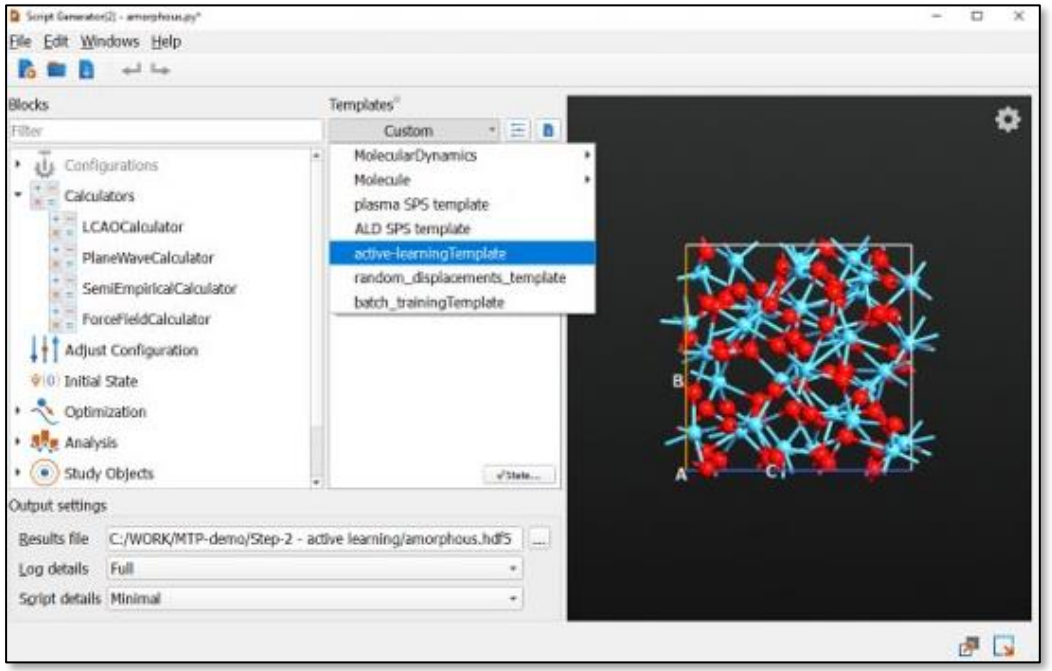
Machine Learned Force-Field Schemes for Fast, Accurate MD Simulations

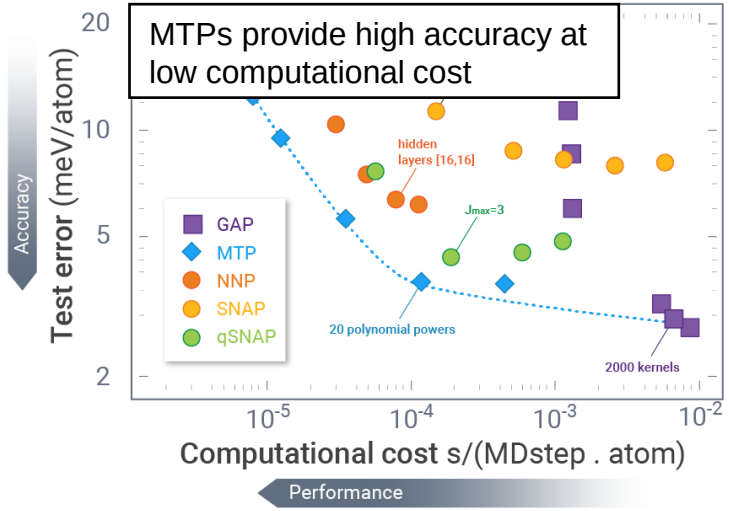
- Accurate *ab initio* methods are computationally demanding and limited to studies of small systems or periodic structures
- Empirical force-fields are used for large systems and trade accuracy for computational efficiency
- Machine learning (ML) methods close this gap and allow for the study complex systems at *ab initio*-level accuracy



Machine Learned Force-Fields can be Trained for Unknown Materials and Systems

Machine Learning is used to generate a Moment Tensor Potential (MTP) Force Field scheme



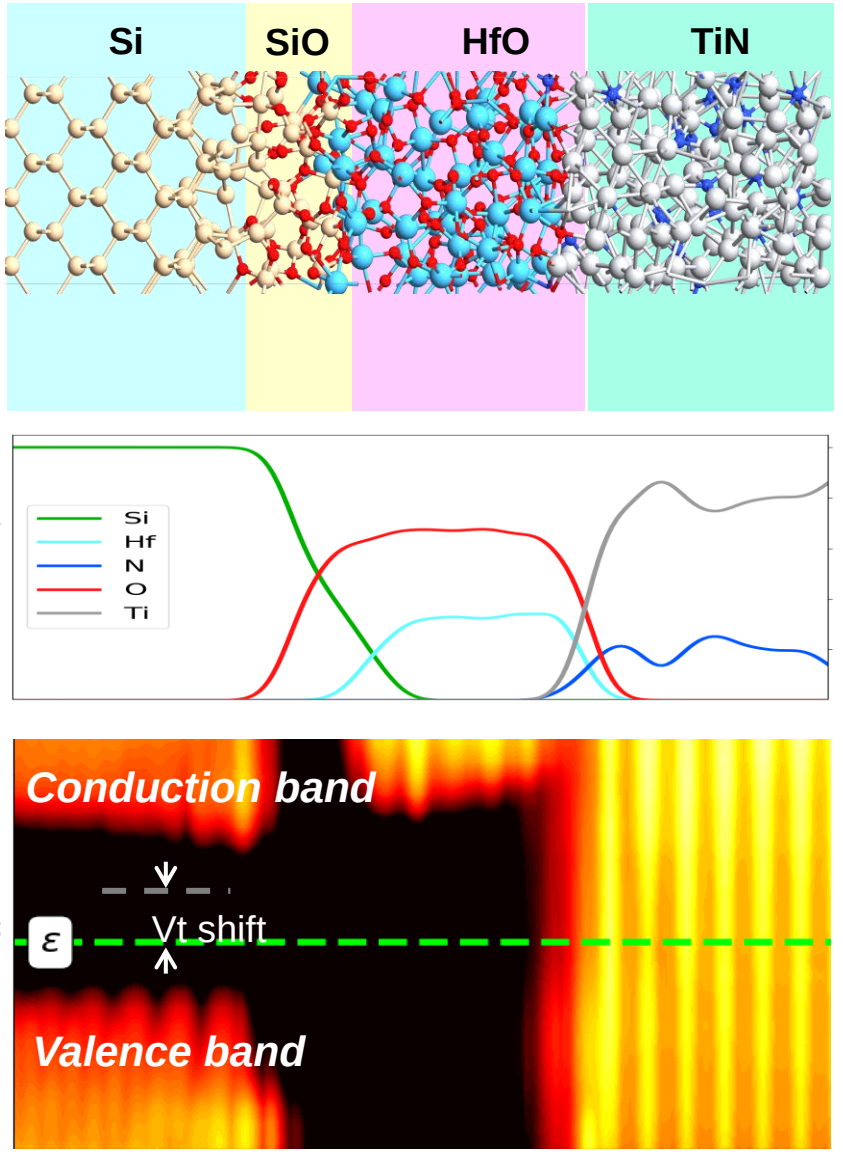


A. V. Shapeev, Mult. Model. Sim., 14, 1153 (2016).
Y. Zuo et al., J. Phys. Chem. A, 124, 731 (2020).

Ab Initio Materials Modeling Can be Used to Engineer Threshold Voltage

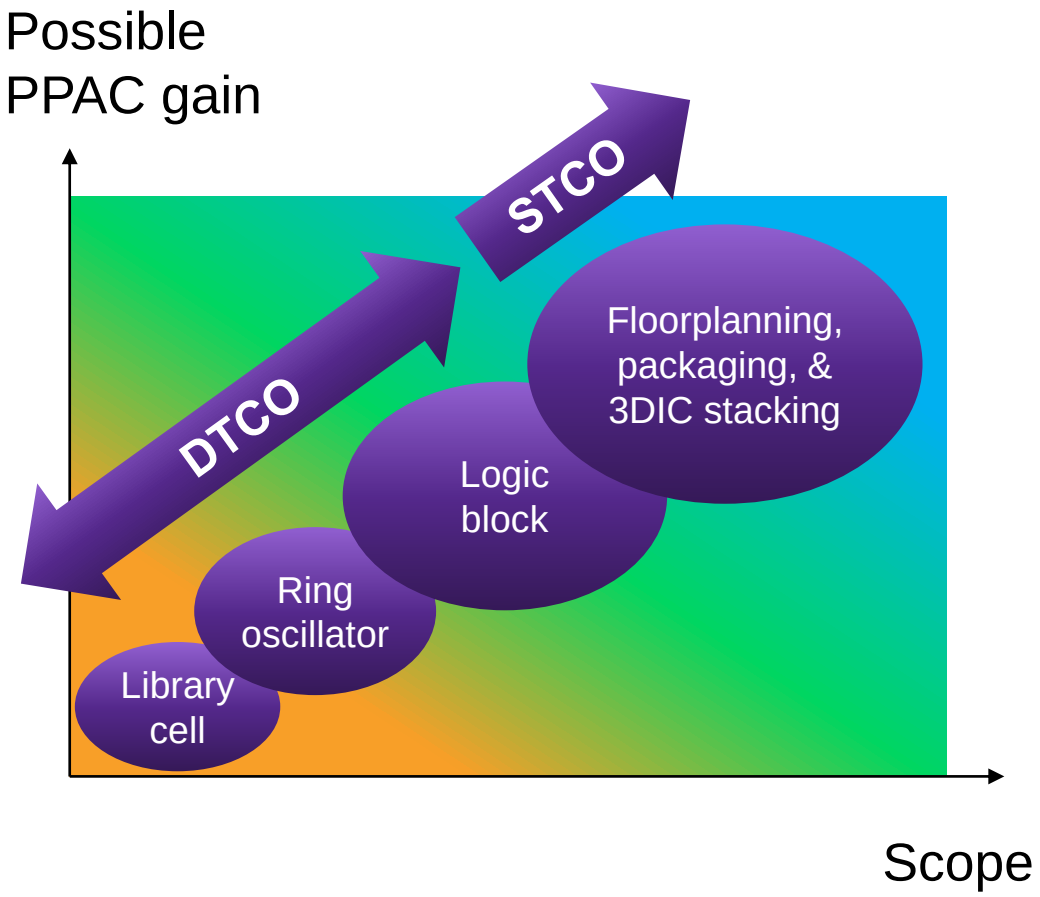
- High-K Metal Gate (HKMG) stack engineering is needed to realize the Vt:
  - Aluminum-hafnium dipole insertion for PMOS Vt
  - Lanthanum-hafnium dipole insertion for NMOS Vt
- HKMG stacks with target Vt can be designed and optimized with MD using MTPs
- Final Vt extraction is done with DFT
- Material composition extracted from atomistic HKMG stacks can be compared with SIMS/XPS

Creating proper stack geometries with DFT is extremely time-consuming.



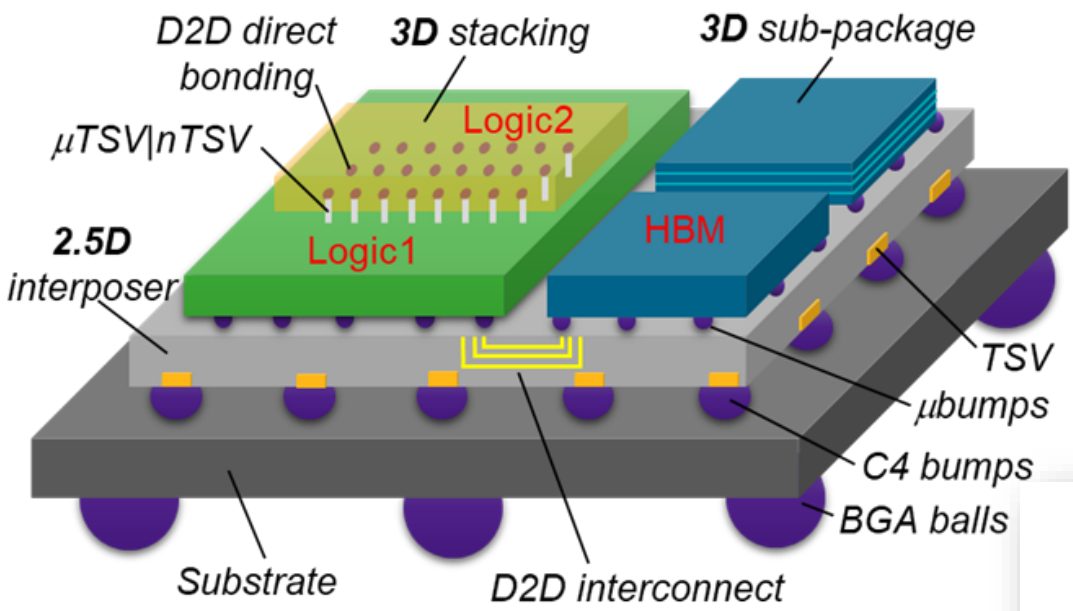
Materials Modeling in STCO

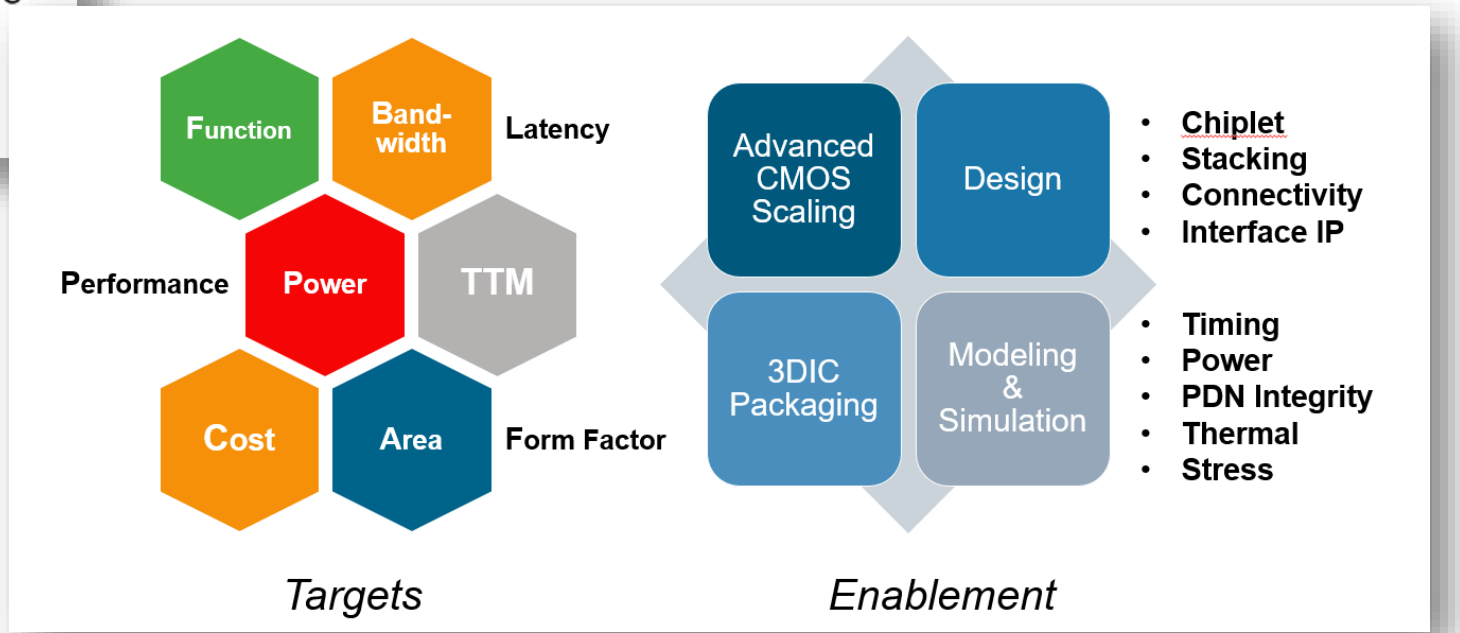
System Technology Co-Optimization (STCO) Scope



- PPAC (Power-Performance-Area-Cost) is the main technology metric
- Smaller scale PPAC analysis is faster and therefore enables evaluation of many technology and design options
- Larger scale DTCO/STCO analysis requires a larger effort, but enables bigger PPAC gains

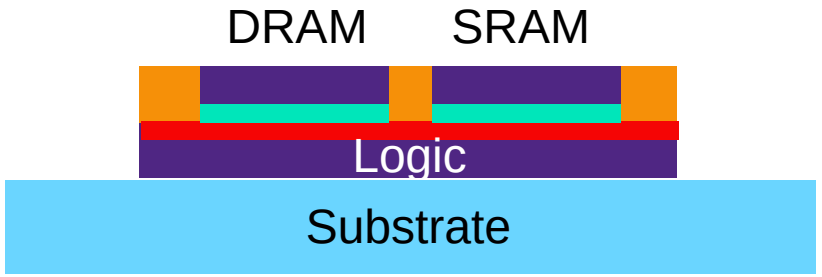
STCO for 3D IC Stacking



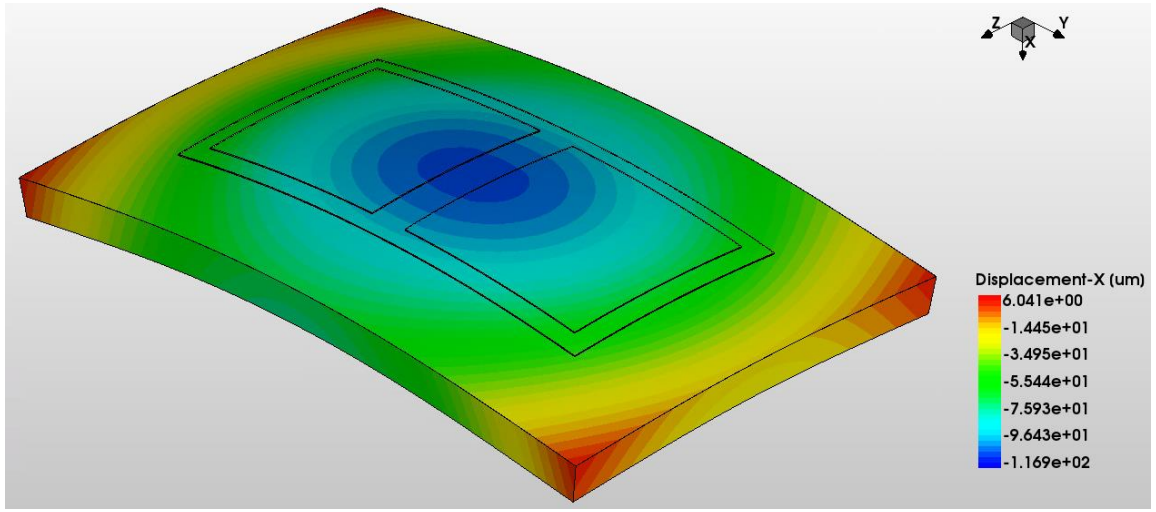


Xi-Wei Lin et al., IEDM 2021

Warpage of a Stack of 2 Chiplets on a Larger Chip

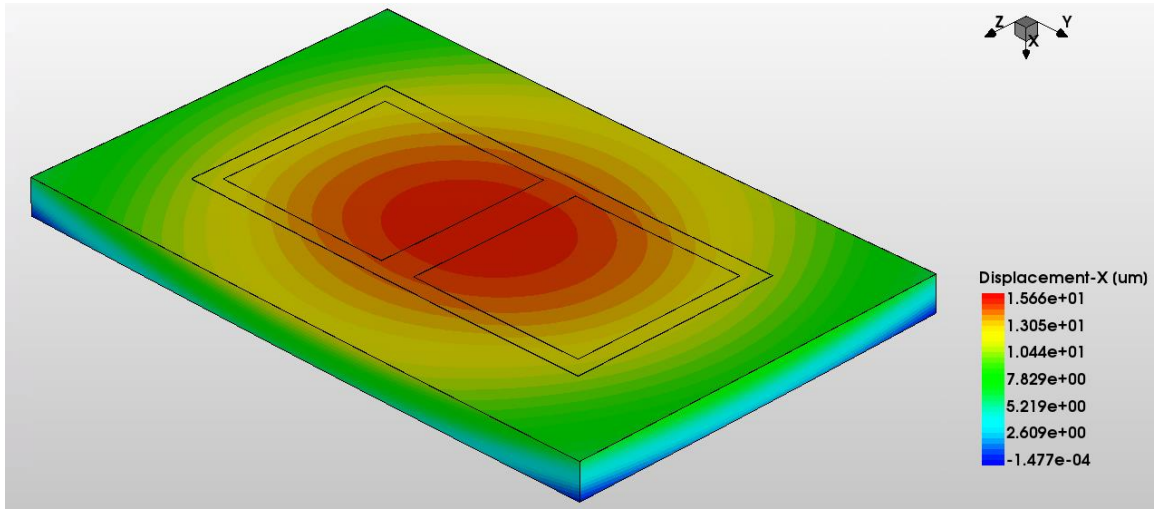


Strong warpage, but low Si stress



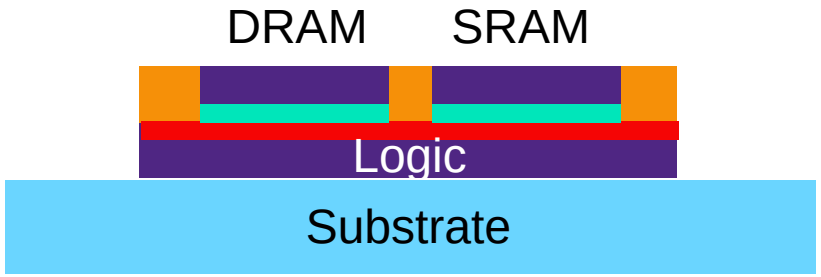
50 um thick Si die

Weak warpage, but high Si stress

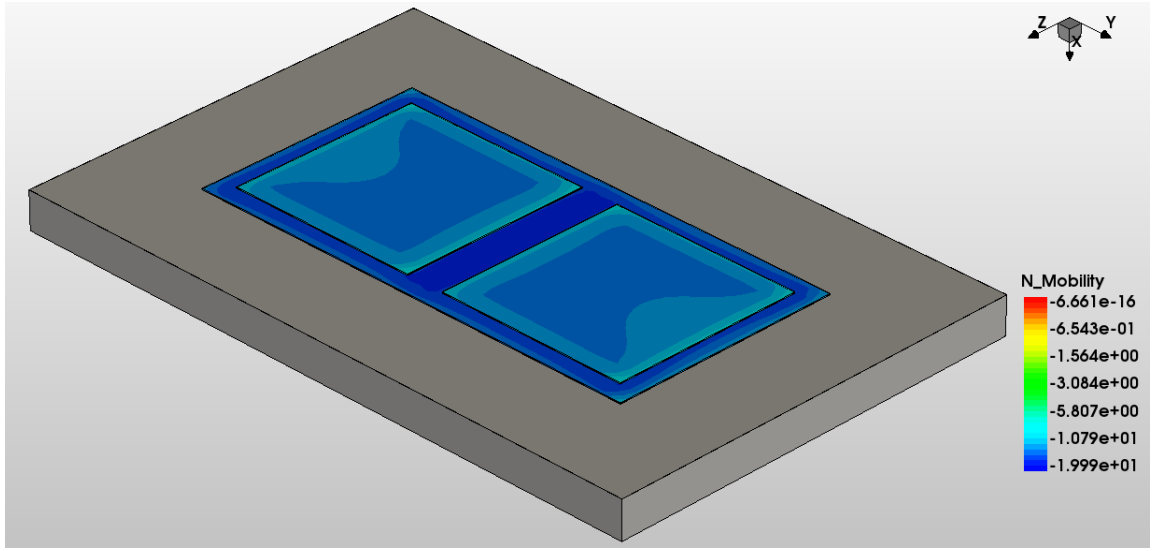


100 nm thin Si die

NMOS Idlin Map for a Stack of 2 Chiplets on a Larger Chip

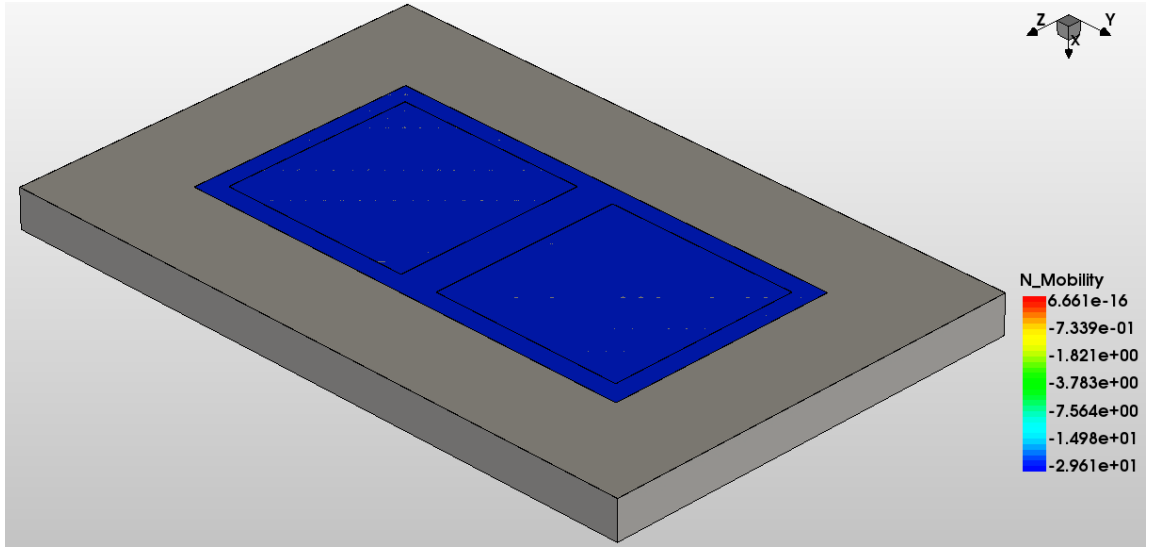


10% to 20% NMOS degradation



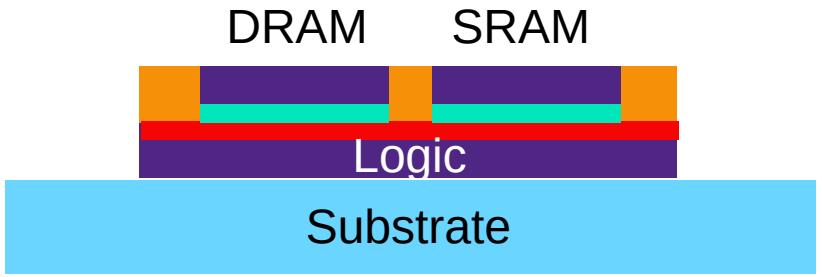
50 um thick Si dies

Uniform 30% NMOS degradation

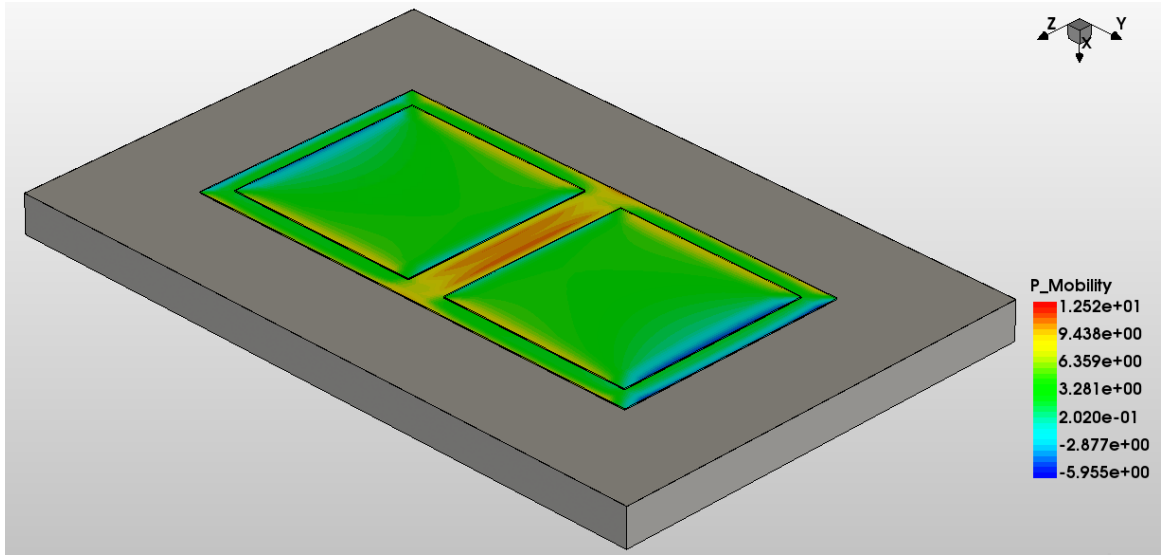


100 nm thin Si dies

PMOS Idlin Map for a Stack of 2 Chiplets on a Larger Chip

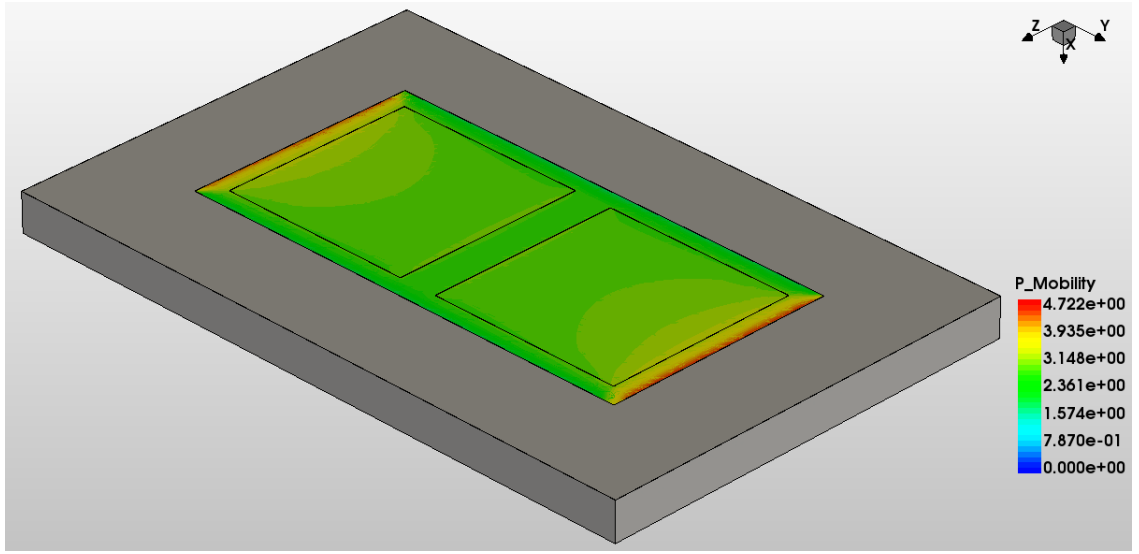


3% to 12% PMOS boost



50 um thick Si dies

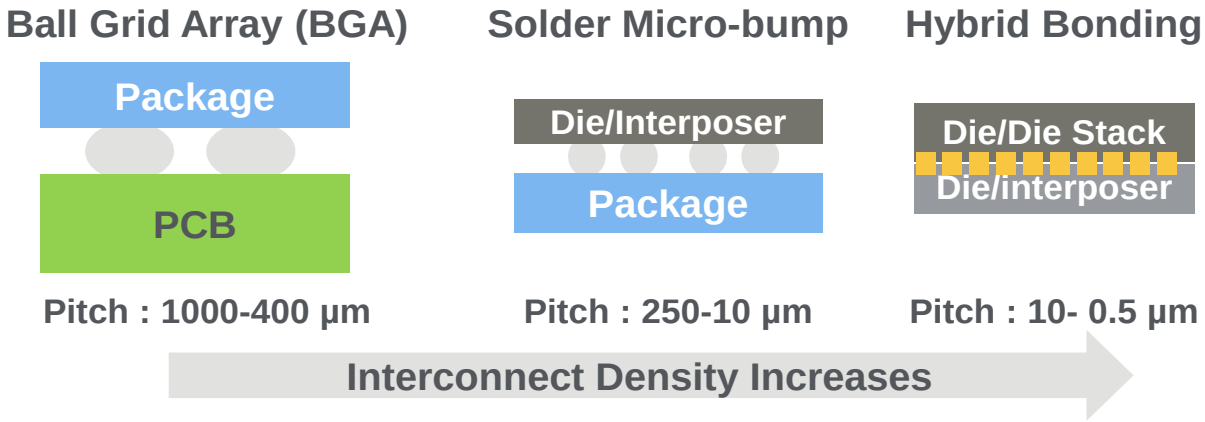
2% to 5% PMOS boost



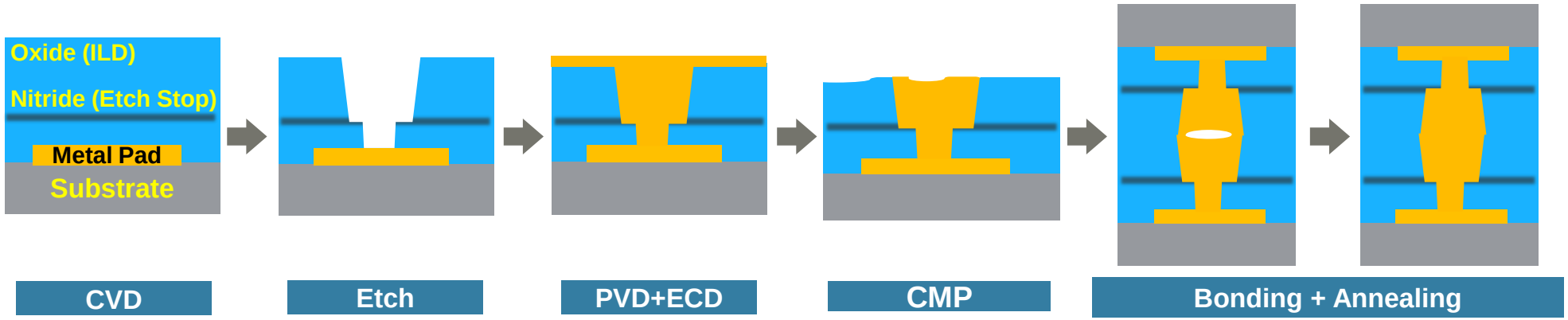
100 nm thin Si dies

Hybrid Bonding Technology Enables Sub-um Pitch

Fine-pitch Interconnect Scaling



Hybrid Bonding Process Flow [1]



[1] Albert Lan, "TSV and Hybrid Bonding Solutions for 3D Heterogeneous Integration Packaging Applying in Next AI/HPC Era", 17th International Conference on Device Packaging, '21

L. Jiang et al., ECTC 2022

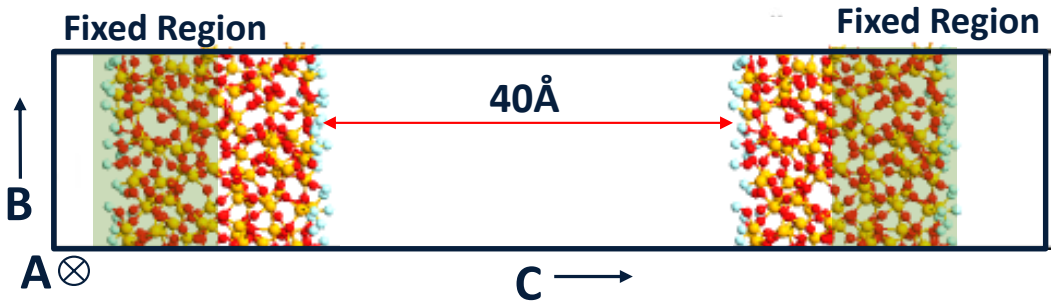
Atomistic Modeling of Binding Strength of SiO_2 Surfaces

2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)

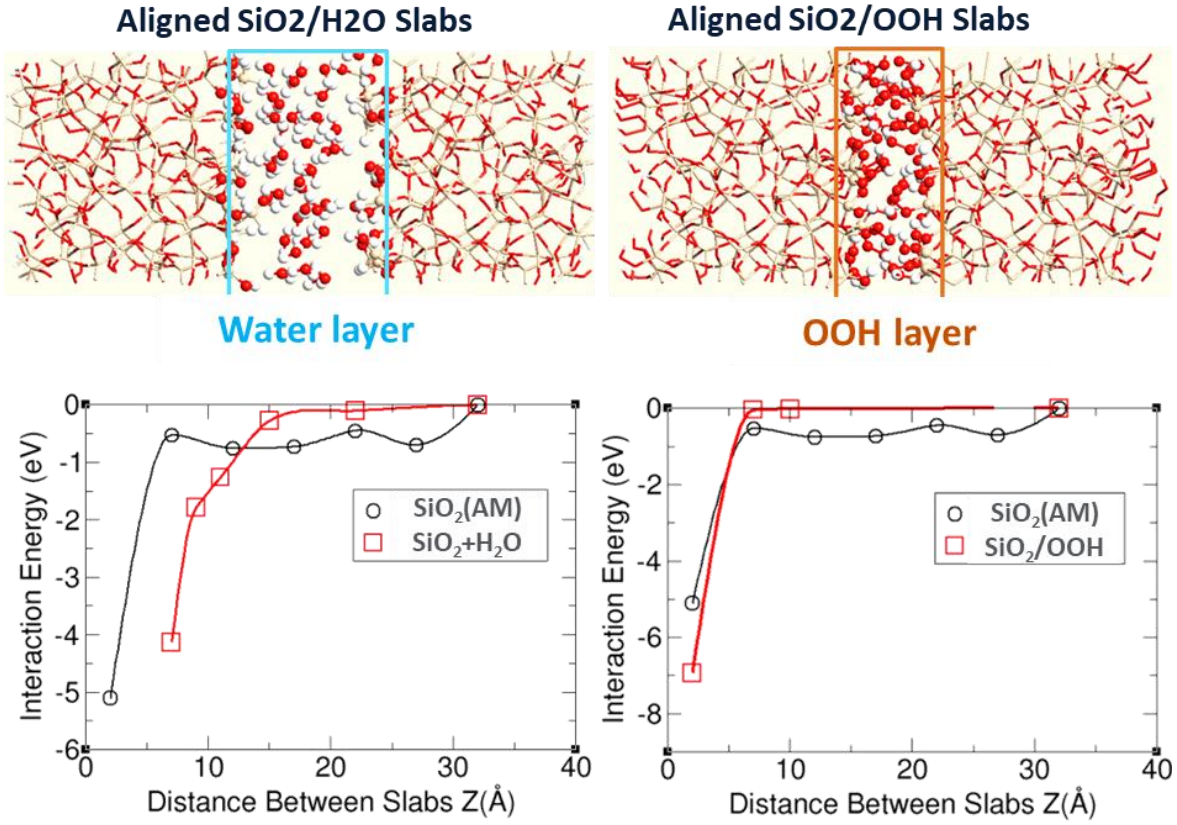
A Holistic Development Framework for Hybrid Bonding

Srikrishna Sitaraman[1], Liu Jiang[1], Sefa Dag[1], Mohammad Masoomi[1], Ying Wang[2], Prayudi Lianto[2], Jinho An[2], Ruiping Wang[2], Gilbert See[2], Arvind Sundarrajan[2], El Mehdi Bazizi[1], Buvna Ayyagari-Sangamalli[1].

[1]*Design Technology, Applied Materials Inc., USA*
[2]*Applied Packaging Development Center, Applied Materials Singapore Technology Pte. Ltd, Singapore*
srikrishna_sitaraman@amat.com



Binding energetics of SiO_2/SiO_2 surfaces



- Water layers between SiO_2/SiO_2 surfaces increase binding strength at larger surface separation
- OOH ligand coverage is beneficial to increase binding energy

Summary

- DTCO is already the main vehicle for transistor density scaling, and will keep Moore’s law going
- STCO and 3D place-and-route are necessary to go beyond 2D IC limits
- Advanced quantum and atomistic modeling are instrumental in optimizing material properties for transistors and 3D IC stacking.


SYNOPSYS®
Silicon to Software™