Holistic Approach to Clean Process Optimization for High Throughput CMP Applications

K. Mikhaylichenko[1], Y. Ding[2], J. Rajan[3], and B. Brown[4],
[1] AMAT, Ekaterina_mikhaylichenko@amat.com; [2] AMAT, Yunshuang_Ding@amat.com,
[3] AMAT, Jagan_Rajan@amat.com; [4] AMAT, Brian_Brown@amat.com

INTRODUCTION

As semiconductor device technology approaches critical scaling limitations, not only do the number of Chemical Mechanical Planarization (CMP) steps increase, but CMP defect reduction becomes critical for yield improvement. Moreover, the customers are facing high cost and restricted CMP Fab space challenges. To address this high value problem, CMP BU has developed the innovative CMP platform, which is targeted to provide best-in-class throughput density, flexibility and performance for various CMP applications.

BACKGROUND

During the more than thirty-year long CMP history, CMP ecosystems transitioned from the predominantly three-step CMP, which dominated the early-stage CMP processes, to the two-step and one-step CMP applications that gained momentum over the last few years. While the three platen CMP systems are ideal to support the three-step applications, there is a need for a flexible platform that can support various combinations of multi-step and one-step applications, as shown in Fig. 1a. To support this industry trend, Applied Materials has released the new Opta™ platform, which allows for operational flexibility, as shown in Fig. 1b. With four truly identical chambers, Head eXchangers (HDXs) with up to two heads per chamber, and central random-access robot, the platform can be operated in a variety of ways to support various application requirements, such as two-step (2x2) sequences running same or different processes, one-step 4x1 batch mode, 1x4 sequential mode, as well as Hybrid modes: for example, the 1x3+1x1 combo or the 1x2+2x1 combo. The system can support up to 200 wafer per hour (WPH) throughput (TPT).

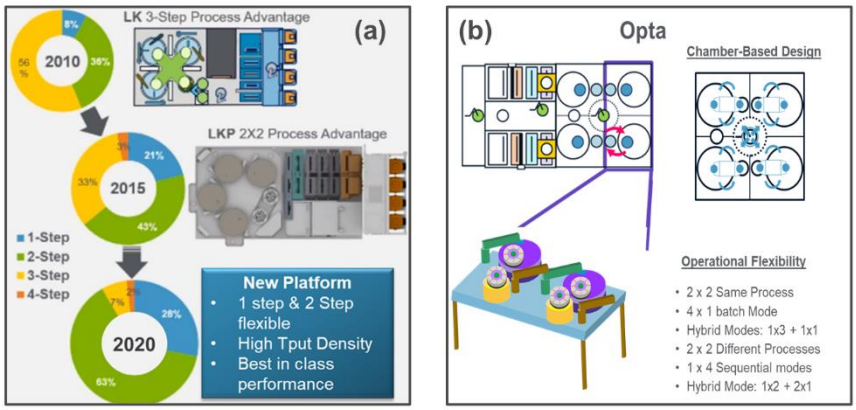

Fig 1a. CMP application trends: The need for a new CMP platform. Fig 1b. Opta: Platform for best defects, best capital efficiency, optimized fleet management

With short polish, the Cleaner becomes a TPT bottleneck. The flexible Cleaner architecture supports various Cleaner sequences with up to four high shear force contact clean modules and the Vapor Dryer, as shown on Fig. 2. With multiple module processes, total wafer cleaning time can be longer without affecting the TPT. Three sequential brush boxes reduce processing time within each of the modules, while maintaining or even increasing the total scrubbing time. With more total scrub time to reduce defects, high particle removal efficiency can be achieved, enabling outstanding defect performance at up to 200 WPH TPT. Moreover, the third brush box is exposed only to relatively clean wafers, already processed through two consecutive scrubs, yielding low brush loading for the third brush box and thus longer brush life.

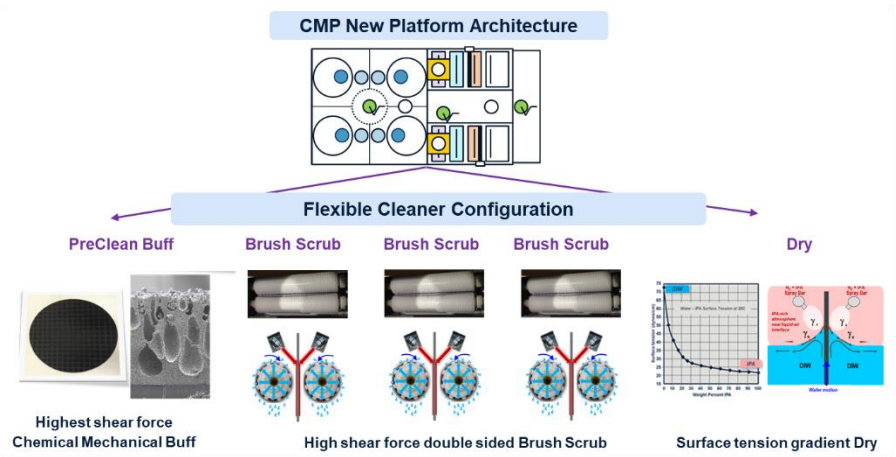

Fig.2 New CMP Platform and Cleaner configuration

Platen buff is considered the benchmark for the chemical mechanical buff cleaning efficiency, as it is associated with (1) the 100% buff duty cycle, with the entire surface of the wafer exposed to buff, and (2) the shortest time between the end of polish and the onset of cleaning and, therefore, the minimal time to develop and strengthen the bond between the polish residuals and the wafer surface. Even though platen buff provides high cleaning efficiency, including platen buff step in the CMP sequence has negative impact on the tool TPT density as the entire platen is dedicated to a step with zero material removal. Moving the buff process into the dedicated module within the Cleaner frees up the platen to be used for polish, allows for a more aggressive choice of buffing chemicals, and creates an overall cleaner environment for the buff, since the wafer coming to the buff station is thoroughly rinsed in the load cup during the head unload.

The PreClean module (HPC), newly developed for the new CMP platform, plays a key role in meeting defect requirements with very short process times. Fig. 3 shows the HPC schematics and highlights design differences for the HPC and the PreClean module used on the LKPrime™ platform: increased pad size allows for 4x improvement in coverage; the maximum buff pressure is 30% higher for HPC; better fluid retention is achieved with the optimized design.

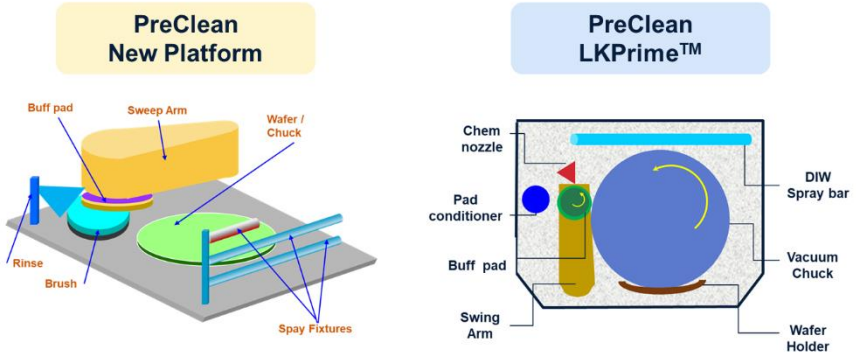

Fig.3 Chemical mechanical buff implementation: Opta™ HPC vs LKPRime™ VPC

EXPERIMENTAL RESULTS AND DISCUSSION

First, we explored the benefits of the HPC module for the difficult to clean ceria abrasive-based slurry CMP Shallow Trench Isolation (STI) applications. Wafers were polished with the ceria slurry (STI24xx-STI29xx) using the NexPlanar pad (NXP60xx) and cleaned with three different implementations of the

chemical-mechanical buff -- platen buff, VPC buff, and HPC buff -- using the same buff recipe times. Commercially available ceria cleaning chemistry was used for the chemical mechanical buff; dilute ammonia solution was used for the brush box cleans. Soft polishing pad (H8xx) was used for the platen buff as well as for the HPC and the VPC PreClean modules. Fig. 4 shows the normalized defect performance on blanket TeOS wafers measured at the 45nm threshold on the KLA SP5 metrology tool for these three buff methods. The corresponding defect adder maps are also shown; map-to-map defect comparison for Pre and Post SP5 scans is used to generate the adder maps.

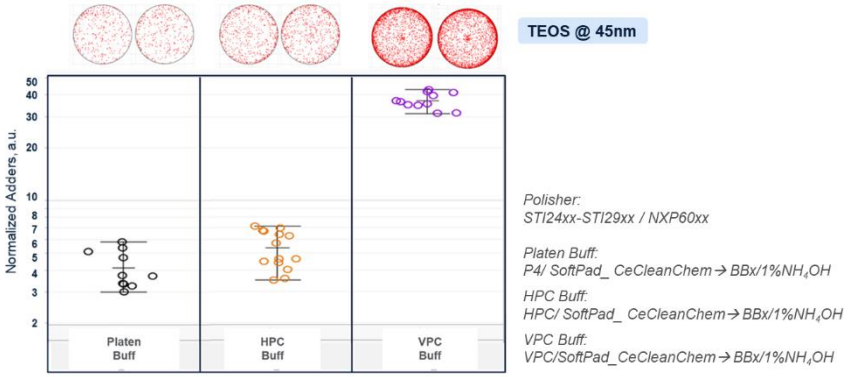

Fig.4 STI Ceria Polish | Chemical Buff Cleaning Efficiency: Platen buff vs HPC vs VPC

The results demonstrate similar performance between the platen buff and the HPC buff. As a result of improved area coverage, improved chemical coverage and increased buff pressures, the HPC process provides 7x defectivity improvement over the LKP™ VPC for difficult to clean ceria CMP, eliminating the need for the platen buff.

Second, Opta benefits for high TPT allocations were explored using acidic silica oxide buff CMP as an example. As mentioned earlier, with multiple module processes, total wafer cleaning time can be longer without affecting the throughput. However, the Dryer becomes the throughput bottleneck. Drying time and its impact on defects is critical: overall defect performance of the system is only as good as the Dryer is.

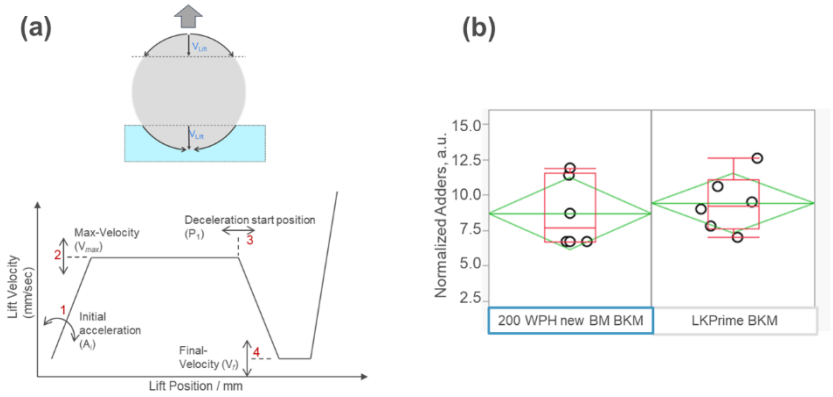

Fig 5a. CMP Vapor Dryer recipe parameters. Fig 5b. Normalized defect performance for the high TPT Opta™ and the standard TPT LKPrime™

Fig. 5a shows Vapor Dryer recipe parameters optimized to minimize the drying time. Fig. 5b shows the normalized defect performance for the high TPT process with the Dryer recipe optimized for the 200 WPH TPT and the standard TPT LKPrime™ benchmark process, demonstrating no negative impact on defect performance. Thus, through Dryer recipe optimization combined with Dryer overhead reduction, we have demonstrated an excellent defect performance at 200 WPH.

Blanket TeOS wafers were polished with the acidic silica abrasive-based slurry (D92XX) using the IC1010 pad and cleaned using the HPC module with the soft polishing pad and commercially available acidic cleaning chemical, followed by the dilute ammonia brush scrubs. Fig. 6a shows the normalized defect performance on TeOS at the 45nm threshold for various buff times; the results of the defect review and classification are given in Fig. 6b. Without the chemical mechanical buff, the defect counts are saturated, exceeding the SP5 measurement capacity at that threshold. Including chemical mechanical buff into the Cleaner sequence results in a drastic improvement in defects. The design of the HPC module allowed for up to 50% reduction in the buff time before the negative impact on the defect performance has been observed as the recipe time has been reduced to the 40% of the baseline. Defect review confirmed that the number of particles remaining on the wafers after the high TPT clean is within the single digits, which is comparable to the environmental adders in the Lab.

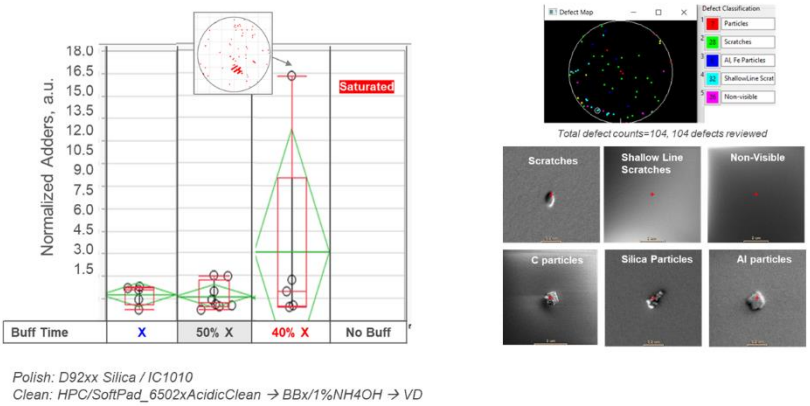

Fig 6. Defect performance on TeOS @ 200 WPH for the Oxide Buff silica 10-step polish

Finally, we have explored the impact of improved platen isolation on the defect performance for the 2-step CMP, as shown in Fig. 7. In this application, the first polish step utilizes ceria abrasive-based slurry to achieve the planarization targets while the second step implements acidic silica abrasive-based process to achieve good defectivity.

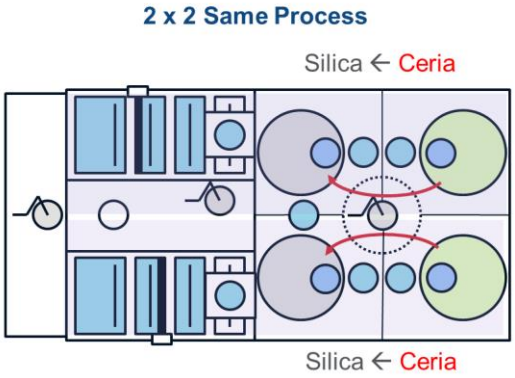

Fig.7. Cross-contamination challenge of the 2-Step CMP (Ceria polish followed by silica polish)

To generate data shown in Fig. 8, blanket TeOS and silicon nitride wafers were polished with the ceria slurry (SEC5xxx) for the first step, followed by the acidic silica slurry (PL61xx) polish for the second step. A combination of acidic and alkaline cleans was implemented in the brush boxes.

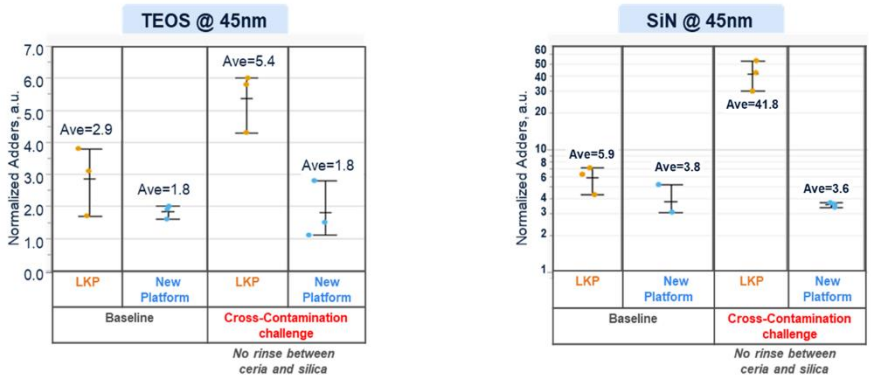

Fig. 8. Platen isolation impact on cross-contamination control for the 2-Step Ceria+Silica STI polish

Fig. 8 shows normalized defect performance for TeOS wafers measured at the 45 nm threshold and silicon nitride wafers measured at the 45 nm threshold. For the baseline process, the wafers were rinsed with the High-Pressure Rinse (HPR) for 10s on the ceria platen at the end of the polish. For the contamination challenge tests, the HPR step was eliminated. For baseline process, the data show slight improvement in defects for the new platform vs LKP™. Larger data sample is needed to determine if this difference is statistically significant. For the cross-contamination challenge test, the benefits of the new platform become apparent. With no HPR rise between the ceria and the silica steps, the defect counts on the LKP™ platform increase by ~ 3X for TeOS and by >10X for silicon nitride wafers. For the Opta™ platform, eliminating the HPR between the ceria and silica steps has no impact on defect indicating improved platen isolation and better cross-contamination control due to the dedicated head-platen architecture.

CONCLUSION

A holistic approach to clean process and hardware optimization is required to meet defect performance targets. Defect optimization for high TPT application must start with the module that is a TPT bottleneck. Multiple modules and time re-allocation between them are needed to meet cleaning efficiency at high TPT. High shear force module is needed to meet cleaning efficiency requirements. Cross-contamination control is also important.

Hardware flexibility and customization is key. Opta™ configuration can be customized to meet performance targets for difficult to clean STI ceria CMP, with moderate TPT requirements, or relatively easy to clean buff CMP with high TPT requirements. In Opta™ configuration, wafer transfer sequences and process recipes have been optimized to demonstrate defect performance meeting target for Oxide Buff CMP with 200 WPH TPT.

Corresponding Author:
Katrina Mikhaylichenko
Tel: +1 408-685-1776
E-mail: Ekaterina_mikhaylichenko@amat.com
Applied Materials
974 E Arques Ave,
Sunnyvale, CA 94085, USA