MODELING EDGE-OVER-EROSION FOR ADVANCED CMP PROCESSES

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ABSTRACT

Chemical mechanical polishing/planarization (CMP) is one of the primary processes used in modern integrated circuit (IC) manufacturing. Modeling of the post-CMP surface profile is critical for detecting planarity hotspots that can cause fatal chip failures during manufacturing. Edge over erosion (EOE) over-polishing is one cause of these hotspots. The EOE effect is usually observed during copper and tungsten CMP, causing open errors within a layer and short errors at upper layers. Detecting and fixing EOE hotspots can reduce variability in the IC and increase yield. We present a modeling and hotspot detection solution for the EOE phenomenon.

INTRODUCTION

Chemical mechanical polishing/planarization (CMP) is a key technology for achieving surface planarity during the manufacturing of multi-level interconnections of semiconductor chips and electronic devices. It is one of the essential processes used in integrated circuit (IC) manufacturing. CMP is used at major steps in IC fabrication, such as front-end-of-line (FEOL) for transistor fabrication, middle-of-line (MOL) for the local electrical connections between transistors, and back-end-of-line (BEOL) for interconnect structures. While CMP is intended to achieve planarity, thickness variations caused by the CMP process are a major cause of yield loss.

Modeling of the CMP process enables the detection and fixing of possible CMP planarity hotspots prior to manufacturing. Based on technology requirements, chip designers define special rules for hotspot detection in post-CMP surface profile analysis [1]. Design for manufacturing (DFM) tools like the Calibre® CMP ModelBuilder and CMPAnalyzer solutions from Siemens Digital Industries Software can be used for hotspot detection based on these criteria.

Accuracy demands in CMP modeling increase with the rapid emergence of new process technologies, larger, more complex silicon systems, and smaller feature sizes. To meet these requirements, CMP models must continually accommodate novel phenomena observed during the CMP process. In addition to classical dishing and erosion, the edge over erosion (EOE) effect has drawn the attention of process engineers and designers (Fig. 1).

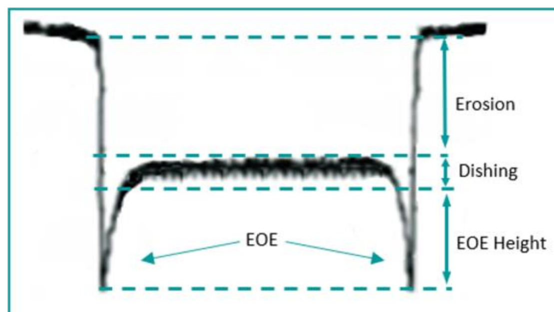

Fig.1 Graphical representation of EOE phenomena.

EOE, also known as the Fang effect, is typically observed during copper and tungsten (Cu and W) CMP at transitional regions between the edge of large non-patterned areas and an array of trenches (Fig. 2).

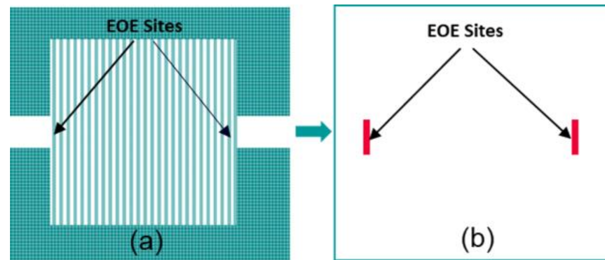

Fig.2. (a) Pattern with array of trenches and dummy exclude area. (b) Potential EOE hotspot regions.

EOE occurs because of over-polishing during barrier CMP when materials in trench areas (Cu or W) are polished much faster than the materials in non-trench areas (oxide). More precisely, the edges of an array of trenches polish faster than at the center of the array, causing over-polishing at the edges (Fig.3).

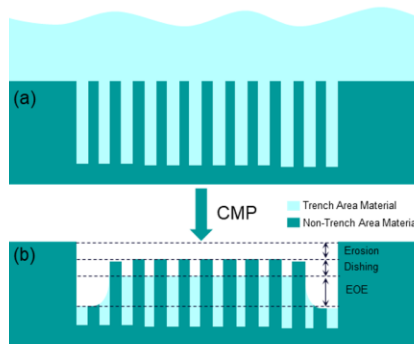

Fig.3 Profile topography (a) before and (b) after CMP, showing EOE effect.

The lost material height at the locations where EOE occurs is much greater than regular erosion (Figs 1, 3), causing open errors. Moreover, during multi-level metallization above EOE over-polished arrays, shorts and metal thickness variations may also occur, which can lead to fatal errors and yield loss.

Elimination or reduction of the EOE effect is a key focus in the CMP industry. Experimental, physics-based [2] and machine learning (ML)-based [3] investigations have been carried out to understand and model this phenomenon. It has been found that the EOE effect usually occurs during the over-polishing step and is the highest for patterns with narrow trenches. It was also found that EOE is highly dependent on feature sizes, pattern densities, and array sizes [2]. It was concluded that, for modeling EOE phenomena, test patterns with wider available pattern densities are more effective than patterns with only EOE effect and limited geometry variations [2]. In [3], the parameters having the most impact on EOE phenomena were extracted from the testchip. A multi-level ML-based EOE prediction method was proposed. Results show that the proposed method attained 2.7-19.2% accuracy improvement of EOE effect prediction and 0.8-10.1% accuracy improvement of non EOE prediction compared with other general ML methods [3].

EOE MODEL BUILDING

CMP modeling requires several steps [1]. First, a testchip containing array patterns with and without EOE sites is designed and taped out. EOE height, erosion, dishing, and topography thicknesses are measured from the testchip using surface linescan tools, and the data is loaded into a measurement data table (MDT). A process recipe file is created that includes parameters for modeling EOE, along with other CMP model parameters. The CMP model recipe parameters are then calibrated to fit the MDT data. After calibration, the model with the best-fitting parameters is saved as a final recipe. Finally, an enhanced CMP model simulation is performed using the recipe to detect EOE, erosion dishing, and other hotspots (Fig. 4).

We used this process with the Calibre CMP ModelBuilder and CMPAnalyzer solutions to predict and model EOE phenomena on testchips and production designs.

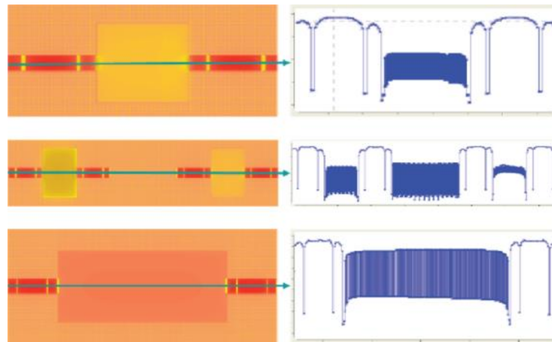

Fig.4 Examples of EOE height simulation on testchip structures using calibrated model.

EOE MODEL APPLICATIONS

As the scale of technology nodes becomes smaller and smaller, accurate hotspot modeling requires moving to smaller and smaller window size simulations on the order of several microns or below. On modern designs, EOE may be observed on small scales around isolated trenches and dummy exclude areas, as well as around small parallel lines of trenches close to unpatterned areas. Performing small window-size full-chip physics-based CMP simulations consume a significant amount of time and computational resources.

We propose an optimal EOE modeling solution as follows: First, run a relatively large window-size full-chip simulation and detect locations of potential EOE sites by performing special design analysis. Next, based on the analysis of neighboring patterns, prioritize these EOE sites by assigning special scoring coefficients to them (Fig. 5(a)). The larger the coefficient, the higher the possibility of extreme EOE over-polishing.

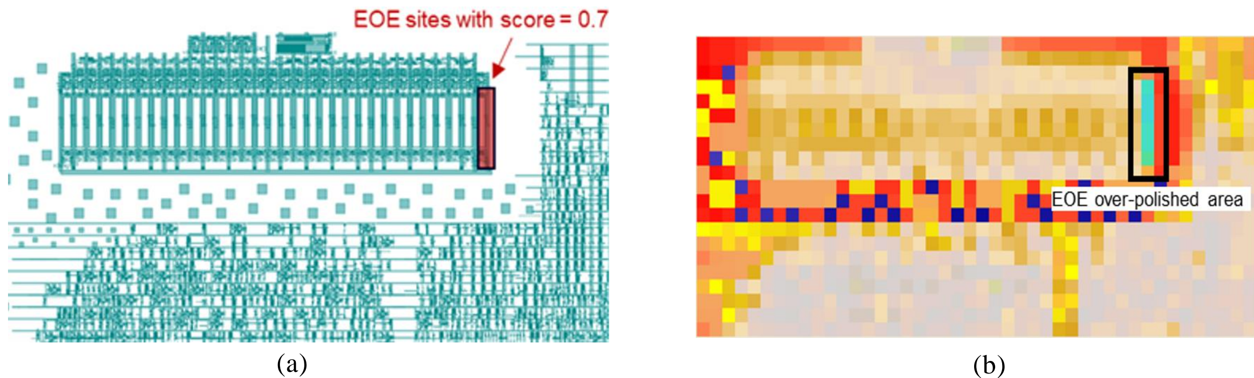

Fig. 5. (a) Potential EOE sites with scoring, (b) Simulated topography with EOE over-polished area.

Once potential locations of EOE sites are detected, perform CMP simulations with smaller window sizes at those locations to detect the surface topography and height of EOE over-polished areas. Fig. 5(b) shows an example of simulated topography around a potential EOE area.

To analyze the topography, use the simulated horizontal and vertical linescans and profile plot, as shown in Fig. 6. It is evident that the detected EOE area is indeed over-polished compared to neighbor sites. Meanwhile, there is no over-polishing of similar structures on the left edge of the pattern, where EOE was not detected (Figs. 5,6).

Hotspots are reported if the EOE height is larger than the specified threshold value for the given technology node and process requirements.

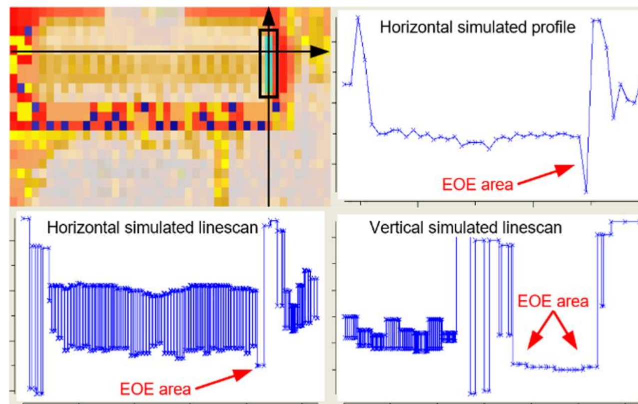

Fig. 6. Simulated topography with EOE over-polished area.

CONCLUSIONS

In this paper, we discussed the modeling of EOE phenomena. EOE investigation is crucial because over-polished EOE regions typically cause open errors within a layer, and short errors at the upper layers, leading to fatal failures in production chips. We discussed a methodology of model building for detection and analysis of EOE hotspots. Modeling EOE phenomena allows design teams or process engineers to observe EOE-affected sites and detect over-polishing heights due to EOE, depending on the pattern. The application of EOE simulations was demonstrated using Calibre CMP ModelBuilder and CMPAnalyzer solutions on a specially designed testchip containing test patterns with both EOE affected and unaffected regions. The model allows engineers to observe potential EOE sites, prioritize them depending on neighboring patterns, and predict EOE hotspots using CMP simulations. An example of EOE over-polished area detection was demonstrated on a production-like design containing regular patterns. Analysis of simulated topography clearly indicated the existence of EOE over-polishing. Detecting and fixing EOE hotspots prior to manufacturing can lead to a reduction in chip variability and an increase in yield.

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