

Advanced SiC CMP for High Volume Manufacturing of Power Devices

John Givens¹, Sean Yu², Jianjun Hu², Longlong Xu²,
Mike Liu², Eulia Liu², Jamie Leighton¹

¹Applied Materials Inc., 3050 Bowers Ave, Santa Clara, California 95054, USA;

²Applied Materials Inc., 28 Xinxi Road, Xi'an, Shaanxi Province, China

Silicon Carbide (SiC) provides excellent characteristics such as superior thermal conductivity, high carrier mobility and extreme chemical stability in comparison with those of Silicon (Si). SiC is already showing significant device performance benefits in power devices, high performance communication, and LED lighting. However, SiC presents many challenges for wafer surface treatment because of its high hardness and remarkable chemical inertness.

Today, mechanical polishing techniques on industrial batch CMP tools are the predominant methods for SiC wafer surface treatment, but material removal rate (MRR), surface defects and wafer flatness control are reaching fundamental limits with increasing wafer diameter.

A unique single wafer chemical mechanical polishing (CMP) technique on 150mm n-doped, 4° off-axis, single crystal, 4H-SiC wafers was developed to create a virtually defect-free surface. A polishing head has been designed to manipulate polishing pressures at various zones of the wafer. This capability can modulate the removal thickness at each region on the wafer surface, resulting in a highly uniform wafer profile. Additionally, a CMP slurry has been formulated to maximize MRR from 2µm/hr to over 8.5µm/hr. Potassium permanganate has been selected as an oxidant and aluminum oxide particles as the abrasive. The oxidant concentration and abrasive content along with slurry pH level have also been optimized for ideal chemical and mechanical activity.

Scratch-free wafer surfaces are observed with atomic force microscopy (AFM) and bright field (BF) and dark field (DF) inspection techniques. Roughness on the Si face is reduced to below 0.08nm. Total length of surface scratches was reduced to 10mm or less. Industrial metrics of wafer flatness, including total thickness variation (TTV) and local thickness variation (LTV) are modulated and improved.

Corresponding Author:

John H. Givens, Ph.D.
Tel: +1 512-422-6820
E-mail: john_givens@amat.com

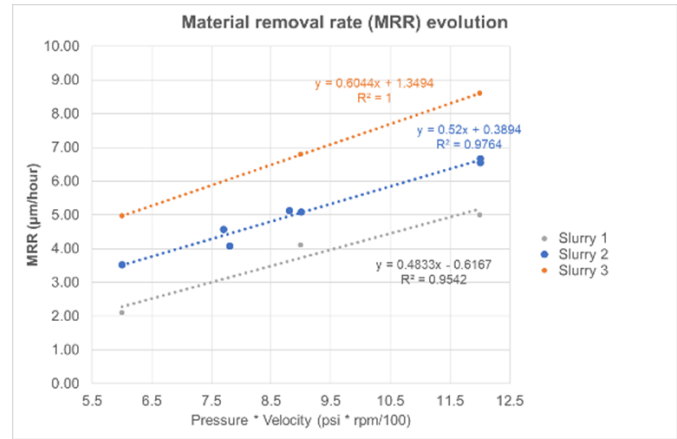


Fig.1 MRR of Si face CMP as a function of P*V (pressure x velocity) for 3 commercial slurries

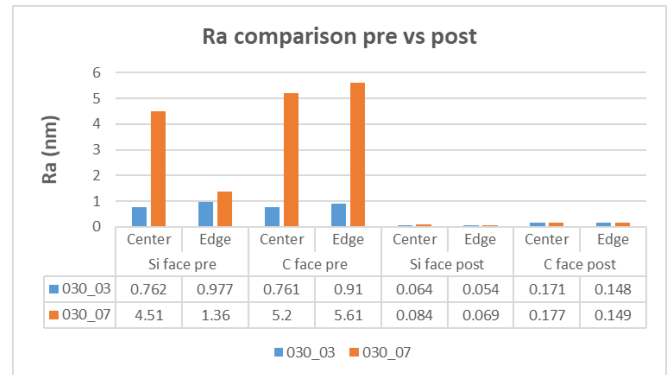


Fig.2 AFM results for before and after SiC CMP. Independent of the incoming surface finish 0.08nm Si-face and 0.18nm C-face can be achieved.

Preference: Oral Poster

- Topic Area: CMP for emerging technologies such as MEMS/LEDs/power devices