Pad Designs

- To navigate the fundamentals of CMP -

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INTRODUCTION

The CMP pad industry has been an oligopolistic market with only few companies being the dominant CMP pad suppliers for over 35 years and their major products containing pores and asperities. Almost every pad supplier has focused on tweaking pad materials to improve the polishing performances and consistency. However, the industry requires a paradigm shift that can deliver more precise and consistent polishing in combination with longer pad life. Table 1 summarizes problems of conventional pads such as planarization, scratches, material selectivity, cost of ownership, run to run variations and edge exclusion limits. To address the problems, a pad with uniform asperity height with a conditioning free and segmented hard layers without pores for extreme edge uniformity and better run to run variation is suggested.

SMART PAD is introducing a complete redesign of the structure of the CMP pad that will help the chipmakers improve wafer production yield by significantly reducing or eliminating scratch defects, increase chip throughput by increasing polishing rates, and reduce the Cost of Operation (CoO) by eliminating the pad conditioning process and extending pad usage time.

Based on characterization of conventional pads, design rules for contact features are introduced. The effect of designs on slurry flow were investigated through Computational Fluid Dynamics (CFD) and Finite Element Analysis (FEA). Through micro-molding technology, new pads with proposed designs were manufactured and evaluated with test wafers.

Problems	Root causes	Solutions	Solution Pad
Planarization	Non-selective polishing Due to non-uniform asperity height	Uniform asperity height Conditioning free pad	
Scratch	Stress concentration Due to non-uniform asperity height	Uniform asperity height Conditioning free pad	1. Conditioning free with
Material Selectivity	Mechanically driven polishing Due to non-uniform asperity height	Uniform asperity height Conditioning free pad	uniform asperity height
Cost of Ownership	Pores & PSA Conditioner	No pores, Less PSA Conditioning free pad	2. Pore free
Run to Run Variation	Non-uniform asperity heights due to conditioner wear Pad temperature increase due to pores	Uniform asperity height No pores	3. Segmented hard layer
Extreme Edge Exclusion (<2mm)	Pad rebounding around edge of wafer Due to thick/bulk hard layer	Independently moving hard layer segment	

Table 1. Problems of Conventional Pad and Solutions

CHRACTERIZATION OF CONVENTIONAL PADS

Pad topographies can be characterized from a top-view and side-view analysis. Figure 1 describes pad characterization done by SEM and a white light interferometry.

First, pores and asperities were characterized from a top-view analysis. The density of pores is typically about 25-35%. Each pore is isolated with solid polyurethane and the pore diameters are on the order of 30-50µm. The pores temporarily hold fresh slurry and provide space for localized mixing of slurry. Pore separation is on the order of 20-100µm, with wall-like structures between each pore. The uppermost features of the wall structure are called asperities, which make direct contact with wafer during CMP. From a bearing ratio analysis at 1%, the asperity size was defined as 20-100µm (Figure 2).

From a side-view analysis of the pad, the topographies can be functionally characterized. Generally, the pad is composed of two layers: a top layer made of a hard material for the purpose of maintaining local planarity, and a bottom layer made of a soft material for global planarity, that is, uniformity. The soft layer helps with the conformal contact of the hard layer with the wafer. Each layer is about 1.3mm thick. A wafer is placed face side down on a top of hard layer during polishing.

As a result of conditioning, peaks and valleys are generated in the pad surface. The distance between peaks matches well with the pitch of the diamond grits on the conditioner. Diamond grits plow valleys into the pad during the conditioning process. The peak-to-valley dimension (height) is around 60-100µm and matches the height of diamond grits above the surface of the conditioner. Based on the analysis, a simplified pad model has been developed using a spring model to explain asperity behavior. In conventional pads, asperities have non-uniform height distribution due to intrinsic conditioning. When a wafer contacts pad during polishing, higher asperities are exposed first and get stress concentration resulting in over yield stress and deformation. So, conditioning is still unavoidable to resurface the deformed asperities. Figure 3 illustrates a simplified pad model and asperity deformation on a conventional pad.



Fig.1 Characterization of Conventional Pads (SEM and White light interferometry)



Fig.2 Bearing Ratio Analysis at 1% and Asperity Sizes(20-100µm)





PAD DESIGNS

Based on characterization of conventional pad, SMART Pad proposes a novel polishing pad. Instead of limited asperities with non-uniform height distribution, SMART Pad has multiple asperities with uniform height and contact area. In addition, hard layer is formed as segments sitting on soft layer. When pressure is applied on pad, the hard layer segments are moving down, and the soft layer absorbs all stresses. As a result, the top of hard layer is self-aligned, and it could avoid stress concentration which is a scratch resource. Figure 4 illustrates the difference between conventional pad and SMART Pad. Figure 5 shows pressure analysis with FEA showing stress absorbance on soft layer.

To design the micro feature array, computational fluid dynamics (CFD) was used to understand slurry flow. Several designs with multiple parameters were tested and slurry flow efficiency was investigated using CFD method. Based on its results, the array of micro features were designed to maximized slurry flow guided on top of hard layer segments.



Fig.4 Conventional Pad with Point Contact VS. SMART Pad with Surface Contact



Base Geometry



Equivalent Stress(Mpa)





Fig.6 CFD Slurry Flow Analysis on SMART Pad

SMART PAD DATA REVIEW

Figure 7 shows planarization and uniformity performance of SMART Pad compared to a conventional pad. In both oxide and STI pattern wafers, extreme planarization and uniformity performance was realized in within wafer non uniformity (WIWNU) and within die non uniformity (WIDNU).

Figure 8 shows removal rate performance in a ceria-based slurry. SMART Pad shows 1.5X faster removal rate compared to a conventional pad in various PxV conditions.

Excellent edge exclusion performance was measured in within wafer removal profile with 1mm edge exclusion (Figure 9). With 1mm edge exclusion, 5.3% uniformity was obtained, and edge removal data is almost same range as center area, which is a promising profile for edge exclusion requirement.

To meet life time requirement, a 20hour marathon test was performed with a ceria based slurry using G&P Poli 762 and 12 inch TEOS wafer. Removal rate was sustained for 20 hours without a conditioning. Pad feature wear amount was controlled around 3% without any feature degradation. Figure 10 describes detail data of marathon test.



Fig.7 Planarization and Uniformity









Fig. 9 Removal Rate Profile with 1mm Edge Exclusion



Fig. 10 20 Hours Marathon Test (Removal Rate, Pad Wear and Feature Profile)

CONCLUSIONS

SMART Pad introduces a novel conditioning free pad with design rules which results in exceeding performance in removal rate, scratch reduction and planarization. Designed micro features enable SMART Pad to provide customized pad patterns according to customers' requests. SMART Pad looks forward working together with CMP colleagues to understand the fundamentals of CMP by designing pad surface.

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