# Effect of Brush Cleaning on Post CMP Defects

Hong Jin Kim hongjin.kim@gf.com

### INTRODUCTION

Chemical mechanical polishing has been employed in semiconductor device manufacturing for several decades due to its benefit to wafer planarization. However, defect generation from CMP process is inevitable, and it has become everlasting challenge as yield detractor. Sources of CMP-induced defects were known as polishing by-products such as abrasive particles, pad debris, polished materials, and tool particles. However, recent studies suggest that brush cleaner module could contribute to the defect generation sensitively [1-3]. Hence, interests in brush cleaning process and its fundamentals draw a lot of attention to the industry. Accordingly, brush characterization is actively performed by industry as well as academia [4-6]. Brush cleaning is complicated process which involves physical contact, cleaning chemistry, chemical flow and dynamics, wafer surface charge, and wafer surface topography. Moreover, its particle removal capability is strongly influenced by adder defects by brush itself, which is difficult to interpret post brush cleaning defect behavior. In this study, effect of brush cleaning conditions on defect generation is investigated. Results from the study underscore importance of wafer surface charge as determining parameter to post brush cleaning defects.

# BACKGROUND

Brush scrubber cleaning is known as highly effective cleaning method by its direct contact with wafer. High pressure physical cleaning can remove most particles in association with appropriate cleaning chemical. However, defects removed by brush are loaded in the brush, resulting in defect re-deposit to the wafer, which is called brush-induced defect or cross contamination [1-2]. Examples of brush-induced defects are shown in Fig. 1. The most commonly observed defects from brush are organic residue and abrasive particles as shown in Fig. 1. As defects are loaded in brush and re-deposit to the wafer, optimized brush conditioning can improve brush-induced defects. However, it is not fully understood how defect removal and cross contamination occur at the same time during brush cleaning.



Fig.1 Defects from CMP in-situ brush cleaner (a) and (b) are organic residues, and (c) is abrasive particles

# EXPERIMENTAL

Both blanket oxide wafers and short loop (SL) pattern wafers are used to investigate brush cleaning effect on defect generation. As-deposit blanket oxide wafers and pre-polished SL pattern wafers are processed with brush cleaning only without polishing. Brush and cleaning chemical in this study is commercially used one in the semiconductor manufacturing. Alkaline cleaning chemical is used for brush cleaning and its oxide etch rate is negligible. Post brush cleaning wafers are inspected by defect inspection tool and SEM review identifies each defect automatically. Pre and post brush cleaning wafer defect maps are compared to confirm particle removal efficiency as well as cross contamination defects. Experimental procedure is depicted in Fig.2. Blanket oxide wafers are characterized by mercury probe after brush cleaning.



Fig.2. Experimental procedure

# DISCUSSION

Effect of brush gap on post brush cleaning defect is given in Fig. 3, which is behavior of adder defect (cross contamination) with respect to brush gap. Defect removal efficiency is also plotted in the same figure. As shown in the Fig.1, most of adder defects are organic residues and abrasive particles. Brush gap is defined distance between brush nodule and wafer surface, and it is negative value since brush presses wafer surface. Thus, smaller brush gap indicates that higher pressure, larger contact, is applied to the wafer surface. Therefore, brush gap C in the Fig.3 is the condition that the highest pressure is applied to wafer surface. Result from Fig. 3 (a) suggests more defects are transferred to the blanket oxide wafer significantly as brush gap decreases. However, adder defect from SL pattern wafer has not changed much regardless of brush gap as shown in Fig. 3(b). Defect removal efficiency with respect to brush gap showed different behavior from adder defect. For blanket wafer, particle removal efficiency is the lowest at brush gap B. However, for SL pattern wafer, brush gap B condition has the highest particle removal efficiency.





Post brush cleaning wafer is characterized by mercury probe. Mercury probe measures surface capacitance that is indirect measurement of surface charge amount. Cleaning chemical in this experiment is alkaline, therefore, blanket oxide wafer, organic residue and abrasive particles (SiO<sub>2</sub> in this study) are negatively charged. Fig. 4 summarizes adder defects with respect to surface charge (capacitance) and brush gap. Adder defect count and capacitance are normalized. Smaller brush gap leaves more defects on the wafers. And wafer surface with higher capacitance has lower defect/transfer from brush to wafer surface. Effect of surface charge plays a pivotal role in defect generation during brush cleaning. The reason why blanket wafer adder defect behavior is different from SL pattern wafer is explained by surface charge. SL pattern wafer has more materials exposed to brush and surface charge effect is less than blanket oxide wafer.



Fig.4 Normalized adder defect with respect to surface capacitance and brush gap (brush gap condition: A>B>C)

Brush cleaning time and brush lifetime experiments are also conducted. As well known, early brush life showed worst defectivity, and defect count decreases as brush life increases. There is optimum brush cleaning time to minimize adder defects. Short brush cleaning time is not sufficient to remove defects; however, longer brush cleaning time leaves adder defects on the wafer. Combined effect of defect removal and adder defect results in V-shape behavior of defects with respect to brush cleaning time.

# CONCLUSIONS

From the results in this study, importance of wafer surface charge is underscored, and provide experimental evidence of brush cleaning mechanism. Both physical contact and surface charge during brush cleaning are responsible for particle removal as well as particle transfer from brush to wafer. As a new brush characterization, mercury probe is introduced in this study. Result from mercury probe characterization showed good correlation of surface capacitance (or surface charge) with adder defects by brush. Brush cleaning modulates wafer surface charge, and brush cleaning condition strongly influence adder defect generation. Defect removal, defect adding, and wafer surface charge change are simultaneously occurring during brush cleaning, therefore combined effects determines post brush cleaning defectivity. Further study how brush cleaning modules wafer surface charge will provide clues on brush cleaning development.

# REFERENCES

[1] HJ Kim, et al., Study of the cross contamination effect on post CMP in situ cleaning process, Microelectronic Engineering 136 (2015) 36–41

[2] HJ Kim, M Rovereto, Effect of brush cleaning on defect generation in post copper CMP, Microelectronic

Engineering 261 (2022) 111808 [3] HJ Kim, et al., A new approach to the formation mechanism of tungsten void defect in Chemical

[3] HJ Kim, et al., A new approach to the formation mechanism of tungsten void defect in Chemical Mechanical Polishing, ECS Journal of Solid State Science and Technology, 7 (11) (2018) P693-P697 [4] J.H. Lee, et al., Comparative evaluation of organic contamination sources from roller and pencil type PVA brushes during the post-CMP cleaning process, Polymer Test. 90 (2020) 106669.

[5] J.H. Lee, et al., A breakthrough method for the effective conditioning of PVA brush used for post-CMP process, ECS J. Solid State Sci. Technol. 8 (6) (2019) P307–P312

[6] Bradley Withers, et al., Environmental effects on post-CMP PVAc brush releasable contamination and break-in optimization for advanced logic and memory technologies, ECS J. Solid State Sci. Technol. 8 (12) (2019) P794–P798.

Corresponding Author: Hong Jin Kim Tel: +1 315-268-2336 E-mail: Iboyea@clarkson.edu Clarkson CAMP, P.O. Box 5665 Potsdam, NY 13699-5665, USA