Copper Metal Loss in Nanometer Fine Features during Chemical-mechanical Planarization

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INTRODUCTION

Being a technically important yet chemically active metal, Cu is susceptible to corrosion in wet environment such as in CMP. By nature, controlled electrochemical reactions is an imperative part of Cu CMP removal process. As the industry continues to move towards advanced technology nodes with shrinking geometry, the capacity of fine Cu features a few tens of nanometers wide to withstand the electrochemical attack during CMP becomes questionable. In this study, significant Cu metal loss is reported on isolated Cu vias after CMP. The amount of Cu loss can vary from 10% to 80% of the entire via height. Partition experiments suggest every sub step in Cu CMP contributes to certain amount of Cu loss with post brush cleaning accounting for more than half of it. Potential solutions to the problem and new opportunities for CMP consumable and equipment development will be proposed.

BACKGROUND

In semiconductor industry, the continuous drive towards fine geometry in advanced technology nodes imposes pressing challenges to all process technologies. Inevitably, the tolerance for defectivity becomes lower as the pattern dimension shrinks to nanometer geometry. For CMP, this means that any FM, residue, scratch, or corrosion at nanometer scale would induce serious yield loss and reliability issues.

Inevitably, the electrochemical nature of metal CMP process exposes the propensity of metal corrosion, whether the metal involved is Cu, Co, or W. In fact, corrosion is a necessary mechanism of the metal CMP removal process, just that it ought to proceed in a controllable manner to facilitate metal removal without excessive chemical attack, leading to metal loss. As illustrated in Fig. 1, metal corrosion during CMP can be galvanic in nature in which the delta in open circuit potential (OCP) drives the corrosion of a chemically more active metal (e.g., Cu) preferentially over that of a more inert metal (e.g., Ta), when both are exposed to an electrolyte (e.g., slurry) simultaneously. It can also occur in form of chemical etching when, for example, local high concentration of residual oxidizer on wafer surface leads to spontaneous corrosion of metal. The extent of corrosion or metal loss depends on factors such as pH, oxidation potential of the metal, the nature of the surface passivation oxide, electrical conduction of electrolytes (e.g., slurries), and exposed area ratio (in the case of galvanic corrosion) …etc.

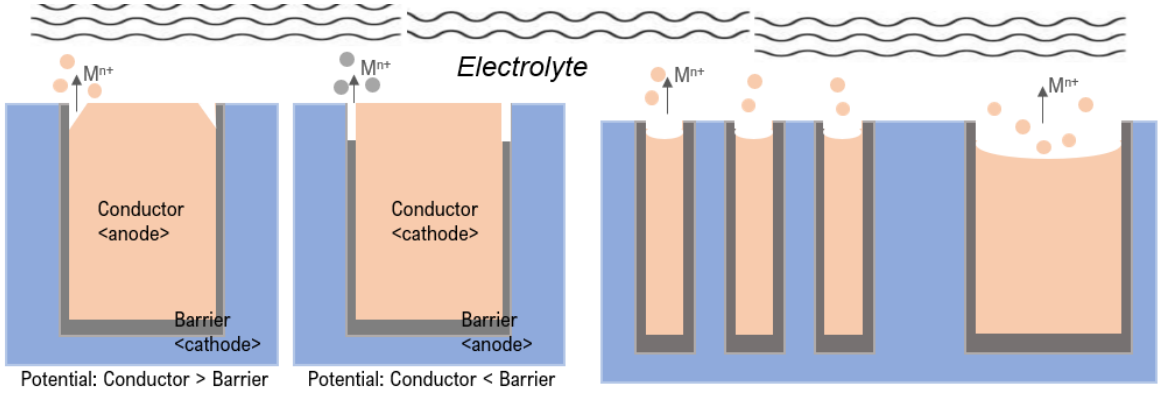

Fig. 1: Cu metal loss due to galvanic corrosion (*left*) and chemical etching (*right*).

Most slurries and clean chemicals for metal CMP are formulated with corrosion inhibitor, e.g., BTA or its variants, and operated at the pH regime where metal surface is passivated with a stable oxide layer. Commercially available slurries and clean chemicals have been adopted successfully to sub-7nm metal

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CMP in HVM environment. However, in this contribution, we report a phenomenon of excessive metal loss post CMP in sub 3nm Cu interconnects of fine geometry. Extensive partition experiments were carried out to isolate the sub process steps responsible for the metal loss. Potential mechanisms involved will be discussed and counter measures to mitigate such phenomenon will be proposed.

EXPERIMENTAL

All CMP experiments were conducted in 300mm commercial polishers with 2-platen process unless specified otherwise. A commercially available high selectivity silica slurry at pH ~ 7 was adopted to polish Cu overburden to end-point plus a certain % of overpolish time. A fixed time polish step with a silica-based barrier slurry (pH ~ 9.5) was performed on the 2nd platen to drive to target thickness. This was followed immediately by an on-platen 5-methylbenzotriazole (5MBTA)[1] rinse step and high pressure DIW rinse before the wafer was transferred to cleaning station. Post cleaning process contains two-stage PVA brush scrubbing steps with a commercially available alkaline clean chemical (pH ~ 10), followed by IPA drying.

The Cu interconnect structural wafers used in the current study are single damascene isolated or fully landed vias with Ta/TaN barrier and low-*k* dielectric, all with CD < 25nm. Post CMP top-down SEM inspection was used to look for sites of metal loss. AFM scan was then employed to determine the amount of recess (loss) which was confirmed by cross sectional TEM later.

RESULTS

A Cu wafer that ran through the full process-of-record (POR) CMP process was subjected to AFM scan across multiple via patterns as shown in Fig. 2. The amount of metal recess is about 11nm from the traces. Cross sectional TEM further confirms the recess is indeed the result of Cu metal loss.

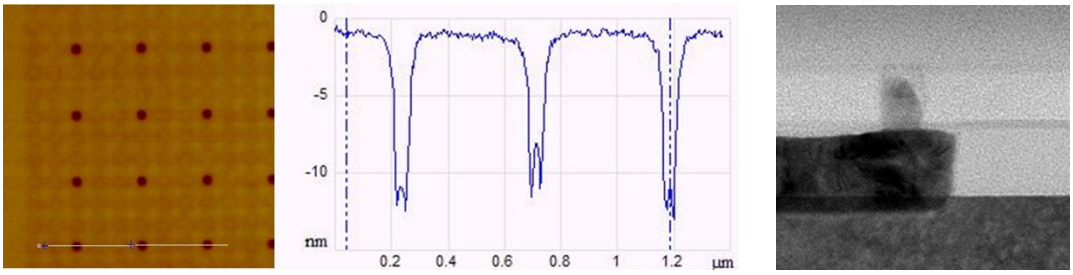

Fig.2: Metal recess in fine Cu vias after CMP as suggested by AFM scan and confirmed by cross-sectional TEM picture.

As a quick first response to address such severe Cu metal loss, a wafer was processed with 2X longer on-platen 5MBTA rinse in the hope for better protection against Cu corrosion. Extensive top-down SEM inspection was performed on the same specific isolated via structure on 39 dies across the wafer. However, the result as shown in Fig. 3 suggests no difference in the amount of Cu loss by doubling the BTA rinse time. The inspection result was later confirmed by AFM scan which shows no statistical differences in the amount of recess between POR and 2X longer 5MBTA rinse.

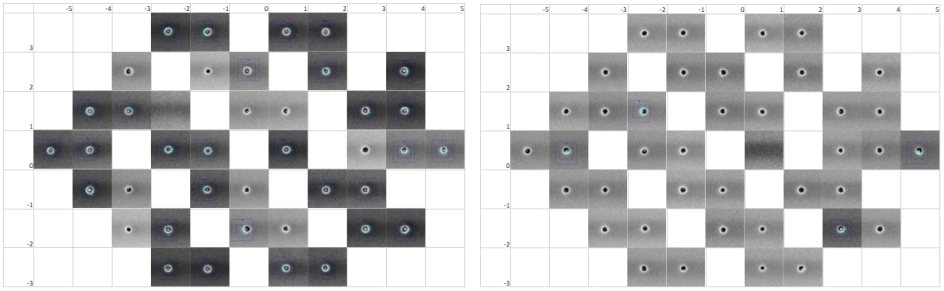

Fig. 3: Top-down SEM inspection on isolated Cu via patterns on 39 dies across a POR wafer (*left*), and a wafer that received 2X longer post polish 5MBTA rinse (*right*).

To study the chemical effects on Cu recess, 3 other barrier slurries of the same pH (9.5) as POR and 1 additional alkaline post clean chemical of pH ~ 10 were selected for experiment. As an additional condition, 5MBTA was replaced by DIW during on-platen too. The amount of Cu recess from this study was summarized in Fig. 4.

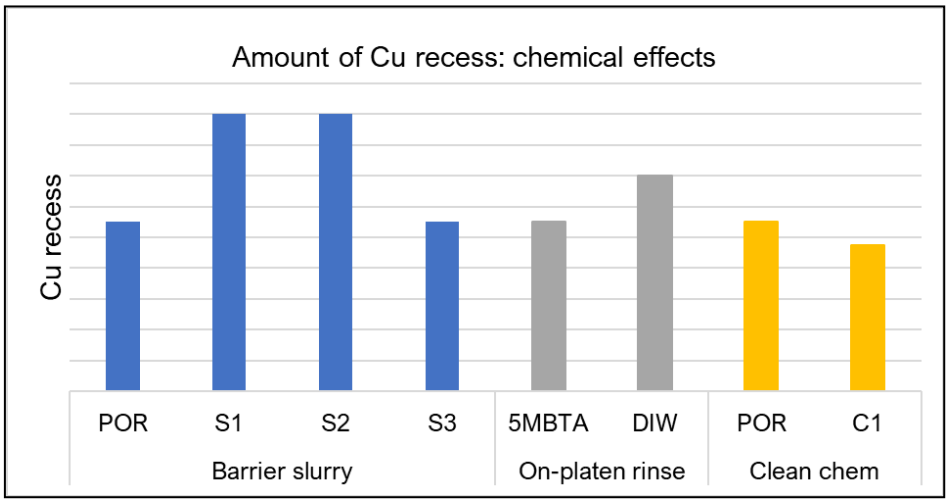

Fig. 4: Effects of barrier slurry, on-platen rinse, and post CMP clean chemical on Cu recess.

The amount of Cu recess does vary among the 4 barrier slurries tested, despite of their same pH. Differences in their additives such as oxidizer, chelating agents, inhibitor…etc. could have played a role here. DIW-only post polish on-platen rinse induced higher Cu loss, as expected. Interestingly, C1, a post Cu CMP clean chemical used in HVM offers slight reduction in Cu loss. The result clearly demonstrates that post CMP cleaning chemical itself can also modulate the amount of Cu loss.

In order to isolate the process steps responsible for Cu loss, a series of post CMP cleaning partition experiments were conducted. The amount of Cu loss was determined by AFM scan across unlanded ("dummy") and fully landed vias on wafer center and edge, as shown in Fig. 5.

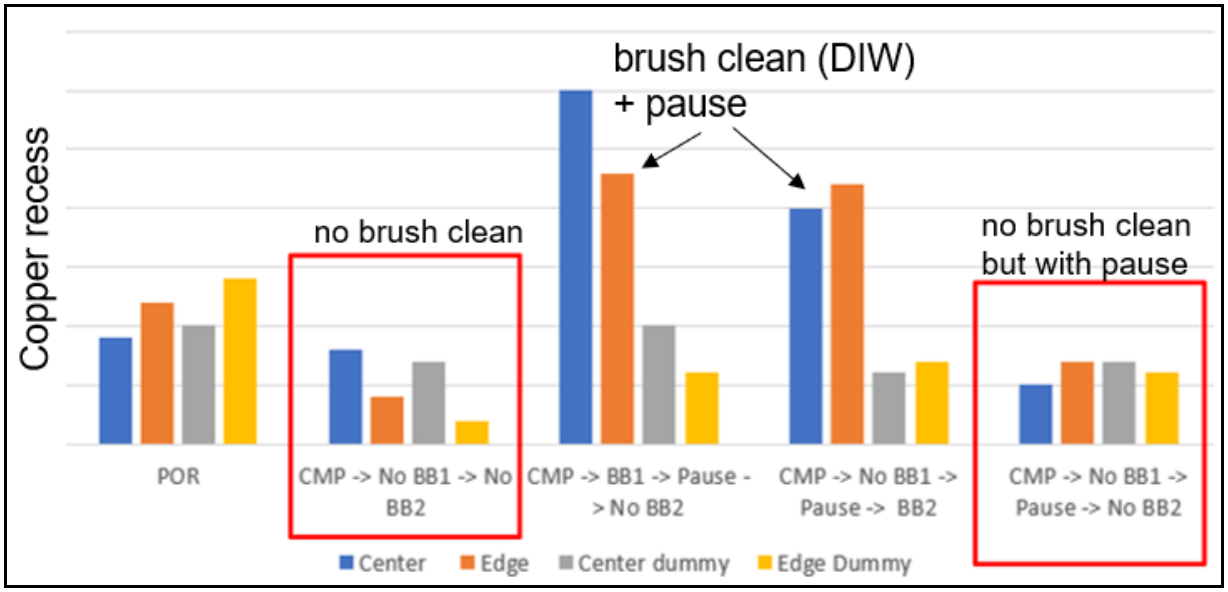

Fig. 5: Post CMP clean process partition showing varying amount of Cu recess. Dummy = unlanded via.

Interestingly, as a group, “no brush clean” wafers show the lowest amount of Cu recess. In this case, wafers were removed from the barrier polish platen right after they finished 5MBTA and high pressure DIW rinse. No further handling of wafer or any cleaning steps were performed. When the wet wafers were paused in the load cup for about 1 min after being removed from platen, however, the amount of Cu recess increased again. When wafers were subjected to DIW-only clean through in either one of the brush boxes (BB1 or BB2), the amount of Cu recess was elevated over those receiving no brush clean, with or without pause.

Also observed from Fig. 5 is that unlanded (dummy) vias exhibit less Cu loss than fully landed vias across all experimental conditions. This implies that for landed vias, the electrical conduction path through the connection with the Cu structure underneath may have exacerbated the corrosion, when the vias are immersed in electrolyte.

As a further partition, an additional wafer was polished to Cu endpoint (EP) only, i.e., without Cu OP and barrier polish, run through POR brush clean and drying process, and subjected to AFM scan. Compared with POR, this Cu EP wafer showed higher amount of recess as depicted in Fig. 6. Part of the increased Cu loss on this wafer may have resulted from elevated galvanic effect at Cu EP, when Cu and Ta/TaN on the field were both exposed to residual slurry, DIW, and later, brush clean chemical during post clean.

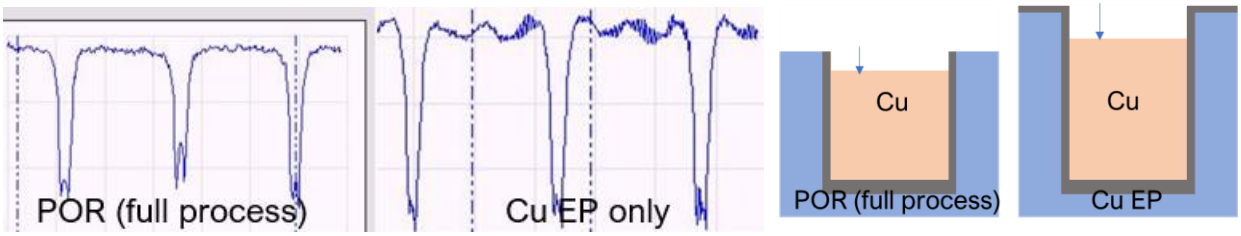

Fig. 6: AFM traces over Cu vias of POR *vs* Cu EP only wafers (*left*); and illustration of the difference in amount of Cu recess between the 2 wafers. (*right*).

Results from the above CMP process partitioning experiments suggest that every sub step in Cu CMP is responsible for certain amount of Cu loss. Basically, corrosion commences as soon as Cu overburden is removed, and it worsens throughout the entire CMP process until Cu wafer is dry and back in the FOUP. Among the most intriguing findings is that wafers bypassing the entire post CMP clean process (i.e., “no brush clean” wafers in Fig. 5) show only about 1/3 of Cu loss, compared with POR. The types of barrier slurry, on-platen rinse chemical (e.g., inhibitor like 5MBTA), and post clean chemical can all modulate the signals as well.

DISCUSSION

The findings from CMP experiments clearly demonstrate the metal loss in Cu vias can be modulated by both the process sequence involved and the chemicals used. This is further compounded by the geometry and design of the Cu vias, plus their surrounding environment on the wafer.

As mentioned before, the mechanism responsible for metal loss can be galvanic in nature. The observation of deeper Cu recess on wafer polished to Cu EP seems to support such hypothesis. As illustrated in Fig. 7, the galvanic potential per unit area along the Cu/liner interface increases with shrinking via width. Consequently, smaller vias will experience stronger galvanic effects in electrolytes and the Cu loss (“notch”) on the edge would eventually coalescence into a continuous segment of missing Cu.

Charging effects can be another mechanism too. Ions and electrical charges build up around copper features during CMP. Current begins to flow when the wafer is exposed to conducting solution (e.g., slurry, DIW, clean chemical…etc.), leading to Cu loss. Likewise, chemical etching as shown in Fig. 1 can play a role too. However, both effects could not explain why no excessive metal loss is observed on Cu lines (*vs*. vias) of the same width.

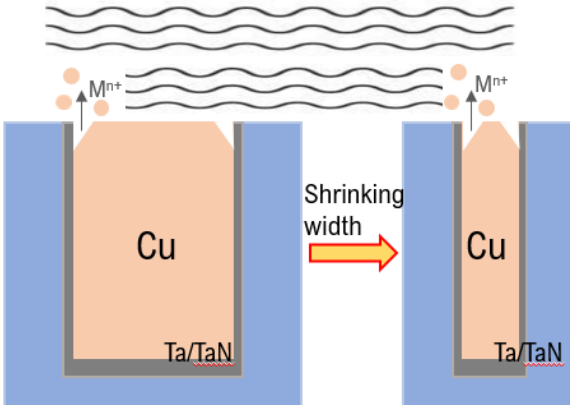

Fig. 7: Metal loss from galvanic corrosion between Cu and Ta/TaN liner.

Among the most intriguing findings from the partition experiments is the fact that “no brush clean” wafers suffer the least amount of Cu loss - less than half of that in POR. In general, the shorter the wafer is exposed to wet environment (e.g., with residual slurry chemistry, DIW, or clean chemical), the less the amount of Cu loss. Besides the existence of DIW and aggressive chemistry, the air inside the CMP tool ambient provides abundant source of oxygen which is a fundamental element in metal corrosion. The galvanic and charging effects mentioned above may have been exacerbated in such wet and oxidizing ambient to cause severe Cu loss.

Provided the above observation and reasoning, a few counter measures against post CMP Cu loss can be projected. From chemistry point of view, extra efforts should be given to the electrochemical characteristics of both Cu and barrier slurries to reduce the corrosion rate under an oxidation potential without compromising polish performance. The same principle applies to the formulation of post clean chemical, which should protect Cu surface and Cu/liner interface long enough before particles and residues are cleaned off wafer surface. In fact, as the current study suggests, reformulating post clean chemical for Cu or metal protection could be even more critical in mitigating Cu loss. Meanwhile, the search for a more effective corrosion inhibitor becomes more urgent as 5MBTA is insufficient to prevent the severe Cu loss.

Perhaps equally important is the effort to minimize the exposure of fine metal features to DIW and oxygen during CMP. In fact, a previous study suggests DIW that contains high concentrations of dissolved oxygen can etch Cu.[2] The ideal situation would be modifying the wet environment into one that is more protective against Cu corrosion (e.g., in the slightly alkaline regime). In fact, the use of functional water where NH_4OH is added into DIW has demonstrated the feasibility to reduce metal corrosion in semiconductor processing.[3] Similarly, purging, or repelling oxygen away from inside the CMP tool ambient can also help reduce the degree of corrosion.[4]

From process sequence point of view, in principle, the transient time between polish platens and from platen to cleaning module should be minimized. In addition, the time spent in the cleaning module, including chemical brush clean and DIW rinse, should be kept as short as possible. Some help from CMP tool design and algorithm would be needed here.

Since heavy Cu loss is mostly observed on fine isolated vias in single damascene structure, some circuit design optimization effort can alleviate the problem. However, isolated vias are not uncommon even in dual damascene Cu. In addition, heavy Cu loss on a single via was also observed when it is connected to a large feature based on a separate study. Lastly, the continuous shrinking design rule for interconnects will only exacerbate the problem as the industry marches ahead to advanced technology nodes.

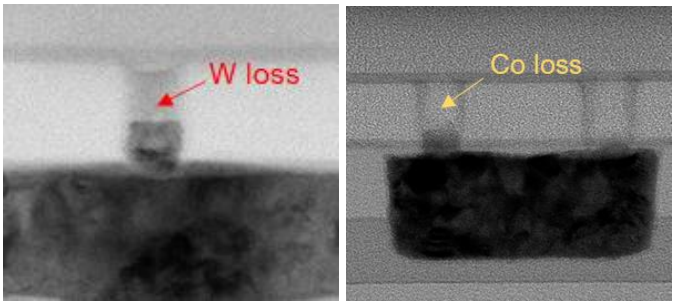

Fig. 8: Cross sectional TEM pictures showing excessive W loss (*left*) and Co loss (*right*) after CMP.

A final remark on the subject of post CMP metal loss is that we observed similar phenomena with W and Co CMP, as shown in Fig. 8. In this case, exactly the same test structures and wafers were used in the study except Cu was replaced by W or Co. Apparently, the problem exists across common metals used in MOL and BEOL processes. The same extensive efforts in CMP slurry/chemical formulation, wet environment modulation, tool ambient control will be required to address the issue.

CONCLUSIONS

In this study, significant Cu loss after CMP on sub-30nm features is reported. This phenomenon occurs mainly on isolated vias with single damascene integration scheme. On-platen wafer rinse with 5MBTA after barrier polish does not protect Cu from heavy loss. Results from CMP partition experiments suggest every sub process step contributes to Cu loss, from Cu polish, barrier polish, post rinse, all the way to post cleaning. Post CMP clean process is responsible for more than half of the Cu loss. In general, the longer the wafer remains in the process sequence, the more severe the Cu loss will be. The same phenomenon is also observed after W and Co CMP with the same isolated vias structure.

Potential solutions to the problem would include re-formulating slurries & clean chemicals for better protection against corrosion. The use of functional water and tool ambient control could offer the opportunities to mitigate Cu loss. Reducing wet transient and process time through CMP tool design and algorithm change may provide additional path to reduce Cu loss.

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