Evaluation of design dependencies in STI-CMP for layout diversification

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Abstract

The process result of chemical mechanical polishing (CMP) is highly dependent on the chip layout and process setup. Characterization of design dependency is demonstrated for three different consumable setups in the area of shallow trench isolation (STI). Special focus is laid upon the process results for uncommon layouts as such is crucial for device diversification. Detailed evaluation of the process results for extended trench oxide regions demonstrates the subtle but crucial differences between different consumable setups under study. Lateral erosion of patterned areas in test chips points at possible homogeneity problems for device arrays in their outer regions.

Introduction

Diversification in the IC industry results in an increasingly broad range of different layouts and designs. It is desirable to make a high number of these without adjusting the fabrication process. As chemical mechanical planarization (CMP) is a process, which results depend highly on the chip layout, the diversification trend poses a major challenge for CMP [1,2]. To tackle this challenge, it is necessary to evaluate the layout dependency of a specific CMP process. Variation of polish parameters and consumables can help expanding the process window, but clear evaluation methods for these procedures have to be defined. Based on the measured design dependency certain design rules are defined: as strict as necessary as loose as possible. Anyway, the concept of design rules is a simplification that sometimes result in excessive constraints for layout diversification. Especially in advanced nodes this results in frequent design rule violation requests – for handling of such it is beneficial for a CMP engineer to have general data of design process interactions in- and outside of the process window on hand.

For fundamental data about the design impact on STI-CMP result, it is necessary to look at basic model structures. Density and pitch variations of line/space structures are common examples of these, furthermore it is desirable to study the impact of various lateral extension of homogeneously patterned regions [3]. Such work is commonly carried out using designated short flow wafers with STI test chips [4-6]. Usual process discrepancies of STI-CMP include the loss of field oxide in the trench itself, erosion of nitride in the designated device area (active area) or remains of oxide on top of the nitride stop liner [7] (see Figure 1). For a working successive nitride strip process active oxide residuals have to be prevented. However, trench oxide loss and nitride erosion are equally important as they may result in a variation/degradation of device performance. All the mentioned effects are design dependent and an optimization of both process and design is needed to balance the expectable process discrepancies.

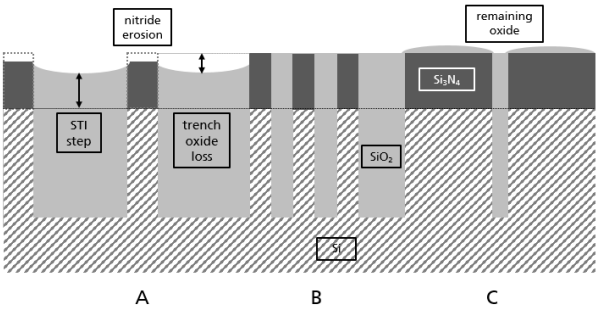

Figure 1: Schematic STI layout showing the process target parameters nitride erosion and trench oxide loss resulting in STI step height. Low density (A) usually results in trench oxide loss and nitride erosion, high density (C) poses the risk of remaining oxide, while medium density (B) is processed smooth [8].

To enable a design team to provide layouts that are favorable for CMP, it is necessary to evaluate the principal design dependency of a CMP process [8], which is highly affected by choice of process parameters and consumables. An alternative understanding is the optimization of the CMP process to certain (increasing) design demands: If a design rule violation is conceivable, CMP

engineers may be asked for the consequences. For both cases (evaluation of the design dependency of a specific CMP process as well as rating of process window violations), it is necessary to have fundamental CMP performance data. Typical commercially available test wafers often lack structures equivalent to advanced nodes and/or are restricted to typical design rules. It is common practice to combine a multitude of rather coarse structures on a test chip, resulting in lateral interactions hard to judge. In this contribution we worked with test structures designed to intentionally violate design rules present in a current minimum dimension node fabrication. Focus is laid on a limited number of homogeneous regions of small feature size, allowing for evaluation of lateral interactions. Three fixed CMP setups with different consumables and process parameters were compared on structured test chips. Based on the acquired data it is possible to judge the different design dependency of the processes under investigation as well as predict consequences of design rule violations.

Experimental

Short flow 300-mm-wafers with two separate STI test chip designs were processed at GlobalFoundries. After oxide fill of the various STI test structures the wafers were sent to Fraunhofer IPMS-CNT and polished on an industry standard AMAT Reflexion LK CMP tool. To study the impact of different consumable sets three different setups based on commercially available slurries, combined with recommended pads and conditioners, were used. In a two-step STI-CMP process the first polish step was identical for all wafers, while the second step (stop on nitride polish) was conducted with the variation of consumables. All wafers were polished until a motor torque-based endpoint was detected implying nitride clearing.

Before and after the CMP process the film thickness was measured ellipsometrically (KLA FX100) at dedicated metrology sites or extended pure active or field regions. For access to the surface level of patterned regions the topography of the wafer surface was measured by tactile and/or optical profilometry (KLA HRP340/ Nanofocus µsurf). Due to the size of line/space structures below the wavelength of visible light and the transparency of the film the optical CMP test structure measurements would be falsified. To overcome this obstacle the wafer surface was coated with an opaque 25 nm TaN film. Thickness distribution of the TaN film was tested by multiple SEM cross sections and was found independent of the test chip design.

The used STI test chip layouts consist of squared regions (patches) with homogeneous line/space structures representative for 2x nm dimension. Between individual patches the pitch (line width + space width) and line density (defined as line width/pitch) were varied. In test chip layout A (see Figure 2a) the size of individual patches was varied between 25 and 1200 µm. The film thickness could be measured in the existing pure line and space regions (0 %- and 100 %-line density). The interaction between pure trench oxide patches and the patterned surrounding regions of different line density was object of study for the surface profile measurements. Test chip layout B (see Figure 2b) features a homogeneous size of patches including a dedicated metrology site in the center of a patch. Different individual patches of test chip layout B feature a variation of line density and pitch. Due to the large lateral extension of the patches little impact on the polish result due to adjacent patches is to be expected. The suppression of long-range effects in this design allows for a fast estimation of the surface topography range due to pure density variation.

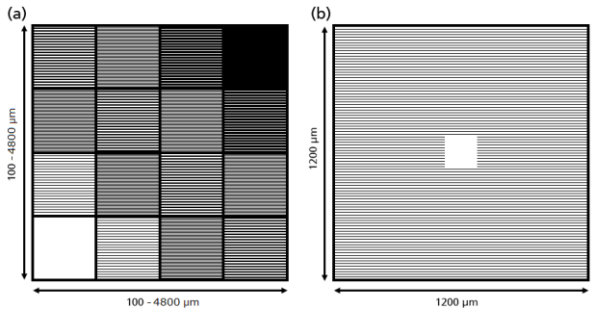

Figure 2: Schematic section of test chip layout used to evaluate the STI-CMP process, variation of line density results in grey scales.

Impact of patch size

Depending on the size of homogeneous patches the polish result can be greatly different. This effect was studied by the analysis of identical patches on different length scales. Critical cases for STI-CMP may be large extended oxide regions, resulting in severe dishing, or large variation in nitride region size as large nitride regions need long polish times to ensure oxide clearing, whilst small patches get eroded. The results for a variation of either pure oxide or nitride patches after STI-CMP with different setups are shown in Figure 3. It can clearly

be seen, that an increasing patch size results in decreasing remaining oxide thickness and decreasing nitride erosion – similar effects have been observed before [5]. If a maximum value for the oxide dishing is defined (e.g., dashed lines in Figure 3a) the test chip results directly indicate a corresponding maximum oxide region size. Comparison of the setups under investigation reveals large differences in the maximum field region size between 50 µm (Setup B) and 600 µm (Setup C). Such values may be far off the classical STI structure size, but may become crucial in the term of add on functionalities.

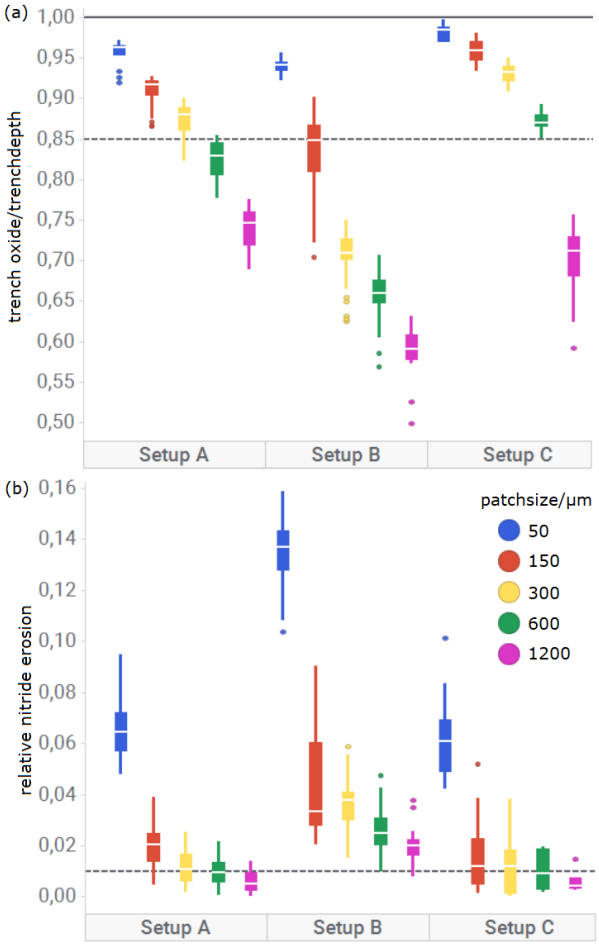

Figure 3: Trench oxide thickness (a) and nitride erosion (b) for different patch sizes after polish with various STI-CMP setups. Horizontal lines are a guidance for the eye and do not represent physical data.

In the case of nitride erosion, it is important to point out, that the maximum pure active patch size determines the oxide clearing and thereby the polish time. Hence, the nitride erosion for smaller patches shown here is only correct for the case of 1200 µm active regions determining the oxide clearing. Nevertheless, some fundamental aspects can be observed here: For all setups under study the 50 µm nitride patch shows highly increased erosion compared to the larger regions. Presumably nitride Patches of 150 µm or larger size behave blanket like, while smaller regions are highly affected by the surrounding regions. For the larger sized patches, it is worth to notice that setups A&B show some decrease of the nitride erosion for size increase from 150 µm to 1200 µm. In the case of setup C, the nitride erosion is approximately constant for 150-1200 µm patches. Regarding the absolute level of erosion, the setup B shows higher values for all studied structures.

Based on the results shown the general trend of increase in oxide dishing and decrease in nitride erosion for larger patch sizes is somehow obvious. Nevertheless, there is no clearer general rule here, different consumable setups result in different behaviors and thereby demand different actions. The design process interactions must thereby be determined for a specific setup in order to evaluate possibilities for unconventional layouts. Dedicated test chips as shown here are an appropriate toolset to do such evaluation. If for example future design diversifications demanded large active (nitride) regions or open areas, the level of risks resulting from these would be a potential question, that would be addressed to the CMP teams. If a design rule based on < 0.15 trench oxide loss was present, a violation of the corresponding design rule would have different effects for different setups: while oxide dishing only increases moderate for setup A and may be acceptable, a stronger impact had to be expected for setup B. For judgement of such future design demands it is thereby required to look at process results outside the conventional design rule window.

Lateral interaction between regions of different density

Extended regions of open space necessarily border to adjacent structured regions for later device fabrication. In our test chip design, the large field regions of varying size were next to regions of 14 %- and 50 %-line density. If we study the topography of the test chip after the CMP process, we observe a clear impact of the field regions on the adjacent structured region (see Figure 4). It is somehow natural, that the CMP process results in a smoothening of the transition between regions of

different topography. Nevertheless, such effects can have a severe impact on the possibility to fabricate device arrays with homogeneous properties. If arrays of active elements with constant properties were to be made, the values shown here would be exclusion zones and thereby define “wasted” chip area. Alternatively, a deviation in electrical property has to be expected for devices in the impact zone of the lateral erosion.

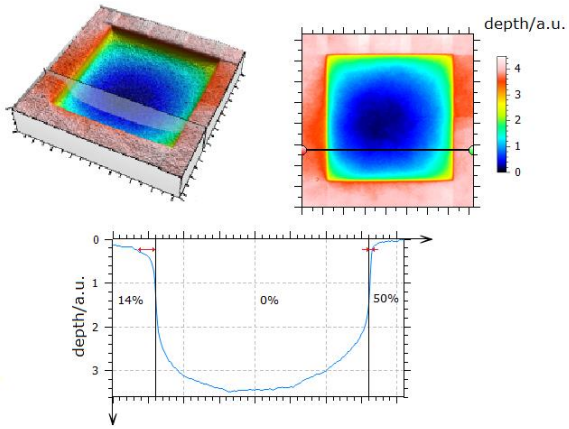

Figure 4: Surface topography of a dishing patch and its surrounding patterned region. The shown cross-section reveals different levels of lateral erosion in the adjacent 14 % and 50 % patch.

The profile of the pattered surface in proximity to the dishing patch is an important property of the CMP result, determining design rules/the possibility to fabricate non-standard layouts. For a qualitative comparison of different STI-CMP setups it is necessary to define a certain figure of merit. In this example we defined a local erosion of 6 % of the nitride layer thickness as a cutoff criterion. The lateral distance from the nominal end of a dishing patch and the beginning of the 6 % erosion region is hereby termed as the lateral erosion value of the CMP process. This value depends on the size of the corresponding dishing patch as well as the density of the adjacent patterned region. Under the mentioned criteria it is possible to derive the lateral erosion values given in Table 1.

Table 1: lateral erosion values in µm for the patterned regions of 14 % and 50 % density in proximity to different dishing patches for the STI-CMP setups under study.

Dishing patch/µm	Setup A (14%/50%)	Setup B (14%/50%)	Setup C (14%/50%)
150	0.7/3	0.2/1	0.2/0.2*
300	16/5.5	10 /6.5	2/1
600	21/18	13/7	3/2
1200	32/25	15/19	32/8

* only 1 nm vertical offset

Based on the data shown, the strong impact of the consumable setup on this figure of merit can be measured. Interestingly the setups under investigation react highly different on a change in dishing patch size. In the case of 14 % density regions setup A shows a constant increase in lateral erosion with adjacent dishing patch size. Setup B has a relatively constant lateral erosion in the proximity to dishing patches > 150 µm. Finally, setup C results in very little erosion except for the large 1200 µm dishing patch with severe effects upon its surroundings.

The comparison of the different densities influenced by the dishing patch does not give a clear picture. The general trend of lower lateral erosion in 50 % density patches compared to 14 % density patches is plausible as higher density of nitride stop regions results in less local pressure for nitride erosion. Nevertheless, some exceptions from this general trend were observed (e.g., in the proximity to the 150 µm patch) were the 50 %-line density region shows higher lateral erosion. This effect is likely due to the relative nature of the value under study: the (vertical) erosion level is not measured absolute in this case, but relative to a constant surface within the patterned region. More severe absolute (vertical) erosion in low density patches does thereby not affect the value of lateral erosion.

The evaluation of the “less common” figure of merit lateral erosion can show differences between consumable setups in another way than the usual dishing behavior. The consumable setups A & C of this study perform almost similar in the size dependent dishing and erosion (see Figure 3). If the lateral erosion in proximity to dishing patches is studied, the process differences become much clearer.

Impact of density

As discussed for the lateral erosion, the density of stop structures (nitride surface) present is a crucial parameter for STI-CMP. In the studied test chips this is reflected by the line density. Based on the test chip layout B it is possible to determine the pure density impact on topography with suppression of long-range interactions. Due to the erosion behavior, regions of different density have a certain topography offset. This topography offset does have an impact on the corresponding performance of devices built later. For a complete evaluation of performance impacting topography, other features such as micro-dishing between individual active regions need to be considered as well. In Figure 5 the relative topography offset is shown for regions of different density. It is obvious, that a homogeneous density (diagonal in Figure 5) results in even topography. For deviations of the perfectly homogeneous density the studied consumable setups perform different. This needs to be considered in design-technology-optimization.

The general performance of the consumable setups under study is somehow similar for setup A & C, showing low topography of ± 5 % of the nitride thickness for small density fluctuations in the high-density region. Setup B on the other hand allows for stronger density fluctuations with remaining low topography if the density is ≥50 %. If the generally more critical cases of low density are considered the difference between setup A & C on the one side and B on the other is also obvious: fluctuations in the low-density range of 30 % have severe effects for the setup B, while they only result in strong topography for setup A & C. This fundamental difference aligns with the previously described low remaining trench oxide for setup B (see Figure 3). Low densities approach the behavior of trench oxide regions, resulting in strong topography.

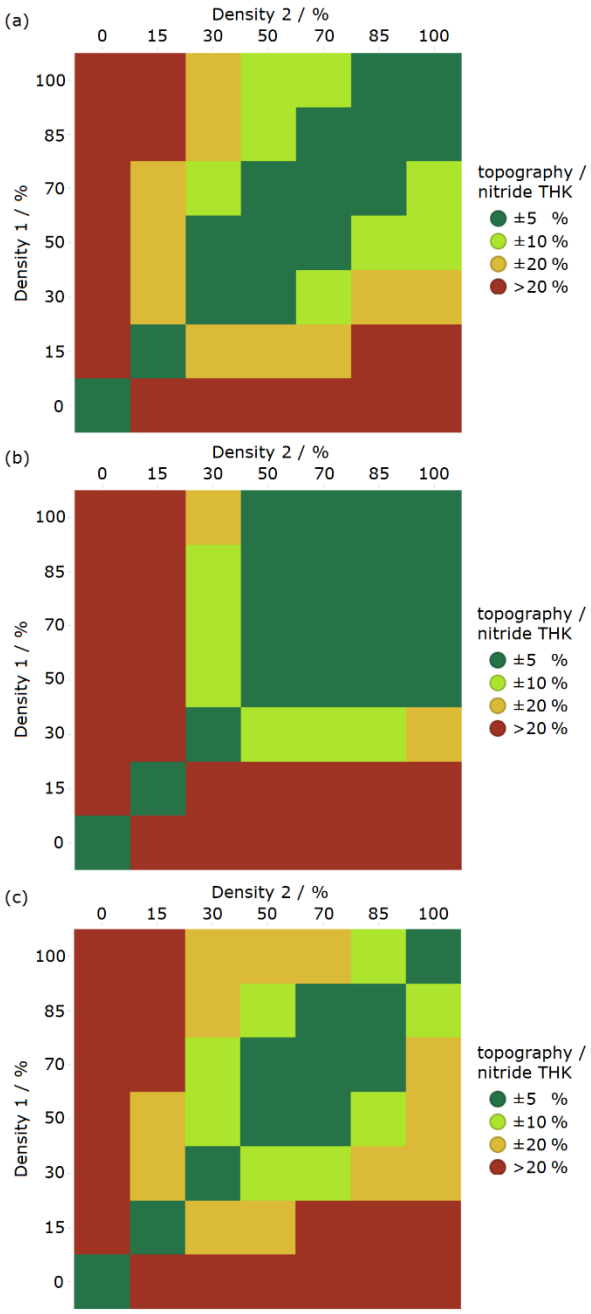

Figure 5: Relative surface topography depending on density regions compared. Image (a), (b) and (c) show the result of the corresponding consumable setups under study.

A design request of increasing the maximum allowed density in a design by ~30 % would have considerably different outcomes for different CMP setups. If the sole density impact on topography is considered, an increase is equivalent to moving in the row of 30 % density 1 towards higher values of

density 2 (see Figure 5). For a maximum density of 50 % the best choice would be setup A, having an unproblematic topography of ± 5 %. For higher maximum densities of 70 % a topography of ± 10 % has to be expected for all setups under investigation. Further increase to 85 % maximum density results in (presumably) problematic topography of ± 20 % for setup A & C, while setup B is still in the ± 10 % region. Such an example illustrates, that the impact of design changes on process results is not trivial. Layout diversification demands for clear datasets on the design dependency of the STI-CMP process result. The consumable setup has a major impact on such design dependency, thus reliable methods for evaluation are needed to judge consumable setups for layout diversification e.g., dedicated test chips.

Summary

For CMP processes in fabrication of non-standard layouts it is crucial to have a deep understanding of design process interactions. In the current work a possible way of evaluation, based on dedicated STI-CMP test chips is presented. Determination of CMP properties in- and outside of classical design windows is necessary to react on inquiries by designers. For evaluation of usage possibilities of CMP setups for diverse layouts a multitude of criteria need to be considered e.g., the lateral erosion. The presented comparison of different STI-CMP consumable setups shows clear differences in design-process-interactions. Such differences also need to be determined to be able to react in an appropriate way on possible supply chain problems and substitute consumables in a running fabrication.

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