

HVM CMP Process Development for Advanced Direct Bond Interconnect (DBI)

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INTRODUCTION

Direct bonding is a spontaneous dielectric-to-dielectric bond at room temperature with a metal-to-metal connection (here Cu-to-Cu bond) by a low temperature batch annealing process (200°C – 300°C). Therefore, the direct bonding process is attractive for heterogeneous integration and has several advantages over the micro bump bonding with solder [1, 2]. Furthermore, the interconnect density and scaling of interconnects is less limited for this metal cap free bonding process. The risk of electrical shorts can be eliminated with this technology, since no solder can be squeezed out from the micro bumps during bonding, which is critical for fine pitch applications. The successful development of wafer-to-wafer bonding by hybrid bonding led into a fast introduction of this technology to high volume manufacturing [3]. Hybrid bond interconnects show excellent reliability and stable microstructure at the Cu/Cu interface, which was already published in recent studies. [4, 5, 6]

The proven direct bonding process flow on 300 mm Wafers at Fraunhofer IZM ASSID is a result of a long-term cooperation with Adeia, Fraunhofer IZM ASSID has licensed the ZiBond® and DBI® technology for the 3D package development. [7]

BACKGROUND

ZiBond is the low temperature homogeneous (e.g. dielectric-to-dielectric) direct bonding technology that forms strong bonds between wafers or die with same or different coefficients of thermal expansion. DBI (Direct Bond Interconnect) is the hybrid bonding technology that include both dielectric and metal-metal bonding. The technology transfer and process qualification of the dielectric-dielectric and metal-metal hybrid bonding at Fraunhofer IZM ASSID on 300 mm Si wafer has been completed. The process uses commercially available process tools from front end wafer processing through bonding.

A crucial preparation step is the chemical mechanical polishing (CMP) of Cu/SiO₂ in order to accomplish low surface roughness and optimal copper dishing. Advanced commercially available CMP consumables are used to achieve state-of-the art planarization including minimal dishing and erosion. This paper presents the latest progress on CMP development for HVM (High Volume Manufacturing) in the industry. The focus is on wafer process stability of surface topography, throughput, and pad life over more than 1000 300 mm wafers.

EXPERIMENTAL

The test structures were built using single layer damascene processes for top and bottom wafers, respectively. A proprietary test chip design was used to develop and qualify the DBI (Direct Bond Interconnect) process. The main feature of the test chip is a daisy chain with 6656 links connecting the top

and bottom die. The critical dimension of the features is a 4 μm DBI via diameter at an 18 μm pitch. The daisy chain was constructed using RDL and DBI layers with damascene metal layers including a Ti barrier material and Cu metallization (Figure 1). The test design can be used for wafer-to-wafer bonding and die-to-wafer bonding.

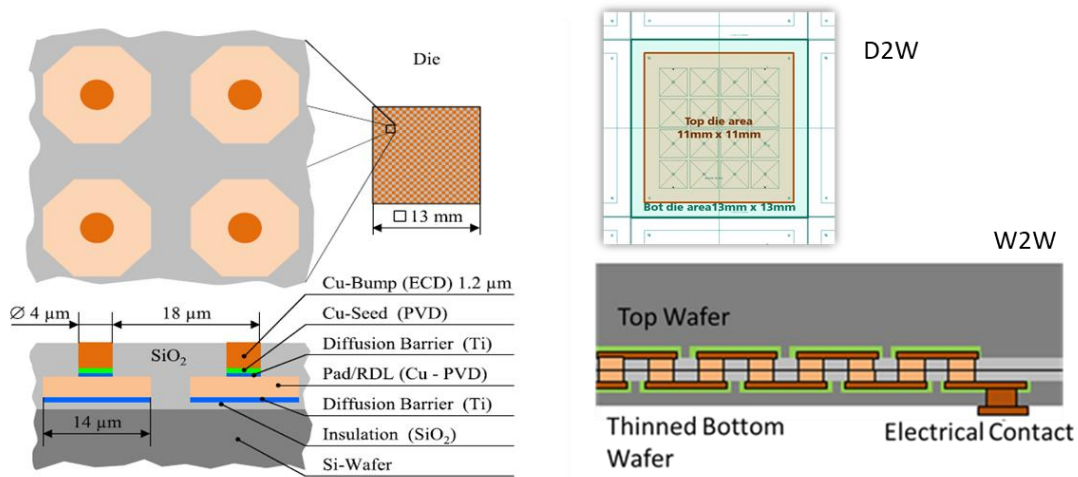


Figure 1. Design and target layer stack for Cu/SiO₂ hybrid W2W bonding and D2W bonding

For the polish process, a conventional CMP tool with 3 polish platens was used (Applied Materials Reflexion LK). In figure 2 the process sequence is shown. After removal of the bulk copper on platen 1 (by use of active endpoint detection) a second copper polish step on platen 2 is performed to reduce the overall copper polish time and increase tool throughput. This polish step ends with an active endpoint detection and minimizes overpolish and allows stopping a Cu polish on the barrier layer with a low copper dishing. The final CMP step to remove the barrier and prepare the direct bond interconnects for bonding was performed on platen 3. All the consumables (polish pads, pad conditioning discs, and slurries for copper and barrier polishes) are commercially available. The integrated Desica Cleaner with a vapor dryer was used for post polish cleaning.

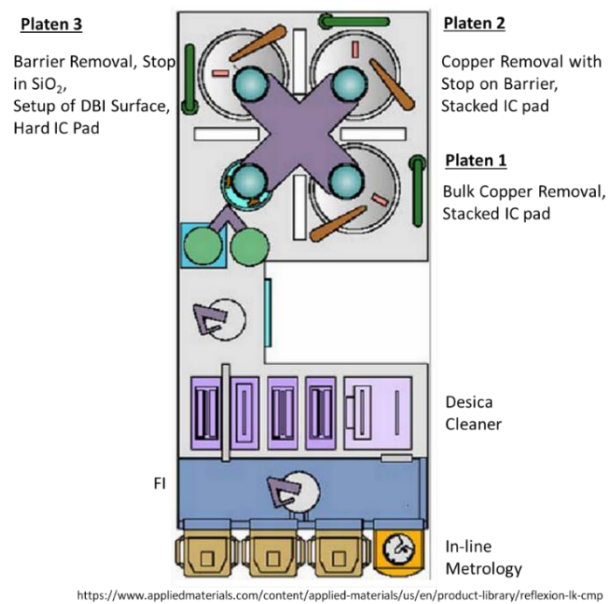


Figure 2. CMP Tool with process dedication for DBI process

The CMP process runs included unstructured and structured wafers with the selected process settings for over 1000 wafers. A structured wafer was polished after every nine unstructured wafers to monitor the removal rates, Cu dishing, and erosion were measured. Process stability of dishing and erosion was studied for over 1000 total wafers polished on a single set of polishing pads since this is a challenge for small via dimensions for hybrid bonding. The post CMP topography was characterized by atomic force microscopy (AFM) on 9 measurement points across the wafer to ensure the dishing uniformity and required roughness for bonding (figure 3 and figure 4).

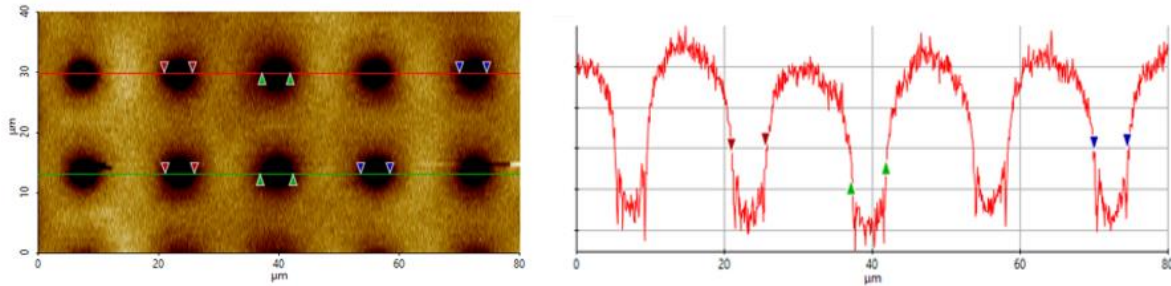


Figure 3: Example of AFM results on a structured wafer with 4 μm copper via and 18 μm pitch (post CMP)

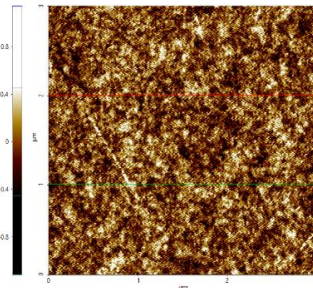


Figure 4: SiO_2 wafer surface roughness ($R_q = 0.25 \text{ nm}$) post CMP [6]

During the extended test run more than 100 structured wafers were polished. AFM results of the standard deviation (SD) of copper dishing as a function of position on the wafer are shown in figure 5 as measured by AFM. The distribution of the copper dishing across the wafer in wafer center (SD = 0.8 nm), \sim half radius (SD = 0.9 nm) and \sim edge (SD = 0.9 nm) is very tight.

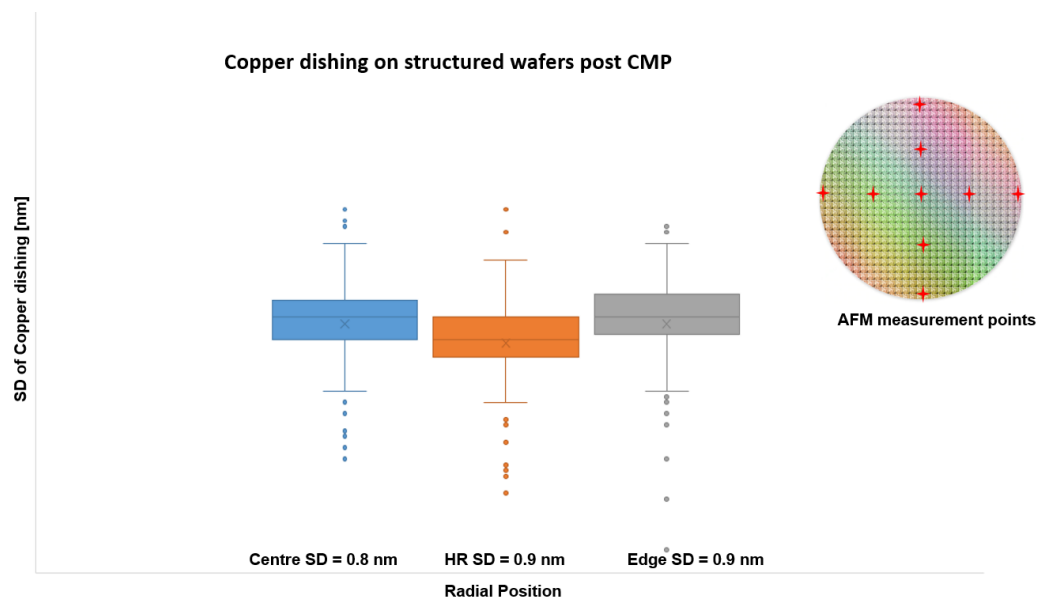


Figure 5: Distribution of copper dishing measured on >100 structured wafers on 9 measurement points per polished wafer

In figure 6 the deviation of the Cu dishing from baseline values is plotted over the pad lifetime is demonstrated. Small deviation of the Cu dishing values is observed during the break in of a new pad and when there are slurry barrel changes; however, the magnitude of the dishing deviation is so small that it does not affect the hybrid bonding results. The slurry was supplied by a barrel which required frequent changes It is notable that no significant change in dishing was observed around the slurry changes.

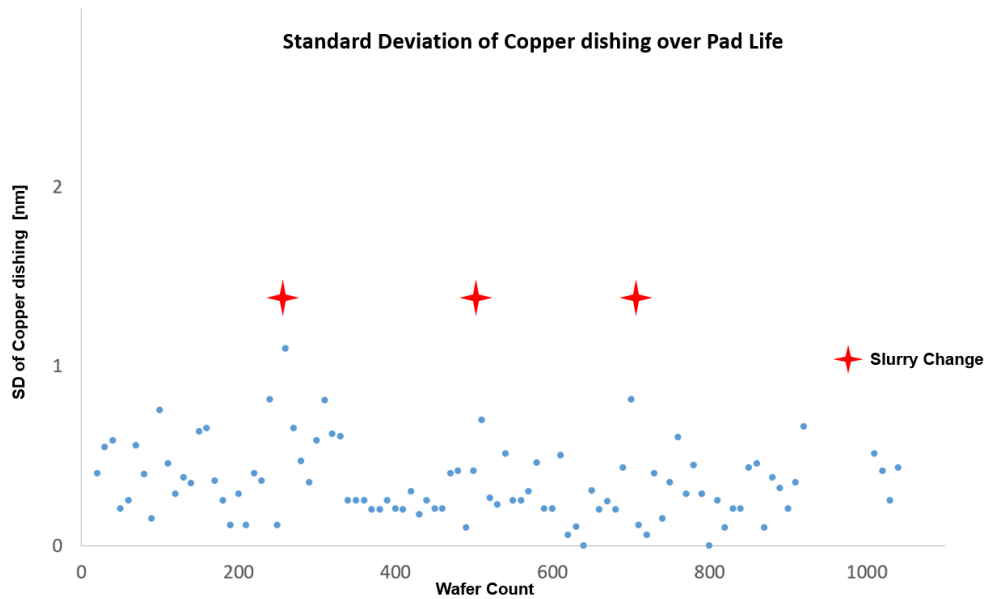


Figure 6: Standard Deviation of Copper dishing measured on >100 structured wafers over pad life

DISCUSSION

The consumable set used was able to provide the required copper dishing and erosion such that, even the measured outliers were within the required defined dishing specifications and therefore usable for direct bonding. The pad break in procedure and slurry age are very important with respect to stability. The main influence was caused by the process setup of the pad conditioner – abrasiveness, downforce influenced dishing stability while sweep cycles influenced erosion.

The polished structured wafers were used among other things for further research on surface preparation tests, W2W ~ and D2W bonding and anneal experiments. Results of this research were previously presented in [6]. Figures 7 and 8 show examples of direct bonded die on coupon and wafer bond alignment results as well as SEM analysis of bonded interconnects.

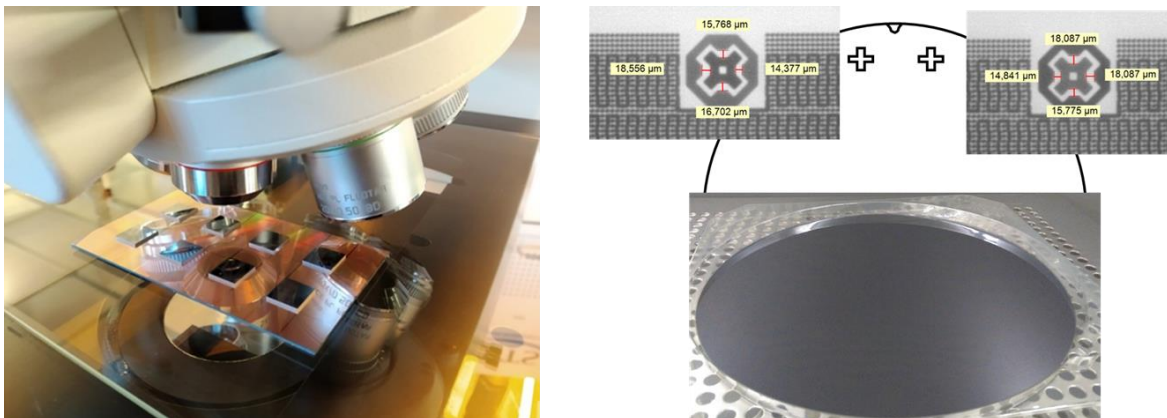


Figure 7: Examples of direct bonded dies on coupon and the alignment on direct bonded W2W [6]

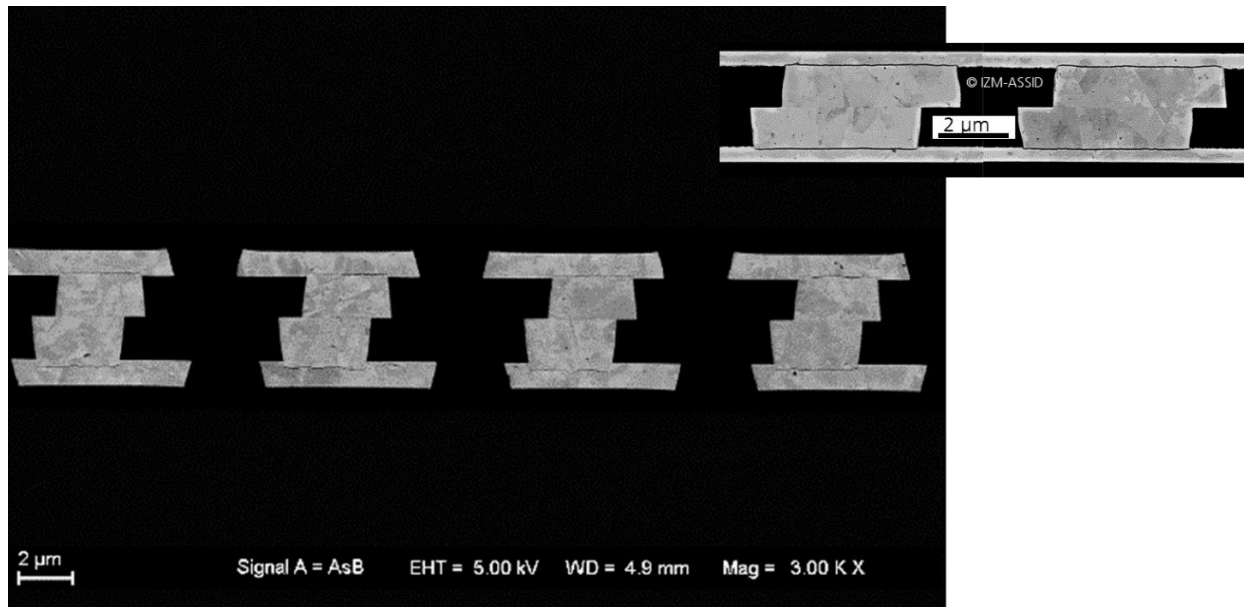


Figure 8: SEM analysis of bonded interconnects (RDL and DBI layer) [6]

CONCLUSIONS

The polish tests demonstrated the stability of the selected process settings for wafers manufactured for hybrid bonding with very stringent process specifications for dishing and erosion for relatively large bond interfaces. Process stability was demonstrated for a pad lifetime of more than 1000 wafers. Since no degradation was observed it is likely that the pad lifetime can be increased further. Consumable changes (slurry) caused a minor drop in dishing values. In a manufacturing environment using a central slurry supply system this effect may not be noticeable. Future work focus on replicating this stability data for different designs and feature sizes.

ACKNOWLEDGMENT

This work was partially funded by the department for science and arts of the federal state of Saxony and by Fraunhofer Society (SAB project "Transfer center: functional integration for the micro-/nanoelectronics", number 100368159). The authors would like to thank all the involved staff of Fraunhofer IZM ASSID for the wafer processing and the staff of Adeia for their continuous support and exchange of ideas and recipes.

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