CMP Challenges for Buried Power Rail Integration

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Introduction

Buried Power Rail (BPR) is acknowledged as an important scaling booster for finFET device technology. The implementation of BPR in the standard cell is innovative because of the smart power delivery approach. Embedding the power lines deep into the shallow-trench isolation and substrate enables track height scaling, limits the IR drop due to a higher aspect ratio and boosts the device performance at system level when combined with a backside power delivery network (BSPDN) [1-3].

BPR can be integrated at different stages in a logic integration scheme. In this work, BPR is inserted in the silicon fin module and requires two additional CMP steps on top of the standard STI CMP process. All three CMP steps involved in the BPR process flow are illustrated on figure 1: (a) STI CMP (b) WBPR CMP and (c) Oxide Plug CMP

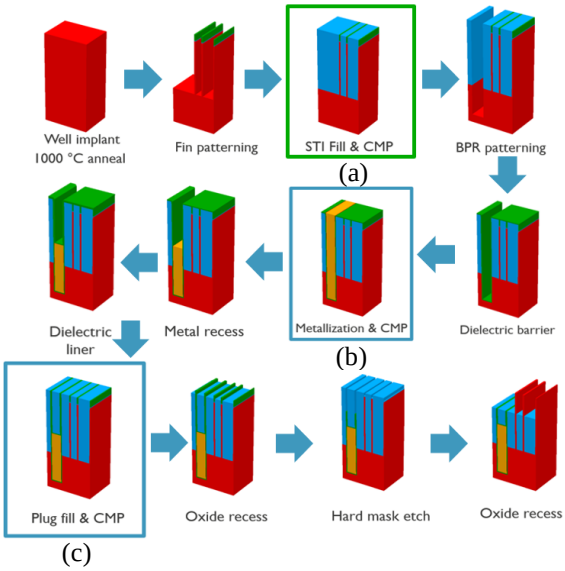

Fig.1 BPR integration in the Si fin module

This work presents the CMP challenges and the implemented process control measures leading to a successful BPR adoption in a Si finFET integration scheme (see figure 2).

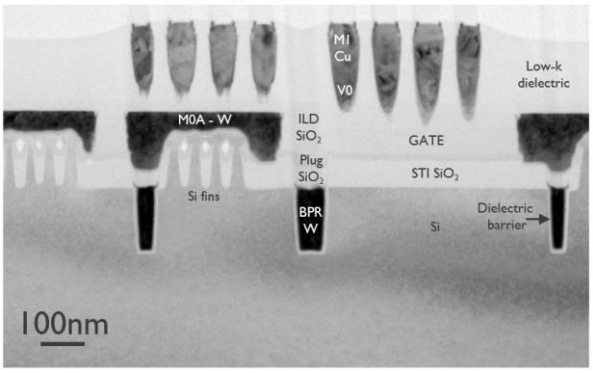

Fig. 2 TEM showing integrated W-BPR lines in a 45nm fin pitch FEOL test vehicle [1]

CMP challenges

The general requirement for the implemented CMP processes is to achieve a selective and controlled stop on thin layers of dielectric. From CMP process perspective, the use of highly selective slurries combined with dynamic full wafer profile control and advanced endpoint features during polishing are key to meet this requirement. The EBARA CMP tool model F-REX300X was used as state-of-the-art polisher to address the CMP challenges and to ensure a successful BPR integration on 300mm wafer level.

(a) STI CMP

The STI CMP process uses a ceria-based slurry for polishing SiO_2 with a high selectivity towards the SiN hardmask covering the fins. A real time in-situ profile control technique SOPM-CLC* significantly improves the resulting within wafer non-uniformity. This is illustrated on figure 3 where the STI field thickness values post CMP are compared with and without the use of SOPM-CLC. The use of profile control results in a thickness range improvement from 30nm to about 10nm.

Another benefit of using SOPM-CLC is an amplified friction-based endpoint signal as the full wafer reveal time on the SiN stopping layer is significantly reduced. This also leads to minimizing dishing and stack erosion on respectively the STI field areas and the SiN hardmask.

**Spectrum Optical Monitor combined with closed-loop control enables pressure adjustments of the different polish zones during the dielectric polish process*

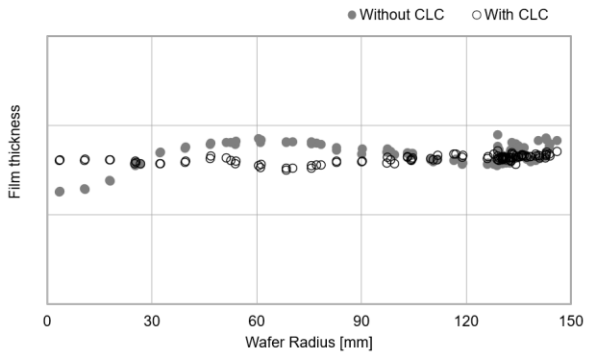

Fig.3 STI field film thickness comparison vs wafer radius with and without use of SOPM-CLC

A comparison of the SiN hardmask thickness between the fin etch and the STI CMP stage reveals a loss of 2-3nm SiN as measured on the actual fins (see figure 4). The step towards the field area and in between the fins as observed post STI CMP is caused by oxide shrinkage during TEM imaging.

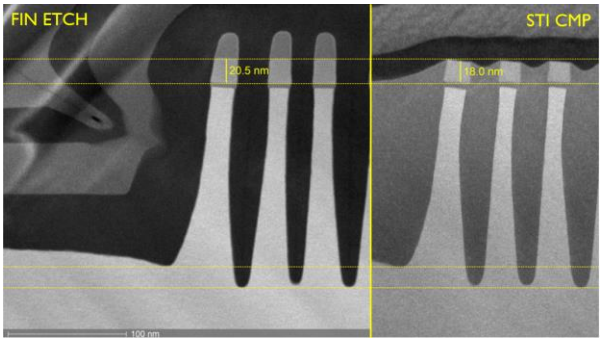

Fig.4 TEM comparison of the SiN hardmask thickness after fin etch and STI CMP stage

The main CMP challenges of the STI CMP process are ensuring a controlled stop on the SiN with minimal hardmask loss while ensuring SiO_2 clear on top of the fins as this will otherwise compromise the fin reveal process in a later stage.

(b) <u>WBPR CMP</u>

After the BPR patterning in the STI module, a thin dielectric barrier is deposited prior to metal fill. A SiO_2 barrier is preferred over SiN because of its higher selectivity towards the metal recess process later in the process flow. The BPR metallization involves TiN barrier deposition followed by W fill.

The WCMP process is performed with an alumina-based slurry that has an extremely high selectivity towards the underlying dielectric barrier. Process control during CMP makes use of RECM-CLC** and ensures both profile control during polishing and a controlled stop on the thin dielectric barrier.

***Resistance Eddy Current Monitor combined with closed-loop control enables pressure adjustments of the different polish zones during the metal polish process*

Due to the thin dielectric stopping layer, the application of an additional non-selective CMP buffing step with stack loss cannot be tolerated. The main challenge here is to obtain metallized BPR lines free from metal and polish residues (see figure 5). Even though some metal residues will be removed in the subsequent metal recess process it is important to control the overall frontside and backside contamination on the full 300mm wafer as this is a risk in a front-end-of-line (FEOL) process flow.

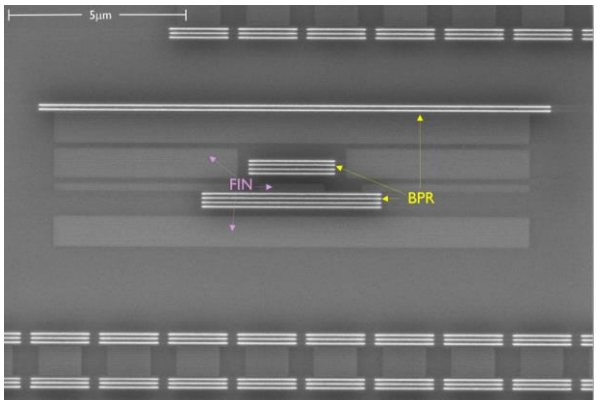

Fig.5 Top-down SEM image post WBPR CMP

Assuming that the initially deposited SiO_2 barrier is equally thick on the sidewalls and on top of the features, the dielectric loss due to WBPR CMP and metal recess is limited to 2nm as illustrated on figure 6.

(c) <u>Oxide Plug CMP</u>

As the plug fill process is performed with flowable CVD SiO_2 to ensure proper gap-fill, a post densification anneal in steam and N_2 ambient is required. The steam anneal can lead to W oxidation and therefore the implementation of a dielectric SiN liner is required prior to gap-fill. The thickness of this liner should be optimal to prevent W oxidation of the BPR plug and to minimize gate plug/spacer loss during the etch of the via landing

on the BPR lines (VBPR) later in the flow. The main challenge for the oxide plug CMP is achieving a controlled stop on a 3nm SiN liner.

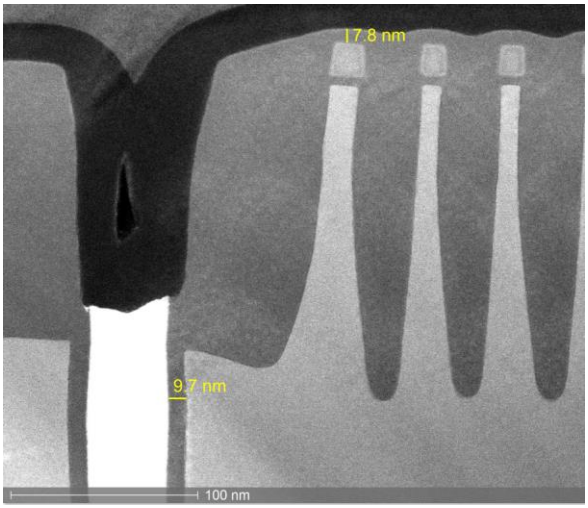

Fig.6 TEM image of the recessed BPR plug and the neighboring fins covered by the dielectric SiO_2 barrier

The oxide plug CMP process is performed with the same ceria-based slurry process as applied for the STI CMP step. This step is crucial in the BPR process flow as any residual SiO_2 on top of the SiN liner will have a direct impact on the downstream hardmask removal and fin recess processes. This is visualized on figure 7 where an oxide plug CMP process without profile control and a short overpolish time can lead to circular areas with oxide residuals that will locally prevent the subsequent SiN hardmask removal.

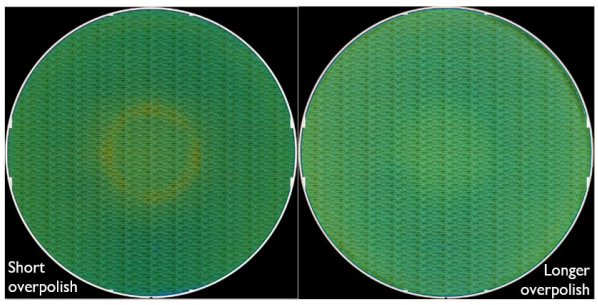

Fig.7 Full wafer optical inspection images post oxide plug CMP (obtained from KLA CIRCL tool) illustrating the overpolish time importance of a CMP process without SOPM-CLC control

The implementation of an advanced CMP control feature like SOPM-CLC is important to prevent this situation and to obtain a controlled landing on the thin SiN liner for the full wafer (see figure 8).

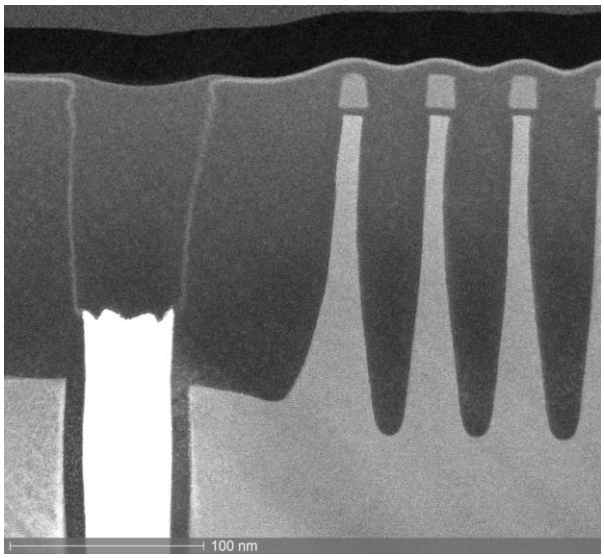

Fig.8 TEM image post oxide plug CMP process illustrating stop capability on 3nm SiN liner

Conclusions

The implementation of BPR in the silicon fin module requires the need of 2 additional CMP steps compared to the standard module. The use of advanced slurries and the implementation of advanced CMP tool features on all the CMP steps are essential to gain process control on these thin dielectric layers and are key for a successful adoption of BPR.

Acknowledgements

This work would not have been possible without the continuous support of Ebara and more specifically the on-site engineers Toshikazu Nomura and Masato Sugawara. We would like to sincerely thank them as well as the integration and material characterization colleagues at imec.

References

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