Trends with Sustainability and Emerging Developments in Wet and Dry Processes

NCC AVS User Group Meeting

December 1, 2022

Mike Corbett

mcorbett@linx-consulting.com

LINX Consulting

see beyond the horizon

Agenda

- Intro to Linx Consulting
- Review of SPCC and ESG Conferences

- Overlap of Wet and Dry Processes

- Perspectives on the Development and Implementation of Sustainable Processes in the Semiconductor Industry

Linx Consulting

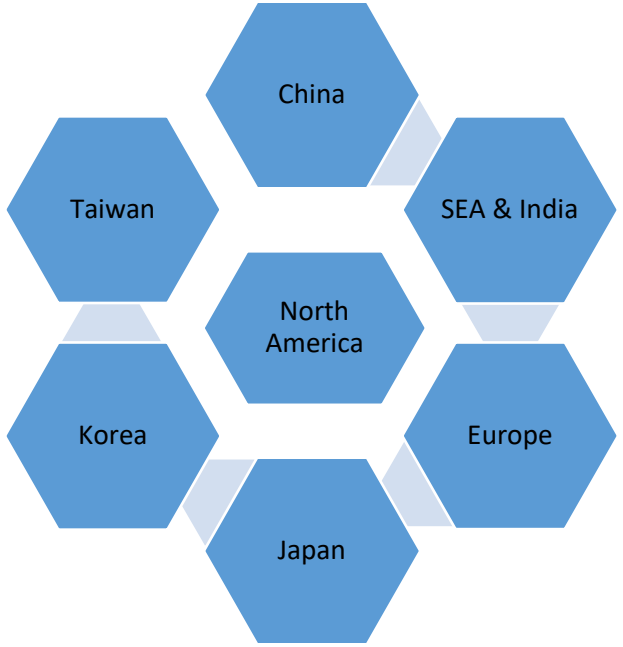
Linx Consulting

1. *We help our clients to succeed by creating knowledge and developing unique insights at the intersection of electronic thin film processes and the chemicals industry on a global basis*

2. *The knowledge is based on a core understanding of the semiconductor device technology; manufacturing processes and roadmaps; and the global structural industry dynamics*

3. *This knowledge is leveraged to create advanced models, simulations and real-world forecasts*

4. *Our perspectives are by direct research and leveraging our extensive experience throughout the global industry value chain*



Linx Consulting Service Portfolio

- **Multi-Client Reports**
  - IC Materials
    - CMP / Abrasives
    - Deposition / ALE
    - Patterning Materials
    - Cleaning
    - Electronic Gases
    - Bulk Chemicals
- **Forecast services**

- **Proprietary Projects**
  - Market & Strategic Planning
  - M & A Services
  - Growth and Diversification
  - Supply Chain Optimization
  - Technology Commercialization
  - Strategic Planning
  - Scenario Planning
  - Voice of the Customer

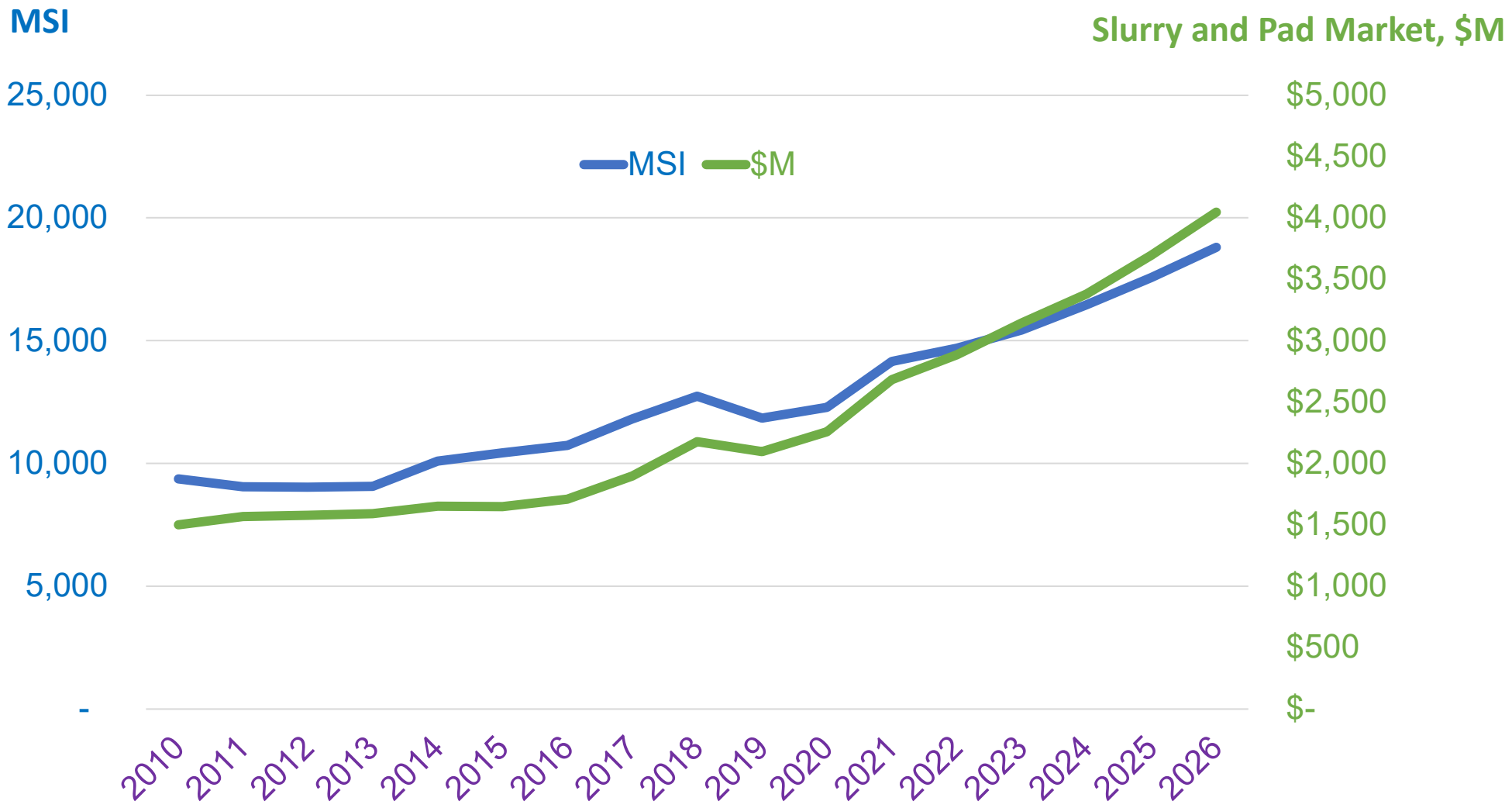
- **Econometric Semiconductor Forecast**
  - Financial planning
  - Sales and Operational planning
  - Forecasting

- **Cost Modeling**
  - Client demand modeling
  - Product development
  - Bill of Materials quantification

- **Semi Technology Conferences**
  - The Business of Cleans & SPCC
  - Electronic Specialty Gas Conference

- **Wafer Demand Forecasting**
- **Regional Forecasting**

CMP Consumables Will Grow Above MSI



24th Edition

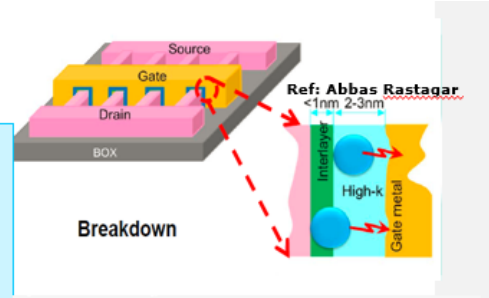
Surface Preparation and Cleaning Conference

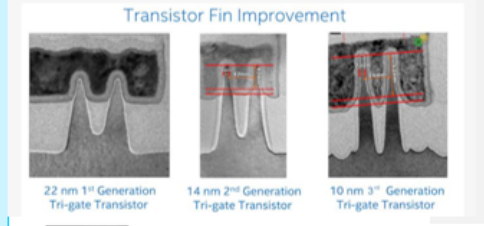
17-18 October, 2022
Chandler, AZ

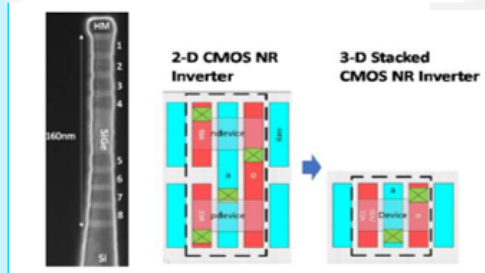
Intel Keynote on Defectivity Trends

Critical Defect Trend

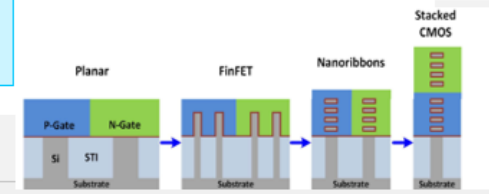
- **Special cleaning formulations, increase # of damage-free cleaning (High aspect ratio structures), precision of patterning and cleaning, unprecedented etch selectivity with atomic level of etch control, more CMP steps, Particle control in ALD, high K deposition/Cleaning challenge**
- **Role of <<5nm conductive particle** for complex topography of advanced 3D gate stack integrity and device reliability
- **Poor signal to noise ratio** (SNR) of localized information
- **HVM EUV towards High NA Readiness: Print even smaller features on Si → 2025**
- **Key Measurement and Metrology challenge: Detection and Measurement of <<10nm SEVD process adders and interfacial defects/films (multiple stacks)**







Source: Intel, IEDM 2020



W PCMP

THE SURFACE PREPARATION AND CLEANING CONFERENCE (SPCC)

SPCC 2022 | October 17-18, 2022

Ti ion contamination and removal mechanism during the W CMP process

Palwasha Jalalzai[1], Ranjith Punathil Meethal[1], Sumit Kumar[1], Tae-Gon Kim[2], Wonseob Cho[3], Andreas Klipp[4], Jin-Goo Park[1*]

[1] Department of Materials Science and Chemical Engineering, Hanyang University, Ansan, Republic of Korea

[2] Department of Smart Convergence Engineering, Hanyang University ERICA, Ansan 15588, Korea,

[3] Electronic Material R&D Center Asia, BASF, Suwon, 16419, Republic of Korea

[4] BASF SE, Ludwigshafen, 67056, Germany

*jgpark@hanyang.ac.kr

The Engine of Korea

PVA Brush Defects

THE SURFACE PREPARATION AND CLEANING CONFERENCE (SPCC)

SPCC 2022 | Wild Horse Pass, Chandler, AZ, USA | October 17-18, 2022

Characterization of impurities from incoming PVA brush for sub 10 nm post CMP cleaning process

October 17, 2022

Kwang-Min Han[1], Suprakash Samanta[2], Jerome Peter[2], and Jin-Goo Park[2,*]

[1]Department of Bio-Nano Technology and [2]Department of Materials Science and Chemical Engineering, Hanyang University, Ansan, 15588, Republic of Korea

*jgpark@hanyang.ac.kr

The Engine of Korea

IMEC Backside Thinning

Extreme Silicon Thinning For Back Side Power Delivery Network Application: Need For a Highly Selective Alkaline Silicon Etch Stopping On SiGe Etch Stop Layer

Farid Sebaai [1], Roger Loo[1], Anne Jourdain[1], Kurt Wostyn[1], Eric Beyne[1]

[1] IMEC vzw, Kapeldreef 75, B-3001 Heverlee, Belgium


Welcome
4th Electronics Specialty Gas Conference
Business Interface Conference
October 19 - 21

Sponsors

TEL™

Entegris

EMD Electronics

KLA

DUPONT

MESSER Gases for Life

Process Insights
Premium Insights Into Process

Tigeroptics

REC Silicon

Sponsors

AMT

BannerIndustries
High Purity & Industrial Flow Component Distribution

HORIBA
Semiconductor

SCREEN

HUNTSMAN
Enriching lives through innovation

KANOMAX
The Ultimate Measurements

ESI Elemental Scientific

FUJIFILM

TECHNIC INC

www.linx-consulting.com

Sponsors

JSR

BASF
We create chemistry

Global ZEUS

ichor

ARKEMA
The world is our inspiration

CS CLEAN SOLUTIONS

EDWARDS

Air Liquide

ELECTRONIC FLUOROCARBON

mott
MISSION CRITICAL PRECISION

EBARA

Athinia

WONIK Corporation

Business Interface Conference & Market Overlap of Wet and Dry Processes

Time	Title	Speaker
8:40 AM	Keynote Speaker: Semiconductor Technology Roadmap – Dry and Wet Tension Points	Scotten Jones IC Knowledge
9:20 AM	Is the Economy in Recession? And Does It Matter for Semiconductors?	Duncan Meldrum Hilltop Economics
9:50 AM	NIST Activities in the Semiconductor Agency	James Maslar NIST
10:10 AM	Semiconductor Industry Growth and Opportunities in Greater Phoenix	Chris Camacho Greater Phoenix Economic Council
10:30 AM	Break	
11:00 AM	Review of Gases and Chemicals by Process Module	David Maloney Linx Consulting
11:30 AM	Wet vs. Dry Processing Challenges for Advanced Transistors	Trace Hurd Tokyo Electron
12:00 PM	Strategies for Targeted Contaminants Removal in Gas and Liquid Filtration	Jad Jaber Entergris
12:30 PM	Lunch	

Sustainability Within The Semiconductor Industry

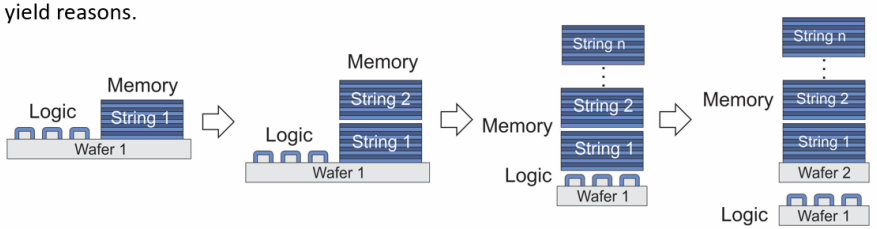
Time	Title	Speaker
1:30 PM	Introduction to the Sustainability Session	Mike Corbett Linx Consulting
1:45 PM	Keynote Speaker: Net-Zero Semiconductor Manufacturing in the Future	Suresh Ramarajan Micron
2:30 PM	Panel Discussion: Sustainability	Moderator: James Amano – SEMI Panelist: Taimur Burki – Intel Tracey Christiansen - Entegris Benjamin Gross – Applied Materials
3:45 PM	Break	
4:15 PM	ESG Sustainability via Materials Innovation and Process Improvement	James Nehlsen EMD Electronics
4:45 PM	Toward Sustainable Fab: Reducing Bulk Chemicals by SPM Reuse in Single-Wafer Process Applications	Jim Snow Screen
5:15 PM	Closing Remarks - End of Wednesday Sessions	Mike Corbett

ICKnowledge Roadmaps

3D NAND Evolution

IC KNOWLEDGE LLC

- 3D NAND layers likely to continue to increase to around 1,000 layers.
- String stacking controls aspect ratio by splitting up the layers into strings.
- Logic under the array improves scaling but presents process challenges.
- Long term the logic and memory will likely be on separate wafers for process simplicity and yield reasons.

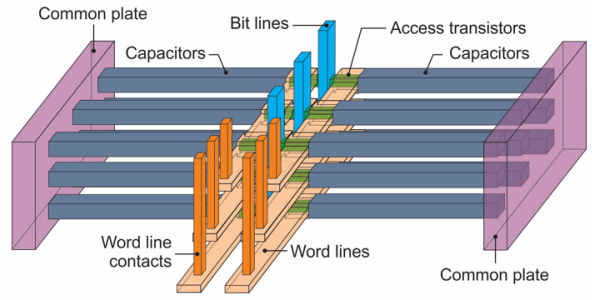


Logic to the side - single string | **String stacking** | **Logic under memory - more strings** | **Logic and memory on separate wafers - more strings**

3D Stacked DRAM

IC KNOWLEDGE LLC

- Stacked horizontal capacitors.
- Memory array and peripheral logic likely to be on separate bonded wafers.
- Vertical pitch ~80nm with ~100 layers needed for density = ~8,000nm stack of epitaxially deposited single crystal Si/SiGe (SiGe is a sacrificial film).
- Vertical bit line.
- Stair step word line that surrounds the access transistor (GAA).
- No EUV

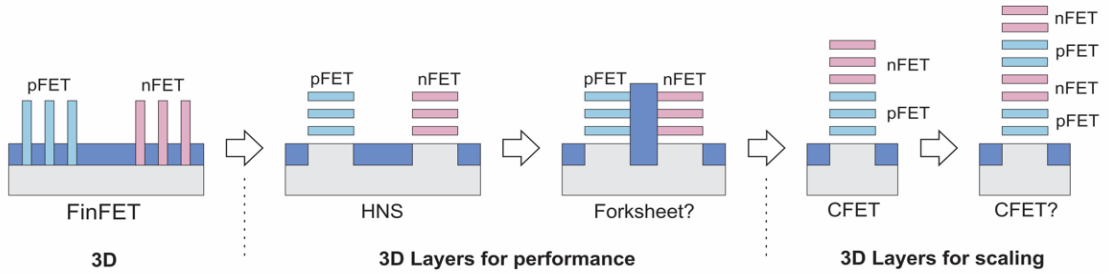


3D DRAM Memory Array

Logic Evolution

IC KNOWLEDGE LLC

- FinFETs are 3D but not layer based.
- Horizontal Nano-Sheets (HNS) use layers for performance. HNS may evolve to Forksheets for density but only Imec appears to be pursuing it.
- Complimentary FETs (CFETs) use layers for scaling. Two device stacks are clearly on the roadmaps at major logic providers, three, four or more device stacks are being evaluated.



3D | **3D Layers for performance** | **3D Layers for scaling**

TEL – Wet & Dry Approaches

Future Challenges

- Growing the Tool Kit
  - Selectivity requirements among Si based films will continue to increase
  - New gases and gas mixtures will be needed
  - Optimizing speed, cost, and selectivity could open new applications in 3D Memory
- Metal and Metal Containing Film Etches
  - Cu, Co, Ru partial etches for FSAV integration
  - Mo, W etches for 3D memory enablement
- 2D Material Compatibility
- Thermal Atomic Layer Etching
  - Research ongoing at numerous universities, e.g. Colorado, NC State…

Conclusions

- Device Technology Roadmap 3D Trends Driving Significant Challenges
  - High Aspect Ratio Structures
  - Confined Space Processing / Hidden Surfaces
  - Increase in Risk of Pattern Collapse
  - Multi-Film Selectivity Requirements Increasing
- Isotropic Gas Phase Etch Processes Address Many of These Challenges
  - Elimination of capillary forces, atomic scale precision, high reactant mobility, little to no pattern loading, morphological control
- Applications for Isotropic Gas Phase Processing Expected to Grow in both Logic and Memory

Challenges - Dry vs Wet Etching

Dry

- **Horizontal-direction etch**
  - The anisotropic nature of gas phase etching reaction make lateral etch difficult to control
- **Damage**
  - Ionized molecules generated by RF power during plasma reaction can damage the underlying substrates
- **Selectivity**
  - Compared to liquid phase processes, gas phase processes can't effectively accommodate sophisticated chemistries to address selectivity requirements
- **EHS**
  - Many dry etch chemistries rely on greenhouse gases (CF_4, SF_6…)

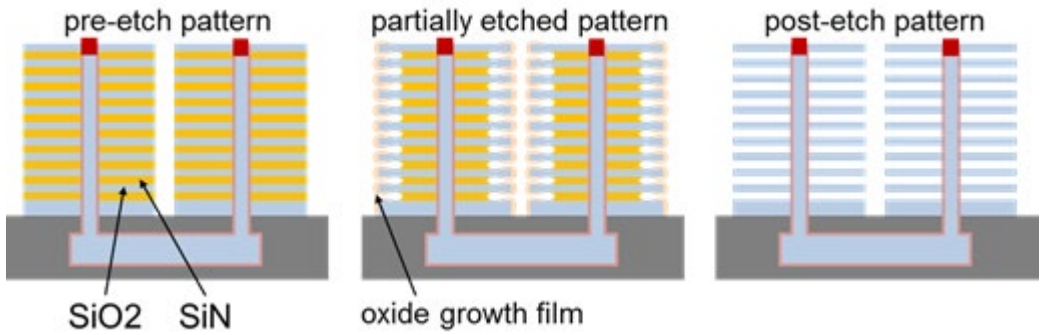
Wet

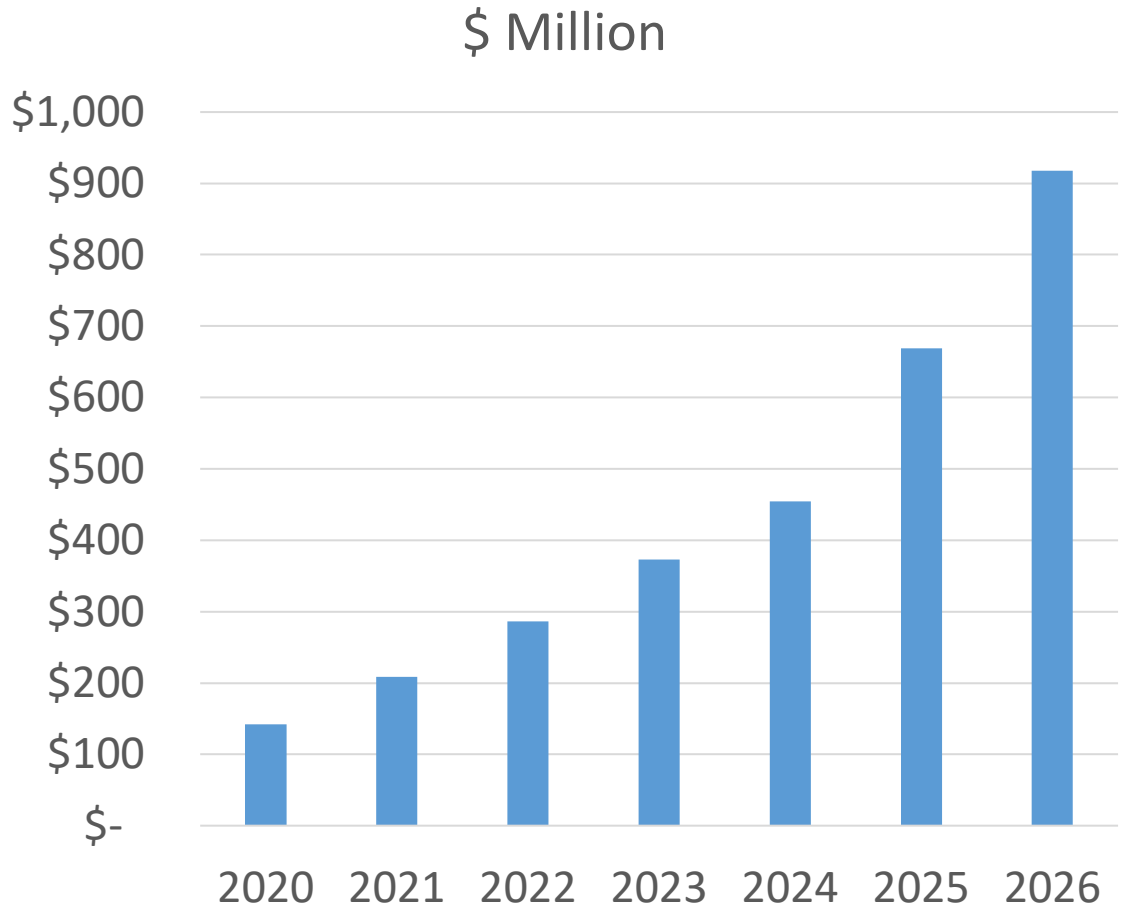
- **Etch profile management**
  - Wet etch is an isotropic process. Difficult to maintain straight vertical post-etch shape through precise control
- **Post drying**
  - The post clean step after wet etch requires IPA drying, which can cause patterned structures to collapse
- **High Aspect Ratio**
  - Wet etchant is unable to penetrate small dimensions at the bottoms of high aspect-ratio structures
- **Throughput**
  - Some wet etch applications like H_3PO_4-based nitride etch take several hours and become bottleneck in the fab
- **EHS**
  - Disposal cost of waste wet process streams continue to go up

High-Selectivity Nitride Etch

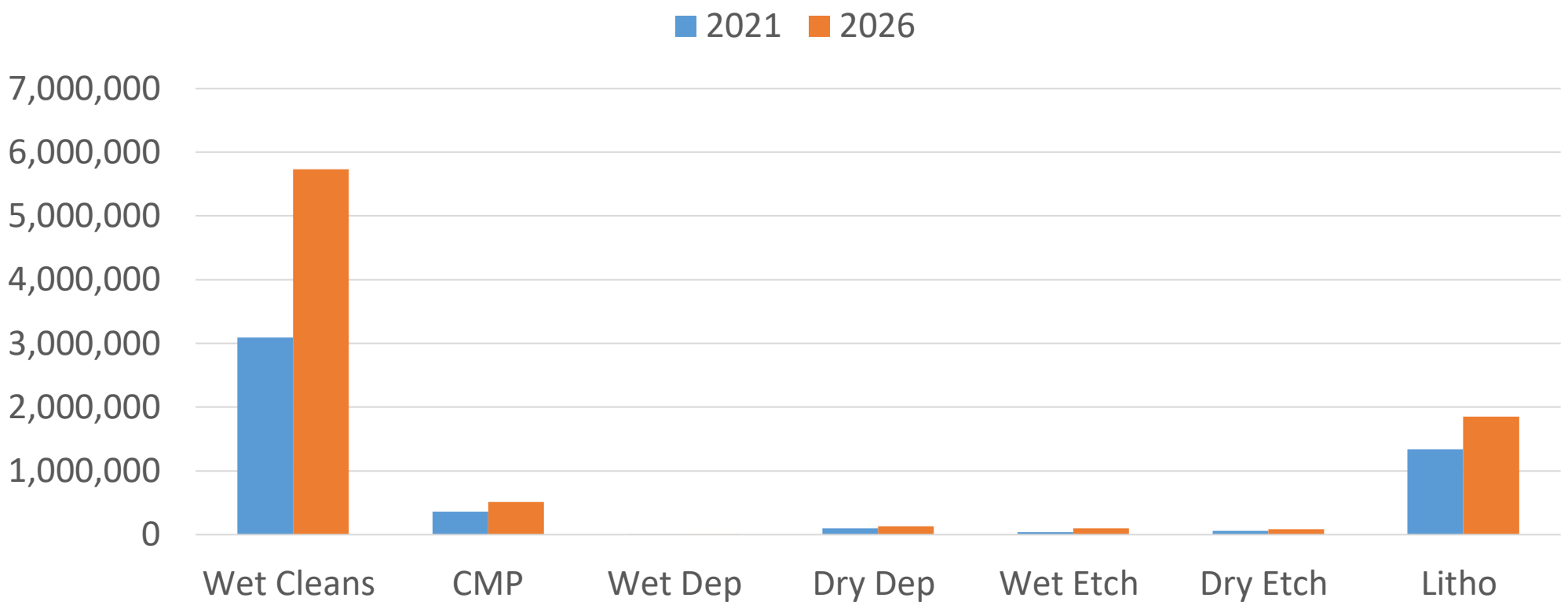
Nitride Strip and Cell Formation

- A slot mask is applied and etched down through the stack. A wet etch is used to etch out the nitride layers that are then replaced with aluminum oxide and titanium nitride memory cell films and then the horizontal layers are filled with tungsten. The tungsten is etched back in the slot, oxide is deposited, and the trench is filled with tungsten.
- Nitride strip in charge trap still remains a challenge. New chemistries are required. This is getting more difficult as the number of layers and HAR increases.



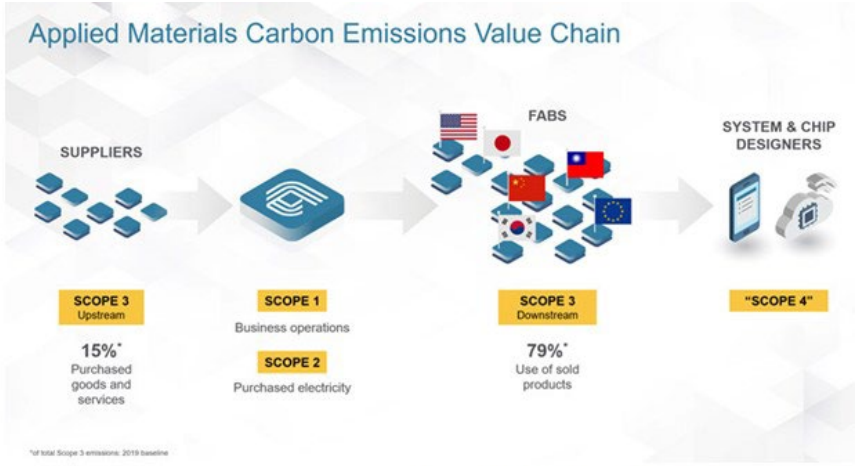


Chemical Volume by Process (MT), 2021 & 2026



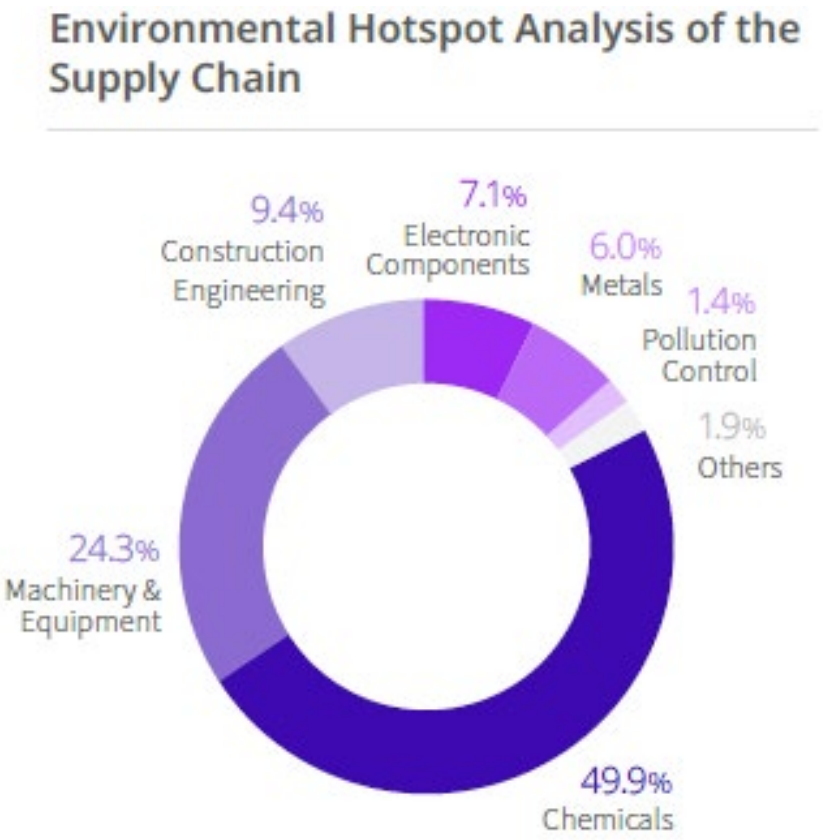
Sustainability – Major Focus on the Uses of Chemicals in Fabs

OEM PERSPECTIVE



	Scope 1	Scope 2	Scope 3 ~99%	"Scope 4"
Primary drivers of emissions	Direct emissions Business operations	Indirect emissions Purchased electricity	Indirect emissions Customer end use of products (~80%) Supplier inputs (~15%)	Avoided emissions Semiconductor Design to Manufacturing collaboration
Applied's ESG Frameworks	1x		100x	10,000x
			Industry collaboration	Industry collaboration ++

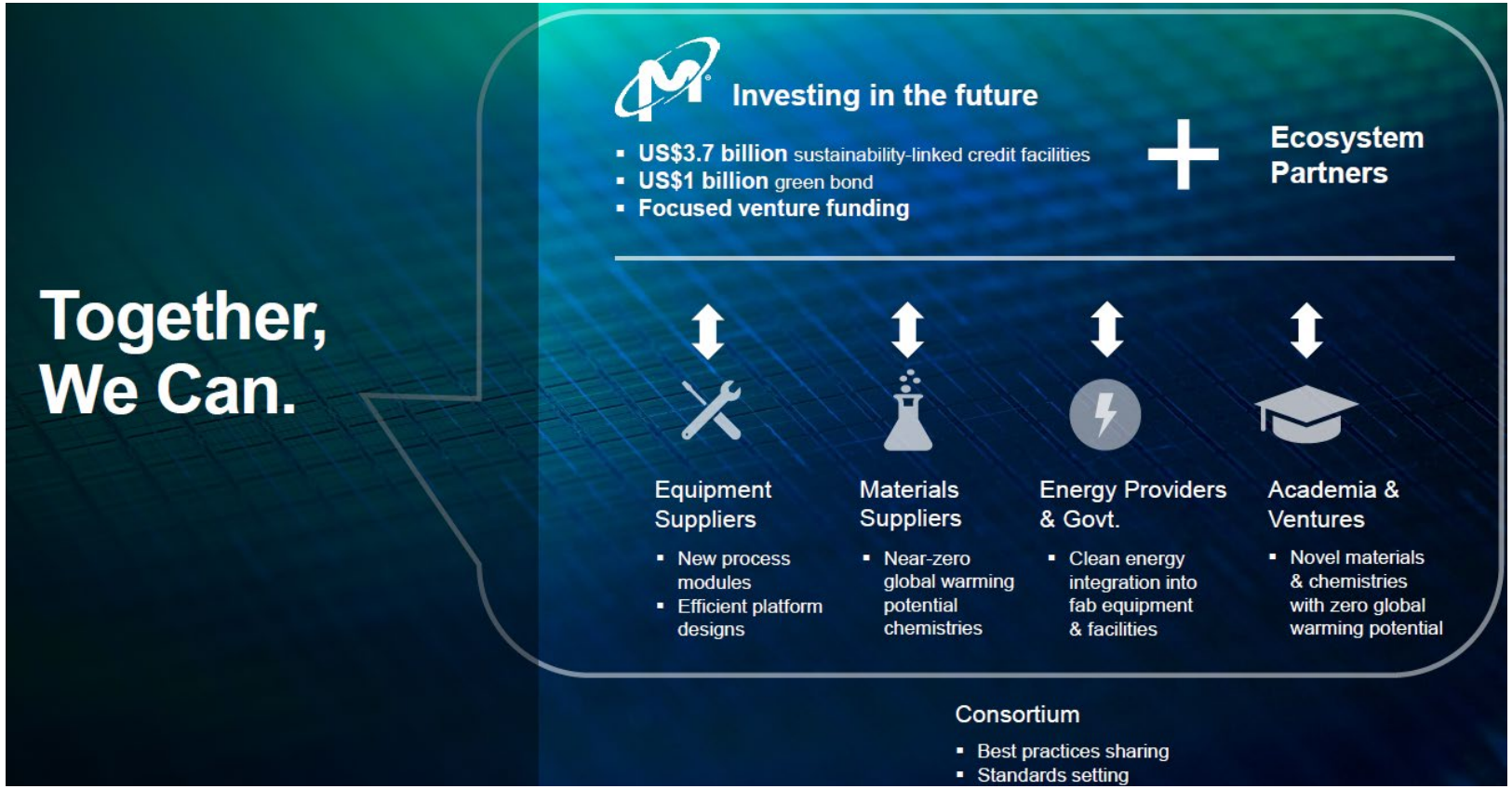
SEMI PRODUCER PERSPECTIVE



Sources: Applied Materials and TSMC

Micron Perspectives

- Process GHG Decarbonization Preferred Innovations
  1. Eliminate / Replace
  2. Reduce / Reuse
  3. Destroy
  4. Data Visibility / Smart Controls
- Heat Transfer Fluid Decarbonization
- Fuel Decarbonization
- Energy Decarbonization



Screen & EMD – Pathways to Sustainability

Low CoM Through SPM Reuse

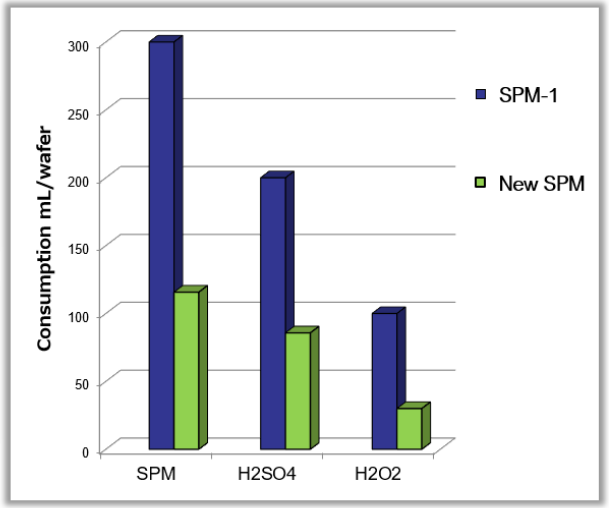
SCREEN

Chemical consumption data

Test Condition

1. SPM-1/No reclaim
SPM mixing ratio : 2:1, 30sec

2. New SPM
SPM mixing ratio : Y:1, 30sec
With Reclaim



SCREEN Semiconductor Solutions Co., Ltd.

SCREEN Semiconductor Solutions Co., Ltd.

SPE-221003152443464-L1

Keys to Sustainability
Reducing Emissions with Chemistry

Abatement

- Minimize formation of highly stable molecules during process to improve DRE and reduce secondary emissions

Process Recipe Tuning

- Optimize for low generation of high-GWP species like CF_4

New Materials

- Can be tailored to specific applications to reduce process emissions by >90% while maintaining or improving performance

Sustainable Etch & Clean

Achievable through multiple pathways while driving capabilities forward

Conclusions

- Vertical scaling bring many challenges
- Many tension points still exist between wet and dry processing
- These tension points may cause inflections on how devices are manufactured, integration approaches and materials
- Sustainability is a major industry driver
- Materials are a target for sustainability initiatives; all process modules will be impacted

More Information

Mike Corbett

+1 973 698 2331

mcorbett@linx-consulting.com

www.linx-consulting.com

Conference presentations from 2016 to 2019 are posted and available for CMPUG members to review at:

https://www.linx-consulting.com/technical-archive/.