CHIPS and Salsa
Understanding the 2022 Semiconductor Legislation

Dr. Eric Breckenfeld

December 1, 2022
$39 billion manufacturing incentive program

25% manufacturing investment tax credit
(estimated at $24.3 billion over duration of credit)

$13 billion in R&D and workforce investment
# CHIPS IMPLEMENTATION – GRANTS

<table>
<thead>
<tr>
<th>TOPIC</th>
<th>REQUIREMENTS/CRITERIA</th>
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</table>
| **Authority**                | • Commerce Department – CHIPS Program Office (CPO)  
                                 • White House – CHIPS Steering Council                                                                                                                                                                          |
| **Eligibility**              | • Fabs, ATP, SME, research facilities  
                                 • Construction, expansion, and modernization; not a relocation                                                                                                                                                   |
| **Process & Timing**         | • Application materials released by Feb. 2023 (within 6 mos.)  
                                 • Pre-application phase to allow for Commerce feedback  
                                 • Projects funded in increments as milestones are achieved                                                                                                                                                     |
| **Funding Priorities & Considerations** | • $28 billion for leading edge logic/memory; $10 billion for mature/current tech, new and specialty technologies, equipment and materials  
                                 • Supply chain and national security  
                                 • Jobs, community investment, opportunity and inclusion  
                                 • Workforce development & education partnerships  
                                 • Commercial viability post-CHIPS  
                                 • State/local incentive packages  
                                 • Taxpayer protections                                                                                                                                                                                         |
| **Clawbacks**                | • 10-year prohibition on a “significant transaction . . . Involving the material expansion of semiconductor manufacturing capacity”  
                                 • Exception for “legacy” – 28nm and older for logic, TBD others  
                                 • Stock buybacks or dividends  
                                 • Failure to meet target dates |
RESEARCH STRATEGY DESIGN

Various administrative organizations play a role

CHIPS Implementation Steering Council
Established in EO 14080; role in research strategy unclear
Co-Chaired by NEC Director Deese, OSTP Director Prabhakar, & NSA Sullivan

President's Council of Advisors on Science and Technology

National Science and Technology Council
Subcommittee on Microelectronics Leadership (SML)

Office of Science and Technology Policy

Industry & Academia

Industrial Advisory Committee
Provide guidance on needs of the U.S. microelectronics industry, national strategy, CHIPS R&D programs, and opportunities for public-private partnership
Industrial Advisory Committee from industry, academia, NGO

PCAST recommendation for Research, NSTC, and Workforce

Department of Commerce

CHIPS Program Office
CHIPS.gov

National Strategy on Microelectronics Research

Strategy for the CHIPS for America Fund
### CHIPS IMPLEMENTATION – RESEARCH

<table>
<thead>
<tr>
<th>National Semiconductor Technology Center</th>
<th>National Advanced Packaging Manufacturing Program</th>
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<tbody>
<tr>
<td>Dept. of Commerce</td>
<td>Dept. of Commerce</td>
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<tr>
<td>- Public-private consortium including DOE/NSF</td>
<td>- Strengthen advanced assembly, test, and packaging (“ATP”) capabilities</td>
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<tr>
<td>- Work with DOL &amp; universities for post-secondary education</td>
<td>- Coordinate with NSTC and Manufacturing USA Institutes</td>
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<table>
<thead>
<tr>
<th>Manufacturing USA Semiconductor Institutes</th>
<th>CHIPS Defense Fund</th>
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<tbody>
<tr>
<td>Dept. of Commerce</td>
<td>Dept. of Defense</td>
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<tr>
<td>- 1-3 manufacturing centers</td>
<td></td>
</tr>
<tr>
<td>- Virtualization &amp; automation of semiconductor equipment; novel assembly, test, &amp; packaging capabilities</td>
<td>- University-based prototyping, lab-to-fab transition of semiconductor technologies</td>
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<tr>
<td></td>
<td>- DoD-specific workforce training programs</td>
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</tbody>
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CHIPS & Science Act includes ~$170 billion in authorizations for research at NSF, NIST, and DOE, subject to future appropriations.
RESEARCH AUTHORIZATIONS

Division B of CHIPS & Science increases U.S. science authorizations; appropriations still needed

<table>
<thead>
<tr>
<th>Key Programs</th>
<th>5-year Authorization</th>
<th>Increase over Baseline</th>
</tr>
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<tbody>
<tr>
<td>National Science Foundation</td>
<td>$81 billion</td>
<td>$36 billion</td>
</tr>
<tr>
<td>NSF Tech Directorate</td>
<td>$20 billion</td>
<td>$20 billion</td>
</tr>
<tr>
<td>NSF Core Activities</td>
<td>$61 billion</td>
<td>$16 billion</td>
</tr>
<tr>
<td>National Institute of Standards and Technology</td>
<td>$10 billion</td>
<td>$5 billion</td>
</tr>
<tr>
<td>NIST Research</td>
<td>$6.9 billion</td>
<td>$2.8 billion</td>
</tr>
<tr>
<td>Manufacturing USA</td>
<td>$829 million</td>
<td>$744 million</td>
</tr>
<tr>
<td>Manufacturing Extension Partnership</td>
<td>$2.3 billion</td>
<td>$1.5 billion</td>
</tr>
<tr>
<td>Department of Energy</td>
<td>$67.9 billion</td>
<td>$30.5 billion</td>
</tr>
<tr>
<td>DOE Office of Science</td>
<td>$50.3 billion</td>
<td>$12.9 billion</td>
</tr>
<tr>
<td>Additional DOE Science and Innovation</td>
<td>$17.6 billion</td>
<td>$17.6 billion</td>
</tr>
<tr>
<td>Total</td>
<td>$169.9 billion</td>
<td>$82.5 billion</td>
</tr>
</tbody>
</table>

Total CHIPS and Science Act Authorizations in Historical Context

- NSF
- DOE Office of Science
- NIST
- COMPETES Acts

RESEARCH LANDSCAPE: NSTC/NAPMP & Valley of Death

- **Broadly Serving Activity Range**
  - DARPA/IARPA
  - AFOSR/ARO
  - ONR
  - DOE Office of Science
  - ARPA-E
  - SBIR/STTR
  - NASA
  - DOE EERE
  - DOD Branch Labs
  - DOE National Labs
  - University & NNCI
  - NIST Laboratories
  - IMEC*
  - Industry Labs & Fabs

- **DOD/IC Serving Core Focus**
  - NSF
  - ARPA
  - DIUx
  - DOE EERE
  - DOE ManTech
  - Title III DPA
  - In-Q-Tel

- **Not US-based, but accessible to US researchers**
  - NSF
  - ARPA
  - DIUx
  - DOE EERE
  - DOE ManTech
  - Title III DPA
  - In-Q-Tel

**Performers**:
- DOE National Labs
- University & NNCI
- NIST Laboratories
- IMEC*
- Industry Labs & Fabs

**Funders**:
- NSF
- DOE Office of Science
- ARPA-E
- SBIR/STTR
- NASA
- DOE EERE

**Regions**:
- Basic research
- Applied R&D
- Prototyping
- Piloting
- Scaling to production

**Private labs conducting publicly funded R&D**
# CHIPS IMPLEMENTATION – WORKFORCE

## Direct Workforce Funding
**CHIPS Workforce & Education Fund**
National Science Foundation

- $200 million over 5 years
- Establishes National Network for Microelectronics Education

## Indirect Workforce Funding
**NSTC/NAPMP, CHIPS Defense Fund, & Manufacturing USA**
Dept. of Commerce, Dept. of Defense, NIST

- $13 billion R&D funding supports STEM education
- Workforce & skills training explicit in legislation

### Company Workforce Initiatives
**CHIPS Manufacturing Incentives**
Dept. of Commerce

- Incentive applications require company workforce development commitments
- Partnerships w/ regional institutions encouraged

### Immigration & Workforce
**NSTC/NAPMP, Manufacturing USA**
Dept. of Commerce, NIST

- R&D funding creates opportunities for low-volume, high-value visa categories
- PCAST report recommends premium processing for semiconductor visas
CHIPS R&D IMPLEMENTATION

Goal: Promote collaborative R&D ecosystem aligned with industry technology agenda

Key investment areas for NSTC and NAPMP

- Support transition pathways for innovative technologies
- Upgrade research infrastructure for early-stage ecosystem
- Establish and expand access for mid-stage development and prototyping infrastructure
- Convene industry, academia, and government for collaborative innovation partnerships
- Promote dynamic workforce programs to increase and hone domestic workforce
Thank You

ebreckenfeld@semiconductors.org