



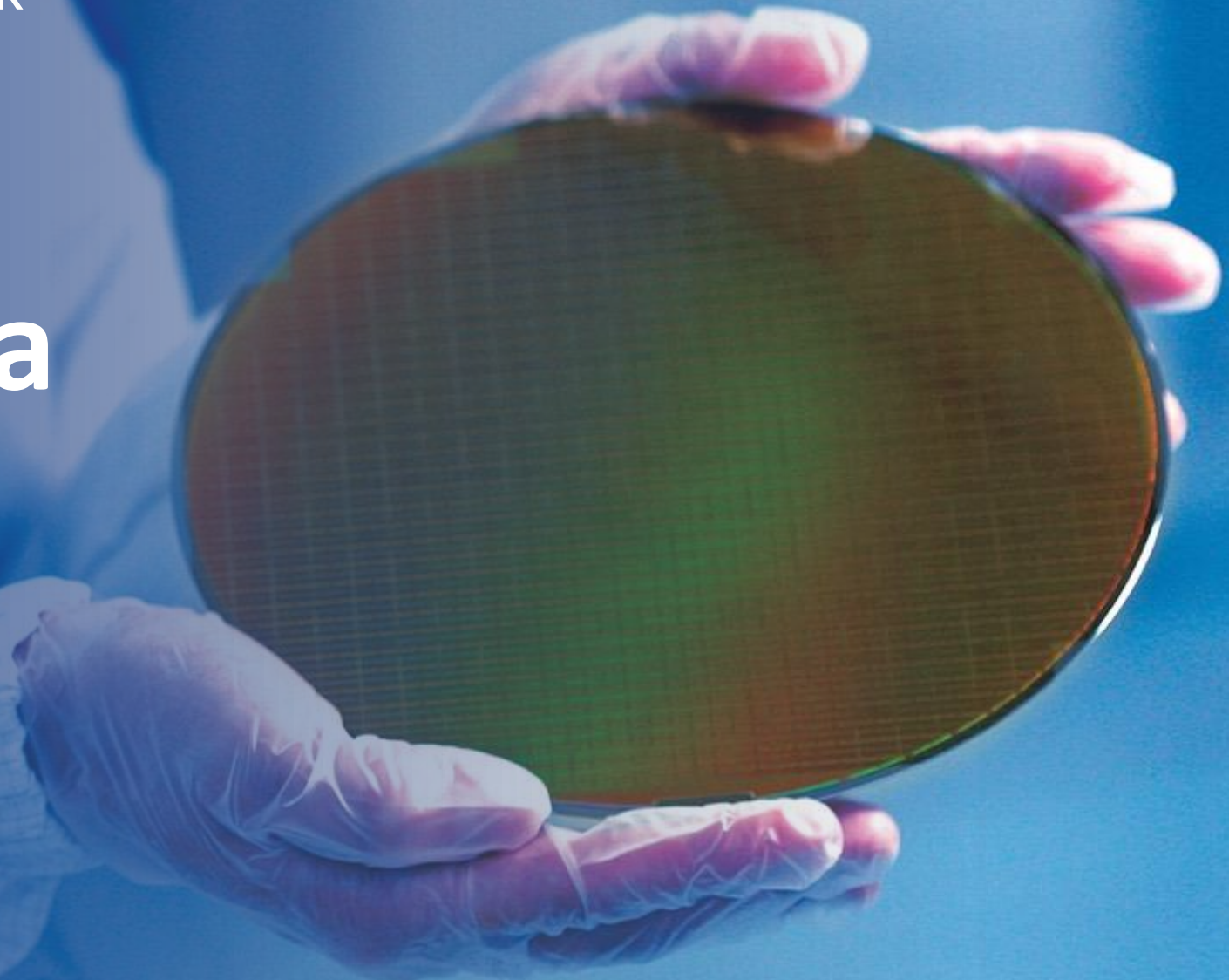
SEMICONDUCTOR
INDUSTRY
ASSOCIATION

CHIPS and Salsa

Understanding the 2022
Semiconductor Legislation

Dr. Eric Breckenfeld

December 1, 2022



SIA MEMBERSHIP

CHARTER



INTERNATIONAL



CORPORATE



CORPORATE PARTNER



2022 CHIPS & SCIENCE ACT

Signed summer 2022 in historic win for the industry

**\$39 billion
manufacturing
incentive program**

**25% manufacturing
investment tax credit**
(estimated at \$24.3 billion over
duration of credit)

**\$13 billion in R&D
and workforce
investment**

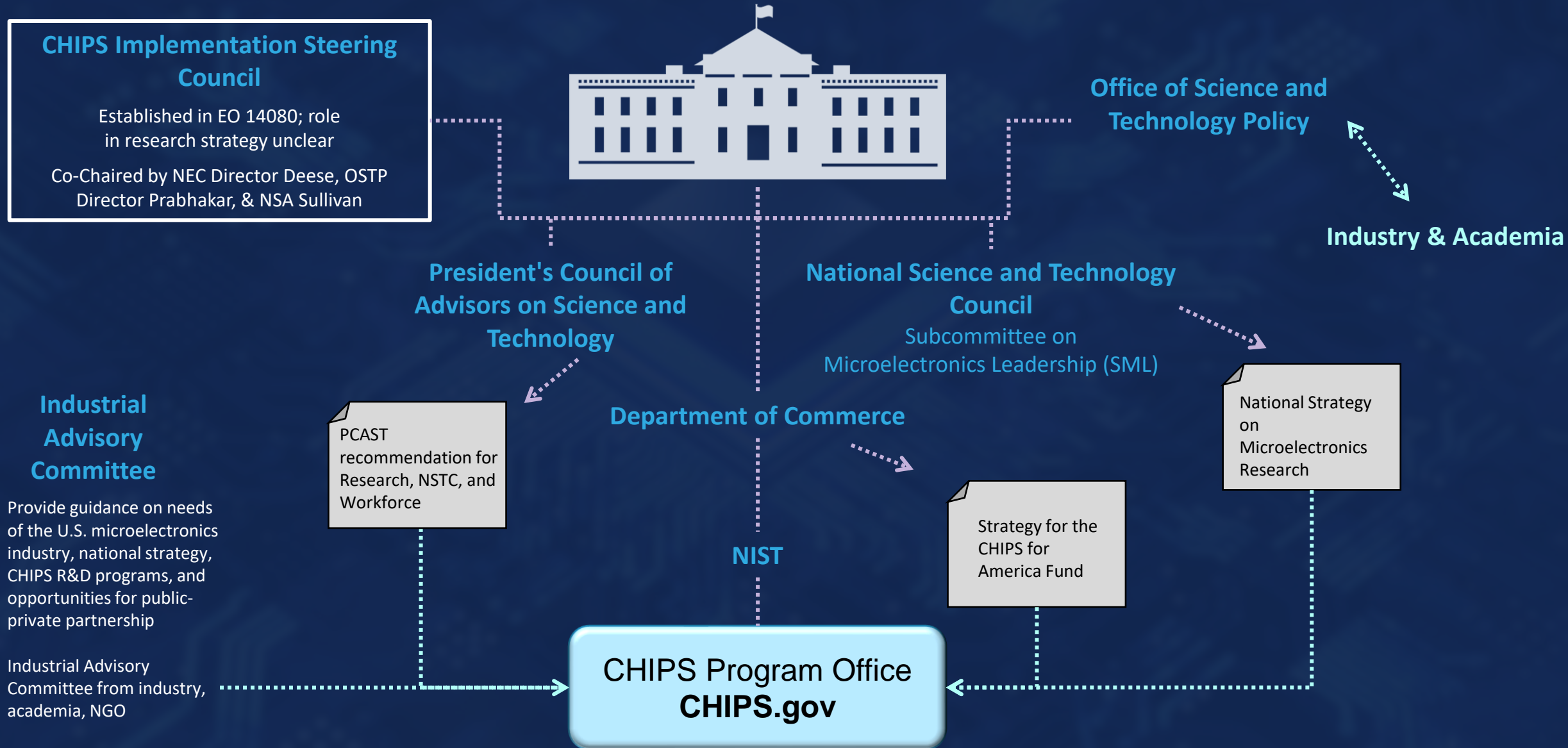


CHIPS IMPLEMENTATION – GRANTS

TOPIC		REQUIREMENTS/CRITERIA
Authority		<ul style="list-style-type: none"> Commerce Department – CHIPS Program Office (CPO) White House – CHIPS Steering Council
Eligibility		<ul style="list-style-type: none"> Fabs, ATP, SME, research facilities Construction, expansion, and modernization; not a relocation
Process & Timing		<ul style="list-style-type: none"> Application materials released by Feb. 2023 (within 6 mos.) Pre-application phase to allow for Commerce feedback Projects funded in increments as milestones are achieved
Funding Priorities & Considerations		<ul style="list-style-type: none"> \$28 billion for leading edge logic/memory; \$10 billion for mature/current tech, new and specialty technologies, equipment and materials Supply chain and national security Jobs, community investment, opportunity and inclusion Workforce development & education partnerships Commercial viability post-CHIPS State/local incentive packages Taxpayer protections
Clawbacks		<ul style="list-style-type: none"> 10-year prohibition on a “significant transaction . . . Involving the material expansion of semiconductor manufacturing capacity” <ul style="list-style-type: none"> Exception for “legacy” – 28nm and older for logic, TBD others Stock buybacks or dividends Failure to meet target dates

RESEARCH STRATEGY DESIGN

Various administrative organizations play a role



CHIPS IMPLEMENTATION – RESEARCH

National Semiconductor Technology Center

Dept. of Commerce



- Public-private consortium including DOE/NSF
- Work with DOL & universities for post-secondary education

National Advanced Packaging Manufacturing Program

Dept. of Commerce



- Strengthen advanced assembly, test, and packaging ("ATP") capabilities
- Coordinate with NSTC and Manufacturing USA Institutes

Manufacturing USA Semiconductor Institutes

NIST (Dept. of Commerce)



- 1-3 manufacturing centers
- Virtualization & automation of semiconductor equipment; novel assembly, test, & packaging capabilities

CHIPS Defense Fund

Dept. of Defense



- University-based prototyping, lab-to-fab transition of semiconductor technologies
- DoD-specific workforce training programs

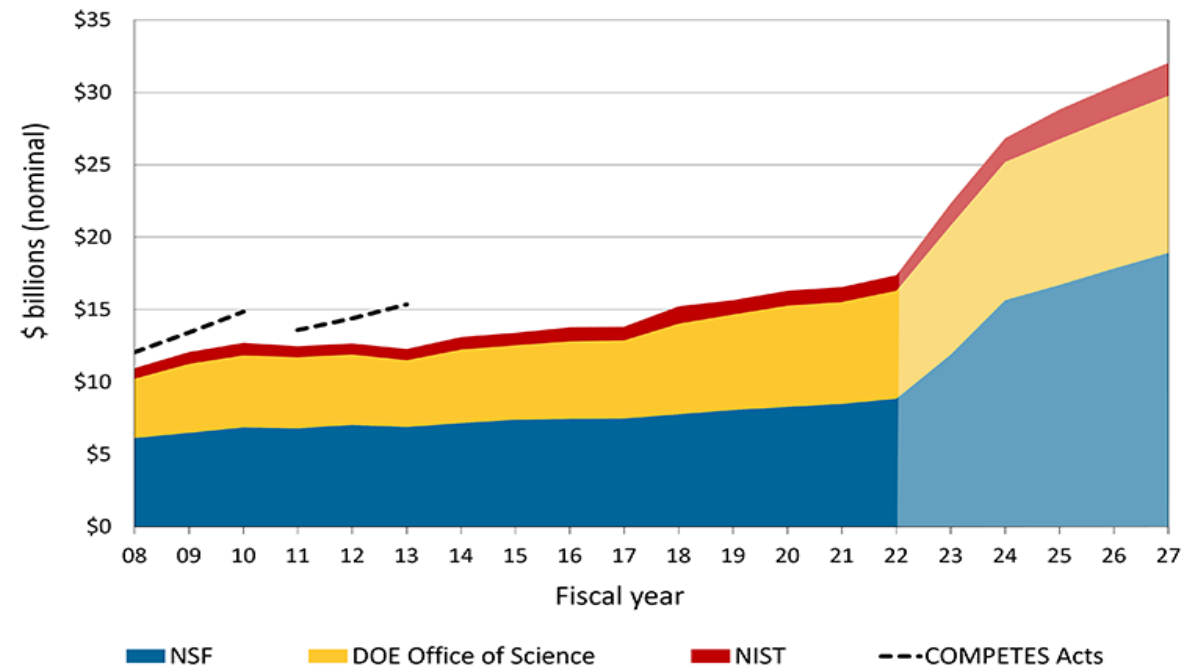
CHIPS & Science Act includes ~\$170 billion in authorizations for research at NSF, NIST, and DOE, subject to future appropriations

RESEARCH AUTHORIZATIONS

Division B of CHIPS & Science increases U.S. science authorizations; appropriations still needed

Key Programs	5-year Authorization	Increase over Baseline
National Science Foundation	\$81 billion	\$36 billion
NSF Tech Directorate	\$20 billion	\$20 billion
NSF Core Activities	\$61 billion	\$16 billion
National Institute of Standards and Technology	\$10 billion	\$5 billion
NIST Research	\$6.9 billion	\$2.8 billion
Manufacturing USA	\$829 million	\$744 million
Manufacturing Extension Partnership	\$2.3 billion	\$1.5 billion
Department of Energy	\$67.9 billion	\$30.5 billion
DOE Office of Science	\$50.3 billion	\$12.9 billion
Additional DOE Science and Innovation	\$17.6 billion	\$17.6 billion
Total	\$169.9 billion	\$82.5 billion

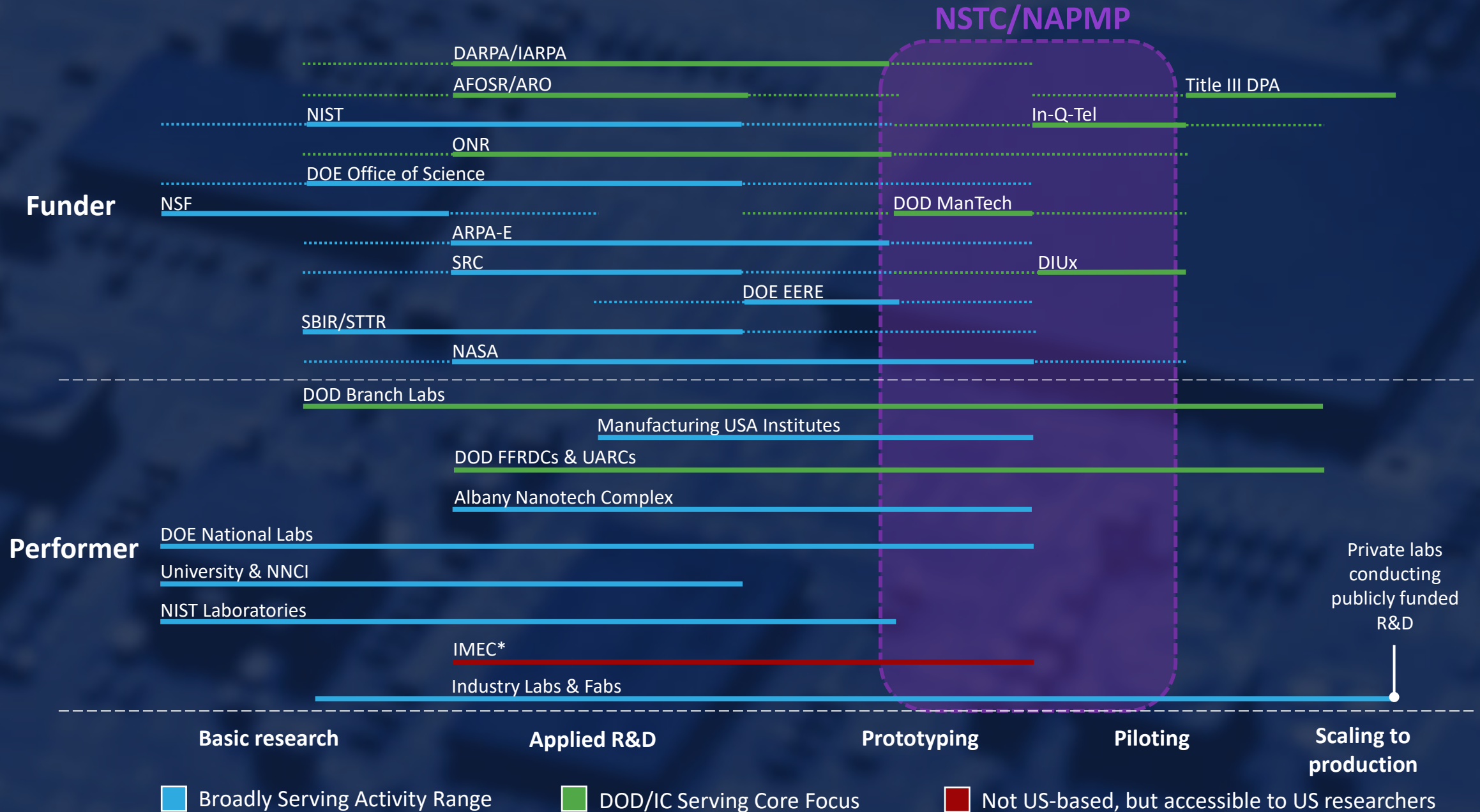
CHIPS and Science Act Authorizations in Historical Context



Includes DOE Office of Science authorizations from the Energy Policy Act of 2005 for fiscal years 2008 and 2009. Excludes supplemental appropriations provided by the American Recovery and Reinvestment Act of 2009.

American Institute of Physics | aip.org/fyi

RESEARCH LANDSCAPE: NSTC/NAPMP & Valley of Death



CHIPS IMPLEMENTATION – WORKFORCE

Direct Workforce Funding

CHIPS Workforce & Education Fund

National Science Foundation

- \$200 million over 5 years
- Establishes National Network for Microelectronics Education

Indirect Workforce Funding

NSTC/NAPMP, CHIPS Defense Fund, & Manufacturing USA

Dept. of Commerce, Dept. of Defense, NIST

- \$13 billion R&D funding supports STEM education
- Workforce & skills training explicit in legislation

CHIPS
Funding

Company Workforce Initiatives

CHIPS Manufacturing Incentives

Dept. of Commerce

- Incentive applications require company workforce development commitments
- Partnerships w/ regional institutions encouraged

Immigration & Workforce

NSTC/NAPMP, Manufacturing USA

Dept. of Commerce, NIST

- R&D funding creates opportunities for low-volume, high-value visa categories
- PCAST report recommends premium processing for semiconductor visas

CHIPS R&D IMPLEMENTATION

Goal: Promote collaborative R&D ecosystem aligned with industry technology agenda

Key investment areas for NSTC and NAPMP



Support transition pathways for innovative technologies



Upgrade research infrastructure for early-stage ecosystem



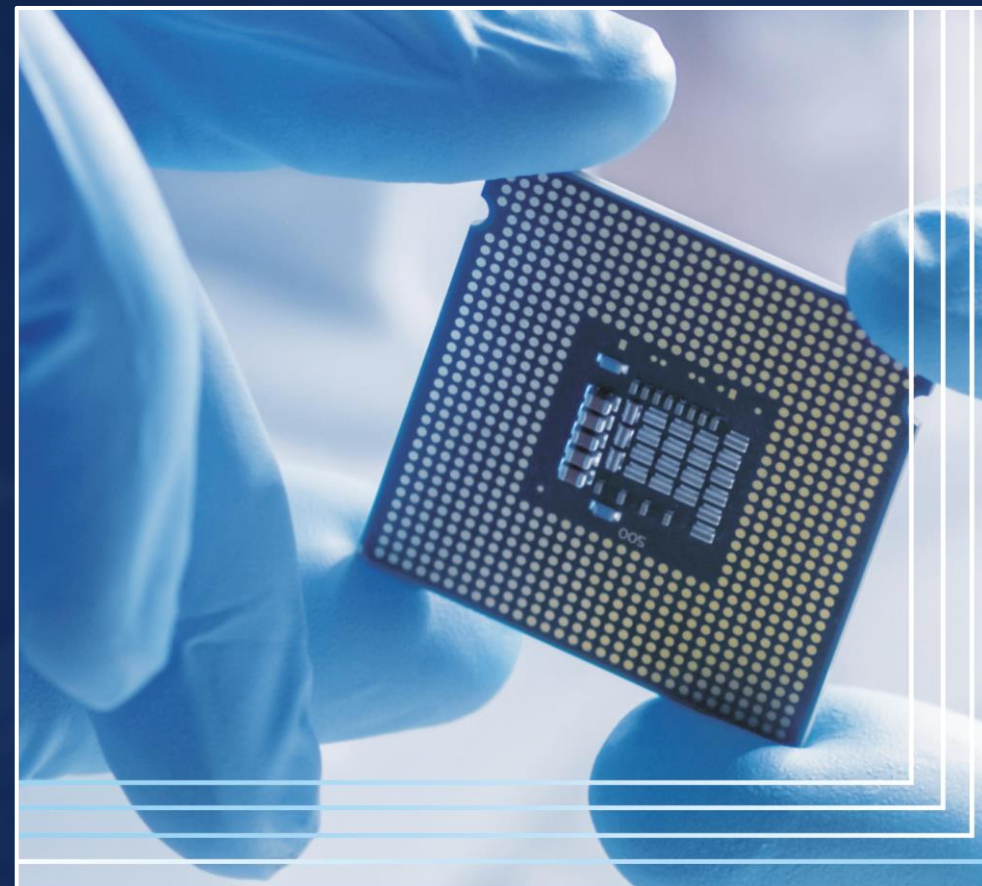
Establish and expand access for mid-stage development and prototyping infrastructure



Convene industry, academia, and government for collaborative innovation partnerships



Promote dynamic workforce programs to increase and hone domestic workforce



**American
Semiconductor Research:
Leadership Through Innovation**

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[semiconductors.org](https://www.semiconductors.org)

Thank You

ebreckenfeld@semiconductors.org