FormFactor™

Strategies for Wafer Probe in a Chiplet World

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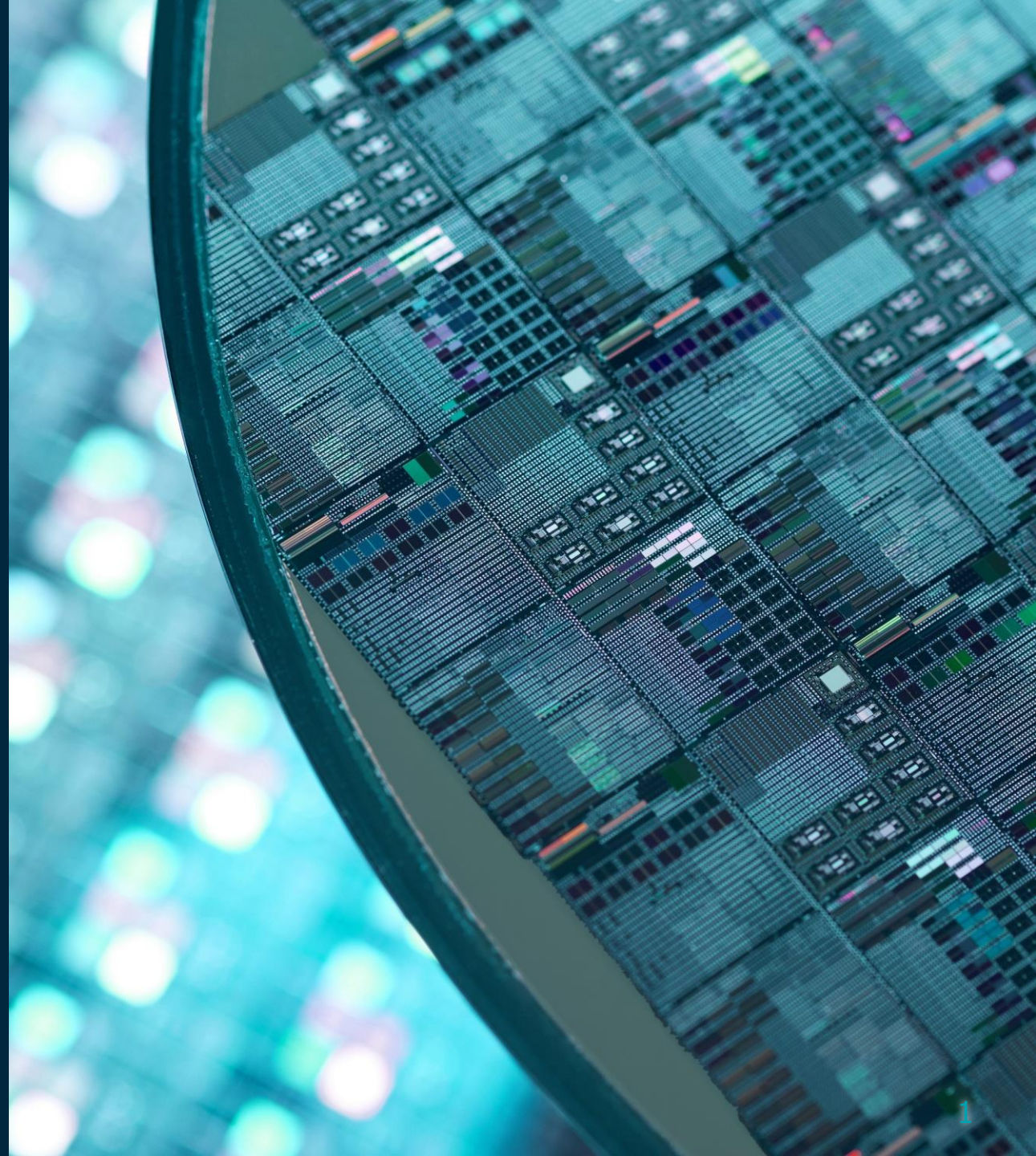
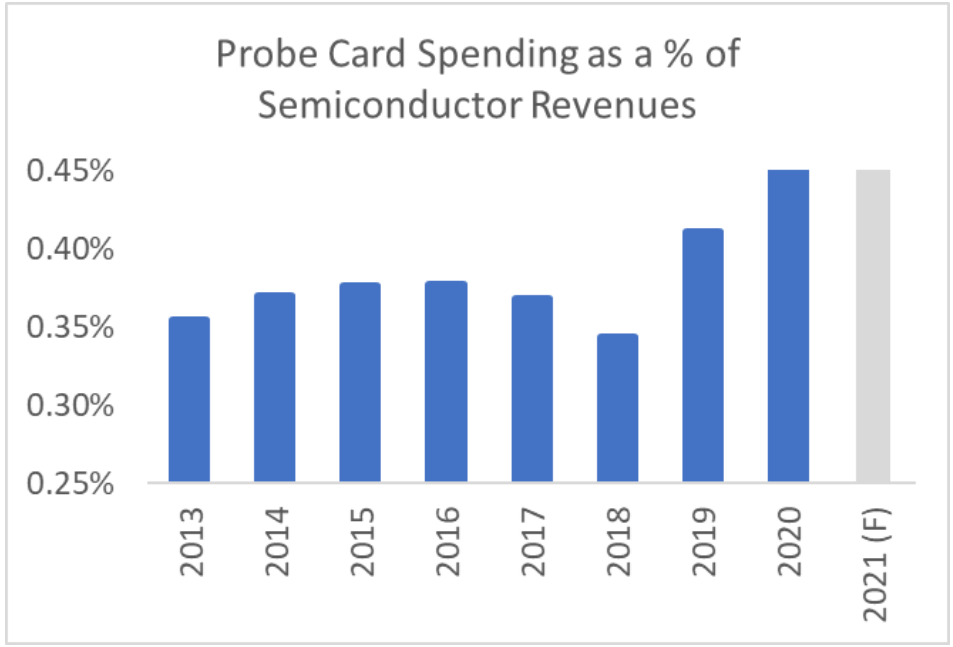


Strategies for Wafer Probe in a Chiplet World
A brief summary to get us started

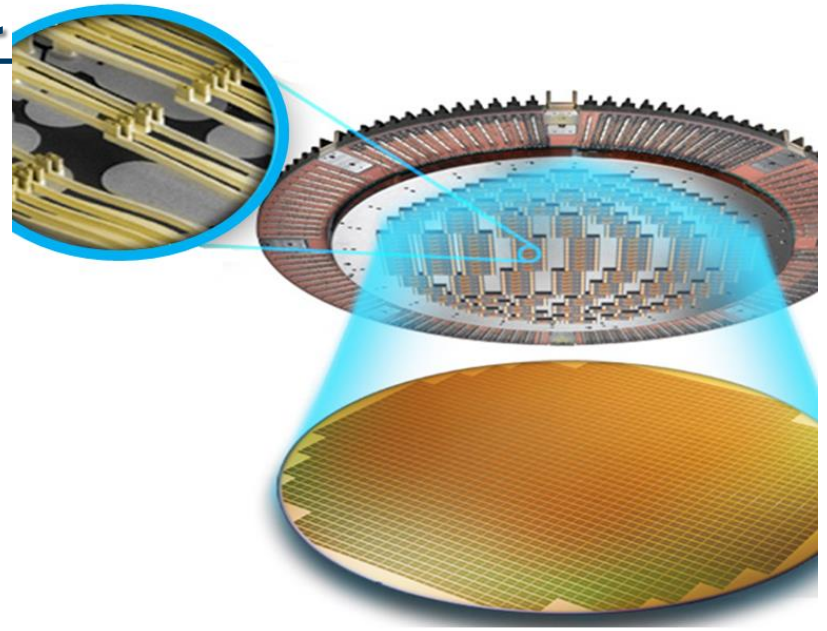
- Wafer probe/sort/test is increasing in importance
  - Probe card intensity up from ~0.35% mid-2010s to >0.4%
- Increase driven by multiple compounding factors
  - Shifting test content from final test to wafer test
    - Faster time to results, fewer bad die into assembly
  - Die-disaggregation composite-yield math is sobering
    - Compels need for (close to) Known-Good-Die into assembly
  - Driving up both test coverage and capability at probe



Source: The Probe Card Report 2021, VLSIResearch

- Historically, packaging interconnect structures have also served as probe interfaces
  - Works well at flip-chip pitches, but below that significant technical and cost challenges emerge
- About FormFactor: broad-based supplier of test & measurement products
  - #1 probe-card market share, engineering probers, metrology+inspection for advanced packaging
  - $760M trailing 12-month revenues, ~2300 employees worldwide

Why Do Customers Spend $$$ on Wafer Test

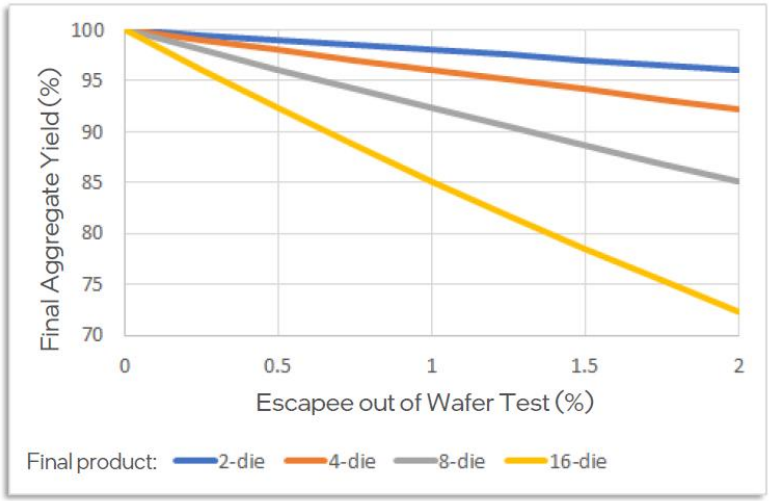


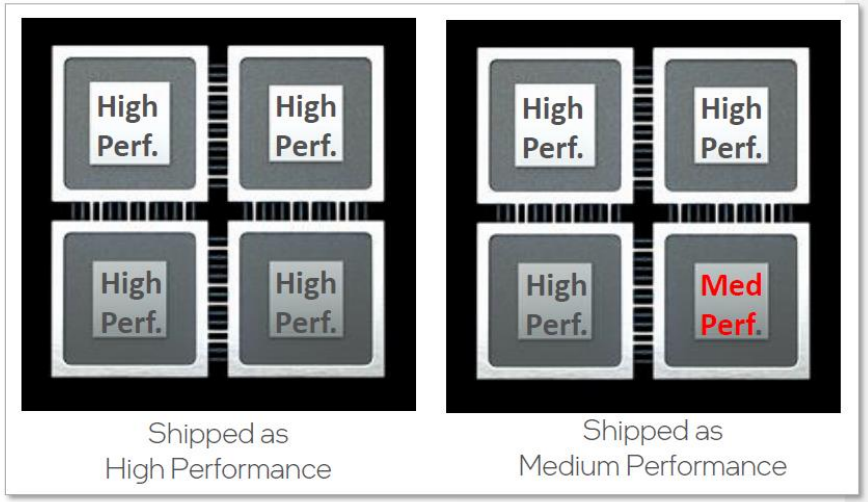
- **Avoid wasted cost of packaging a bad die**
  - Valuable when yield low and backend cost high
  - Test cost must be << bad-die packaging cost
- **Inform an adjustment/trim/change**
  - Exercise redundancy (DRAM)
  - Feedback for frontend fab process changes
- **As outgoing QC for product title transfer**
  - Bare-die sales (or wafer-packaged die)
  - Foundry-fabless-OSAT handoffs

Wafer Test Coverage			
Die Yield	High	Zero	Some
	Low	Some	Lots
		Low	High
		Packaging Cost	

Wafer Test/Probe is a Key Enabler for Advanced Packaging
The "chain" of chiplets is no stronger than its weakest chiplet

Impact to Test from Heterogenous Integration & Die Disaggregation





KGD has historically been associated with yield and the goal of minimizing number of defects escaping wafer test

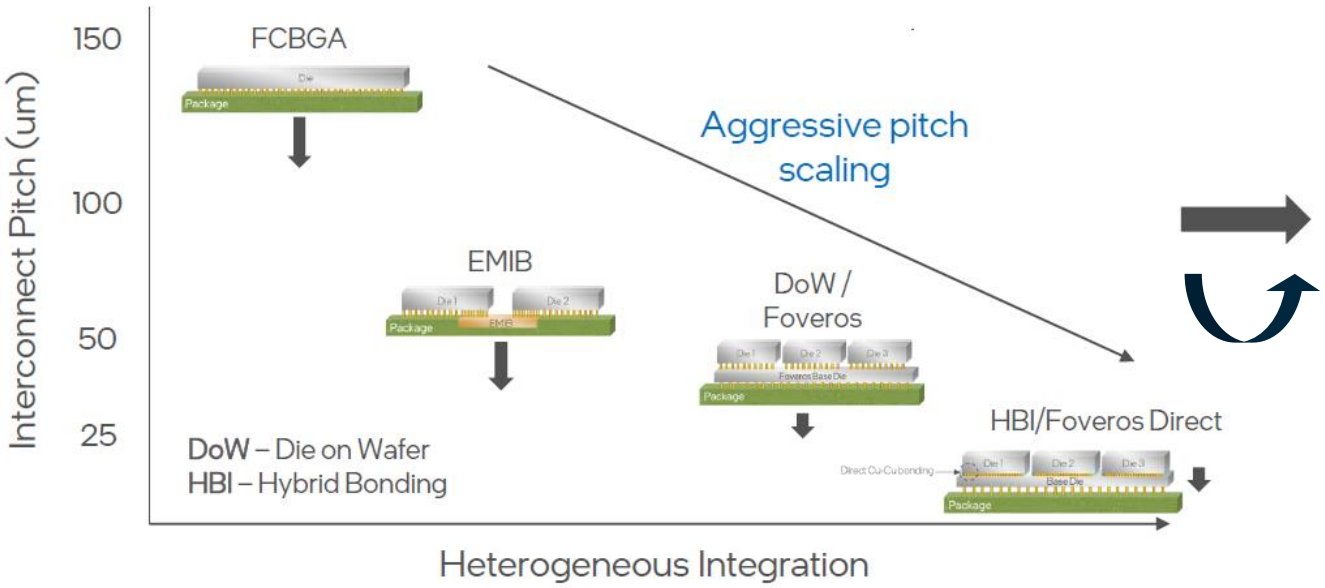
In addition to yield, die disaggregation demands an accurate prediction of device performance in the final package & system environment

- Economically viable multi-chiplet products require near-KGD component chiplets
  - This requirement is especially acute as the number of chiplets in the product increases
- Matching of component chiplet performance bins (right) is more subtle, but is also an important factor

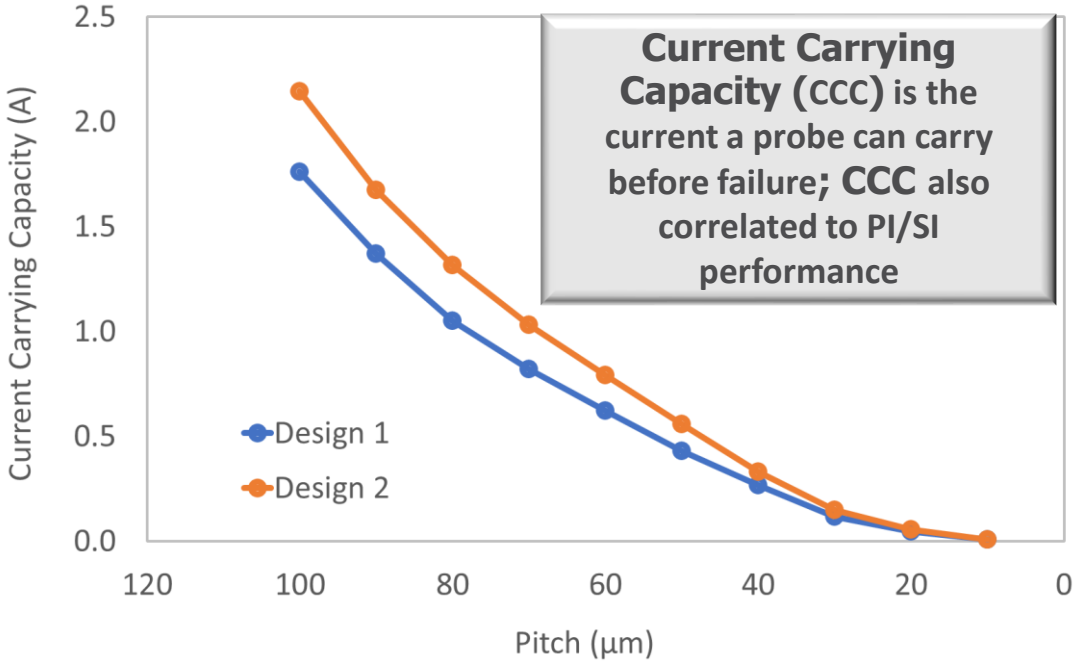
Source: Advanced Packaging Architectures, Opportunities and Challenges; Hamid Azimi, SEMICON West '21

Chiplet-to-Chiplet Interconnect Scaling Poses Challenges for Probe

Probing the assembly interconnects means pitch (and probably performance) reduction

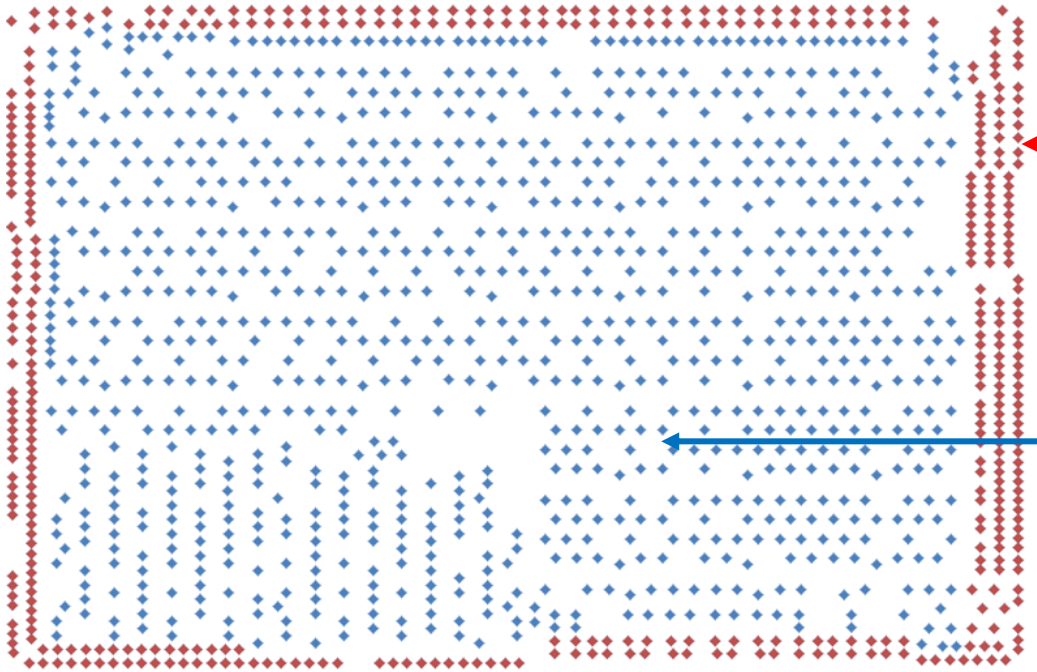


Source: Advanced Packaging Architectures…; Hamid Azimi, SEMICON West '21



- Historically, wafer probe has used the packaging interconnects (eg, flip-chip bumps) to connect to the die
- For a given probe design, geometric scaling generally results in reduced performance, eg, CCC at right
  - Lower CCC = more probe damage (repairs and downtime) and higher power impedance (yield and coverage)
- Potential advantage in decoupling packaging interconnect from probing contacts/interfaces
  - Ex: Dedicated test pads in TSV-packaged HBM DRAM enable one-touchdown parallelism, lowering cost of test

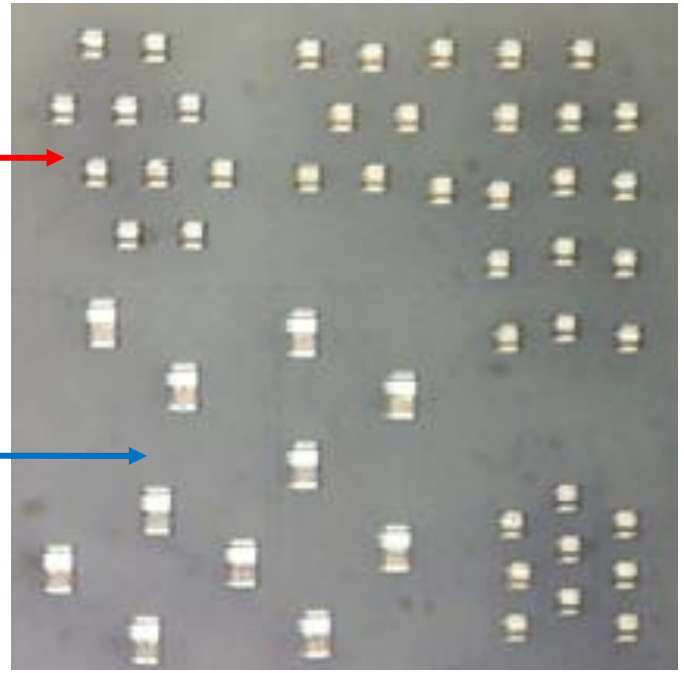
Optimizing Use of Packaging Interconnects - the "Hybrid" Probe Card
Use different probe designs in different areas of the die to do different jobs



Die Bump Layout

Utilize smaller probes for I/Os at tighter pitch

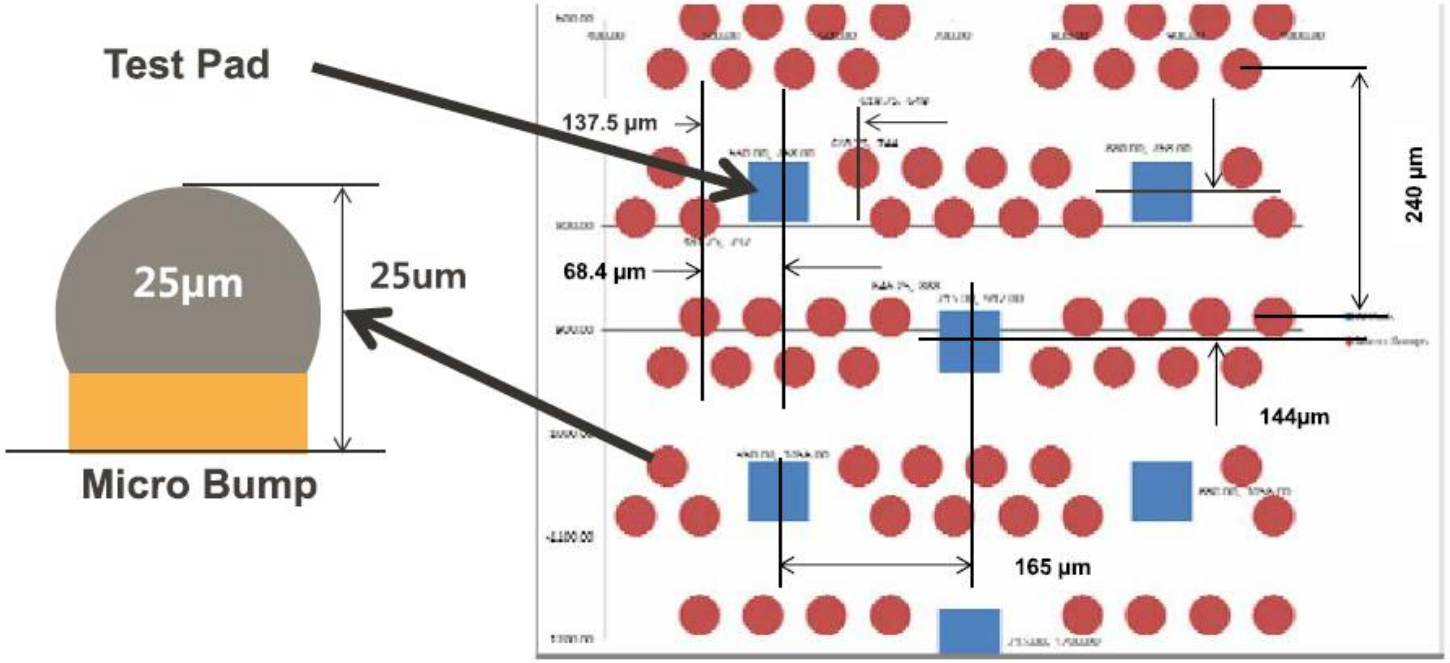
Utilize larger probes for power and ground with higher CCC requirements

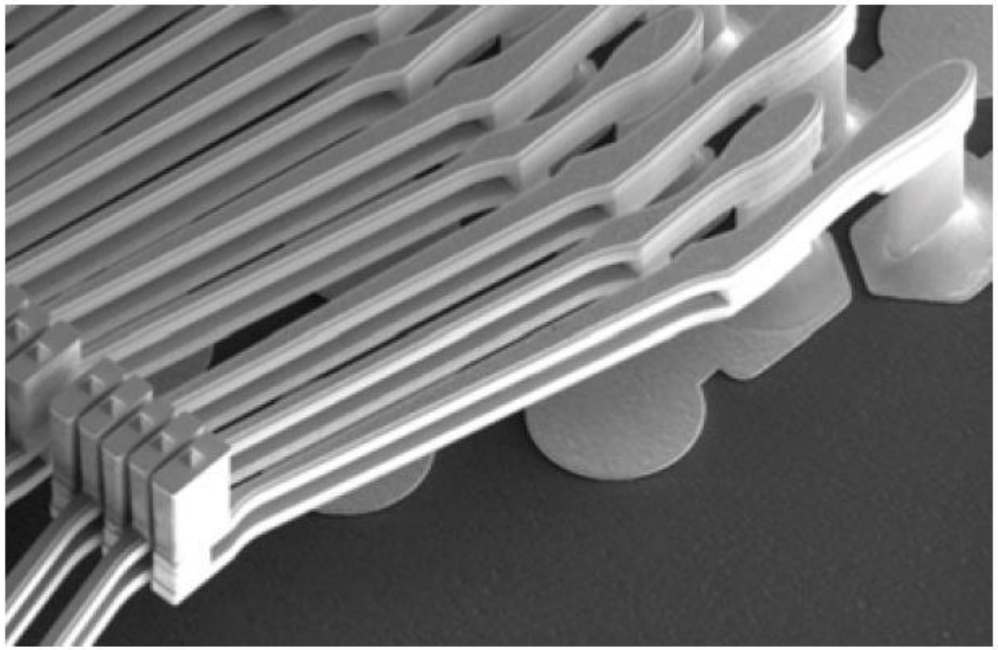


Local Image of Hybrid Probe Tips
(image is small sub-section of probe card)

- Layout of power and ground interconnects are often at larger pitches than the high-density fine-pitch I/Os
  - Hybrid probe cards exploit this, using larger probes with higher CCC on the powers+grounds (where it's needed)
- Benefit: Higher MTBF from less probe damage/repair, better test coverage from lower power impedance
- Variations on this general theme are possible, for example, a single probe that contacts multiple bumps

HBM: Don’t Probe the Micro-Bumps if You Don’t Have To





From Loranger+Yaglioglu (FormFactor) and Oonk (Teradyne), IEEE Design & Test 2016

- HBM DRAM die are sparsely populated with micro-bumps, real estate available for dummy test pads
- Some significant advantages to this approach, similar to “regular” DRAM sort
  - No micro-bump damage to worry/argue about
  - One-touchdown (whole wafer) parallelism provides a tremendous (~100x) cost advantage over single-die
- For high-volume HBM manufacturing, this has become the standard probe methodology
- Still more (high-speed) probe cards required, since one HBM stack is 8+ DRAM die and 1 SoC die

Summary and Conclusions

- Advanced packaging can pick up the slack from a slowing front-end-driven Moore's Law
- But, the burden shifts from the front end to the back end
  - Where lithography once drove, now assembly and test
- As a result, probe is becoming (legitimately) more valuable to the industry
  - And spending on probe cards is going up on both a gross and normalized basis
- Significant challenges with increasing test complexity and coverage
  - Both technical and economic challenges
  - Complexity: higher densities, faster speeds, etc.
  - Coverage: composite yields of component die
  - KGD is a comforting ideal, but too expensive
- And, remember probe is all about economics, so cost will rule the day
- Many options and choices available for optimization
  - Needs multi-supplier and customer collaboration

Q&A