Introduction to AIM Photonics and it's outside of the mainstream Laser-PIC integration with the AIM Active Interposer

June 29, 2022 1:00pm

David Harame and Colin McDonough

Outline

- Introduction to AIM Photonics
- Datacom trends and Co-packaged optics driving Si photonics packaging
- Getting light on and off the chip
- AIM Active Interposer as a co-packaging platform
- Heterogeneous Laser Integration on the Active Interposer
- Summary

Introduction to AIM Photonics

AIM Photonics Mission

Advance integrated photonic circuit manufacturing technology development

Meet commercial, defense and civilian agency needs

Create an adaptive integrated photonic circuit workforce

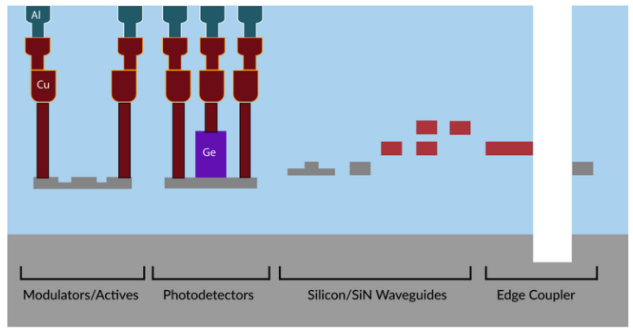
AIM provides an **accessible** best in class state-of-the-art 300mm Photonic Integrated Circuit & Heterogeneous-Integration technology as well as test, assembly, and packaging capabilities

- AIM uses the Albany Nanotech 300mm Facility
- >130K square feet of class-1 clean room operating 24-7
- Same facility used to fabricate 2nm transistors

AIM Photonics MPW Technology Offerings

https://www.aimphotonics.com/mpw

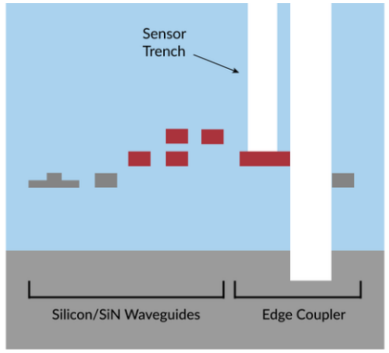
Active PIC



Base Active PIC

Si and SiN waveguides with active devices, Ge PD, two wiring levels and an Al termination pad

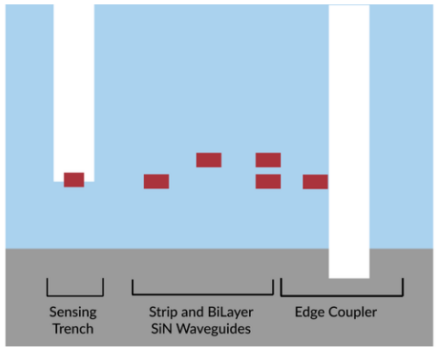
Passive PIC



Base Passive PIC

Silicon and silicon nitride waveguides with a trench down to the SiN

Low Loss SiN

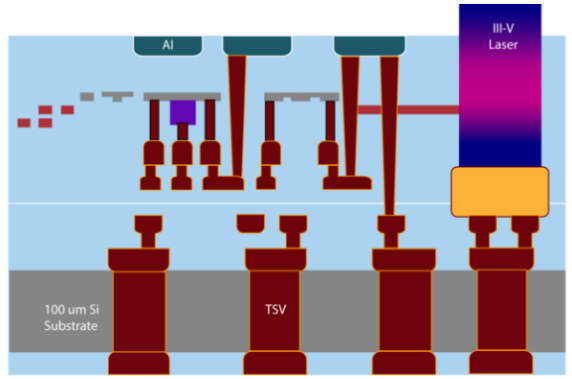


Nitride Only Passive PIC

Ultra low loss/low fluorescence silicon nitride waveguide and a trench to selectively expose the nitride waveguide

- MII use manufacturing relevant tooling and processes to address transitioning technology from basic research to manufacturing

Active Interposer

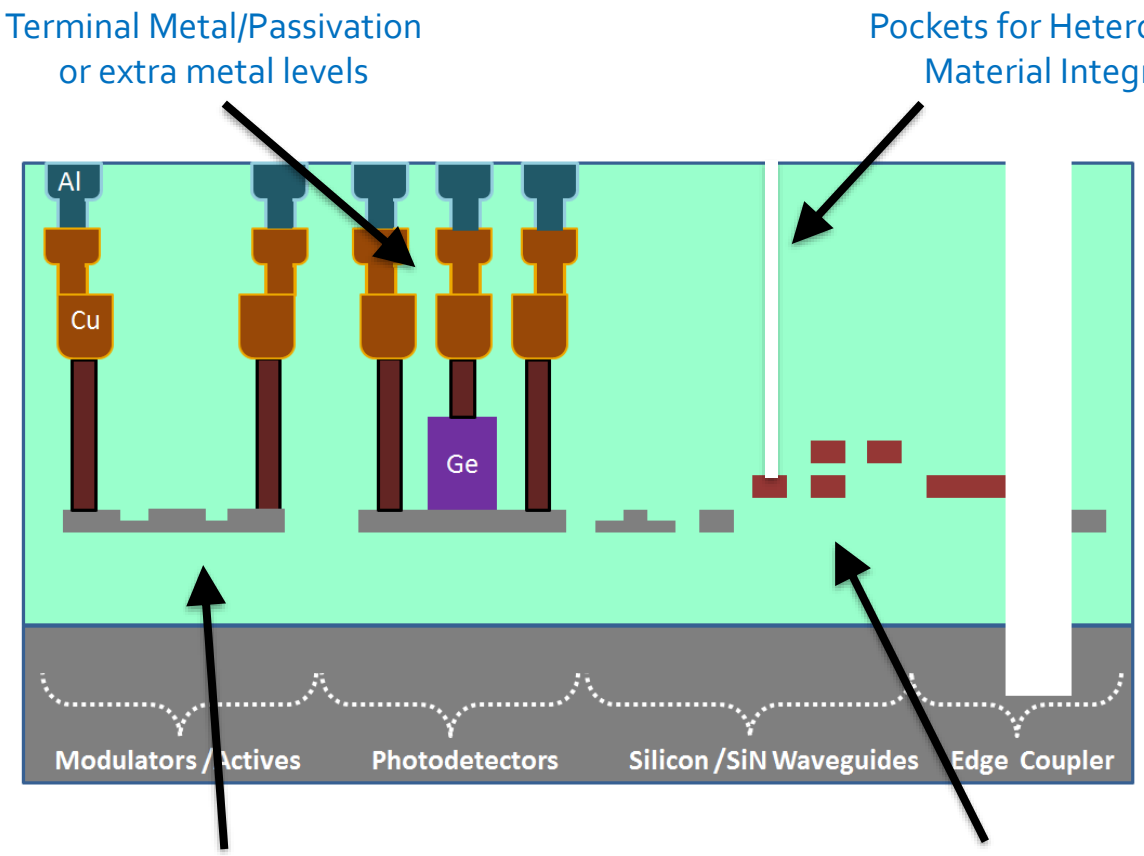


Active PIC Chip Carrier

Base Active PIC flipped to an interposer wafer with pockets for laser die attach

AIM Photonics Enables Bite Sized Custom

AIM Photonics is able and willing to provide low volume customizations for a wide variety of application spaces.



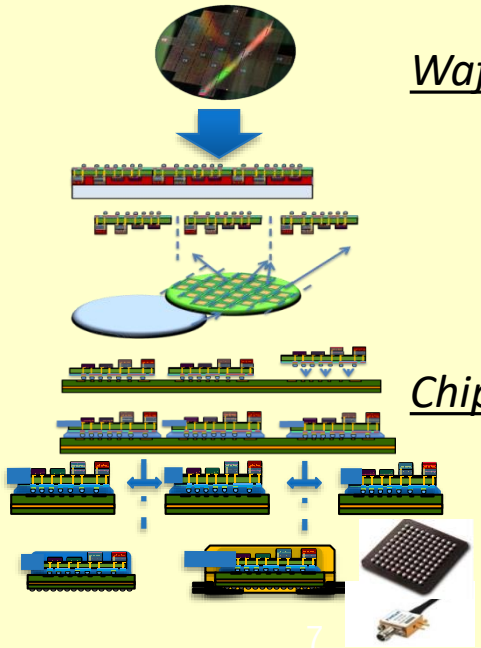
Other Possibilities:

-Wafer bonding to interposers or CMOS wafers

-Flip chip packaging of CMOS chips or laser die

AIM Test, Assembly & Packaging (TAP) – Rochester, NY

- *12,000 sq ft Class 1000 Cleanrooms*
- *Test & Metrology Lab*



<u>*Wafer-scale* Test and Assembly</u>

- Wafer-scale testing *(Opt/RF/DC)*
- PIC & Interposer Metallization
- Die bonding *(laser & PIC)*
- Singulation

<u>*Chip-scale* Test, Assembly and Packaging</u>

- Chip Scale Testing *(Opt/RF/DC)*
- Fiber and Laminate attach
- Surface Mount Assembly

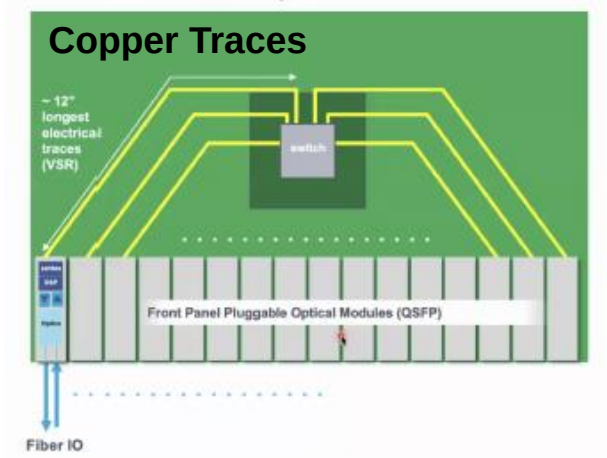
300mm, Open Access, Photonics & Electronics Packaging <u>Development Center</u> with Wafer Scale and Chip Scale capability

- Fiber Attach
- Flip Chip (photonic & electronic)
- Wafer Probing
- Dicing
- Die Attach
- Wire Bonding
- Metallization
- Bumping
- Metrology

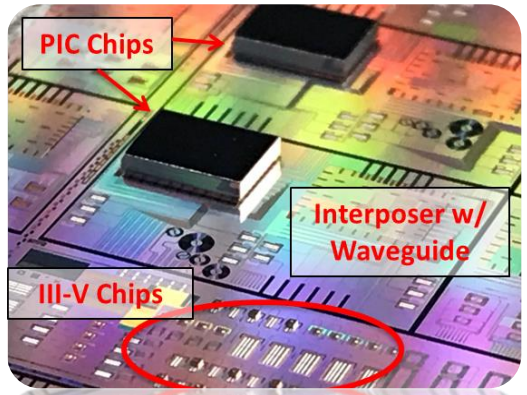
DATACOM Scaling and Co Packaged Optics

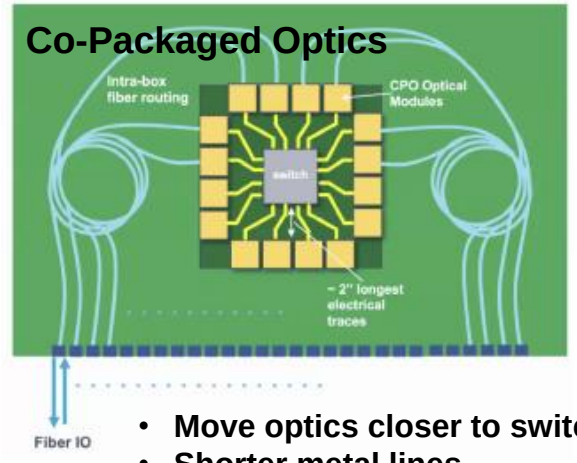
IPSR Datacom Photonics Report

- Question addressed: What are the roadblocks & solutions to get to > 1 Pb/s
- System software, hardware and architecture will have to coordinate progress into a new Interconnect Scaling paradigm.
- Architectures will densify to meet metal interconnect limits.
  - electronic-photonic co-package integration will first meet off-chip interconnect requirements
  - …and later disaggregate as electronic-photonic integration becomes pervasive
- Accelerating compute performance increases compulsory data movement.
- For > 50 Tb/s there is a feasibility gap: need a plan B
  - No simultaneous solution for cost, power, reliability, deployment
- The Chip era has ended.
  - The System-in-Package era in full implementation…with photonic functionality a requirement



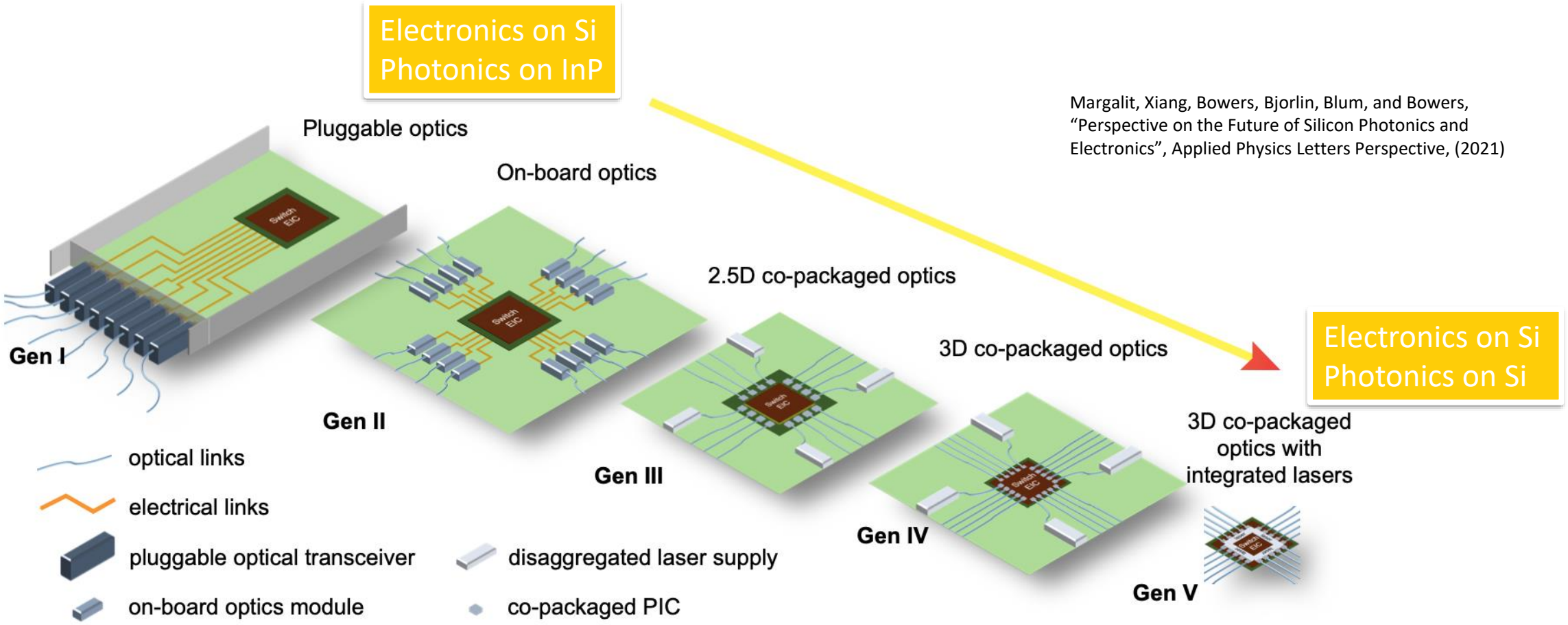
- **Increase # metal lanes**
- **Increased SERDES power budget**





- **Move optics closer to switch**
- **Shorter metal lines**
- **Lower SERDES power**

Economic Driver: Merging Photonics and Electronics

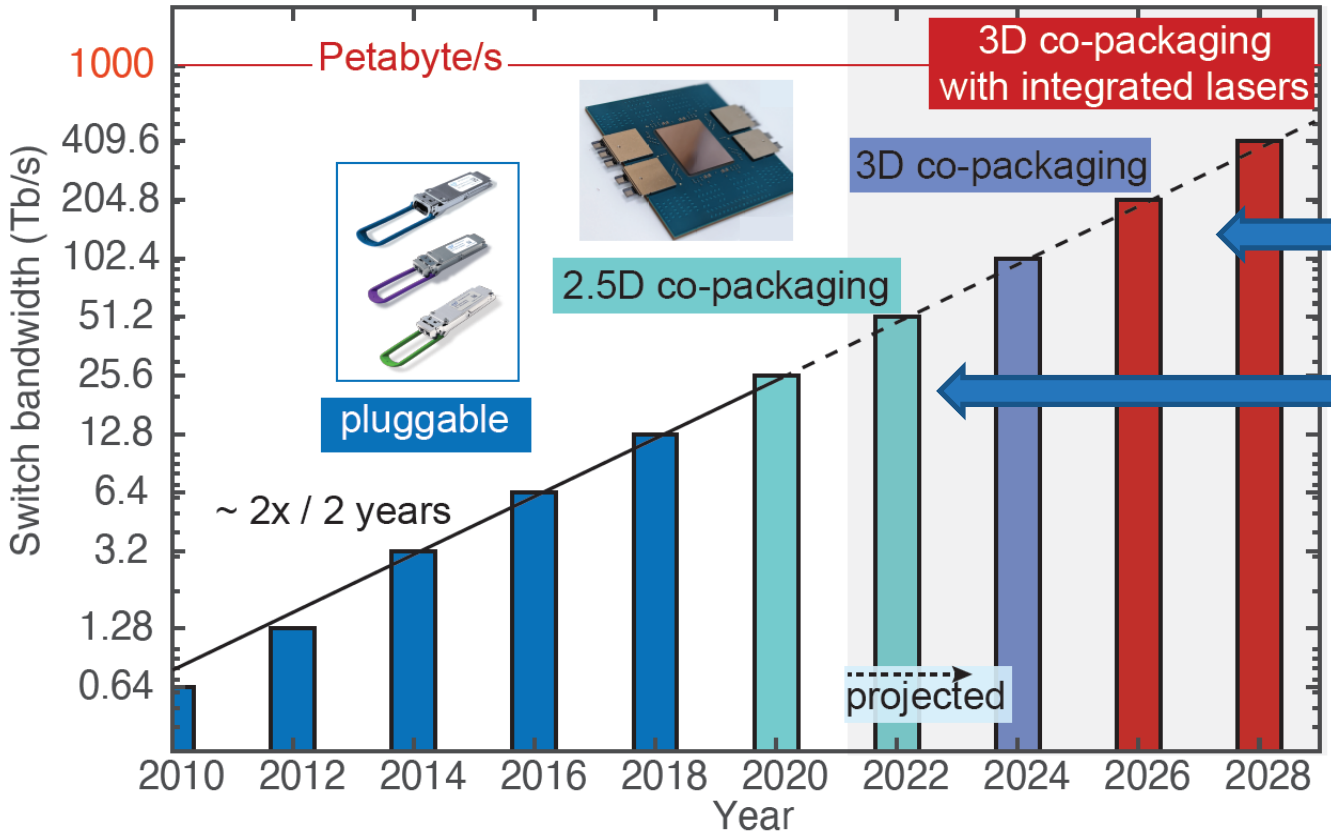


Margalit, Xiang, Bowers, Bjorlin, Blum, and Bowers, "Perspective on the Future of Silicon Photonics and Electronics", Applied Physics Letters Perspective, (2021)

- Generations of optics and the evolution of co-packaging technologies used in data center applications.
- The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip.

High Capacity Switches (Broadcom, Intel, Cisco, …)

Margalit, Xiang, Bowers, Bjorlin, Blum, and Bowers, "Perspective on the Future of Silicon Photonics and Electronics", Applied Physics Letters Perspective, (2021)



204 Tb/s in 4 yrs

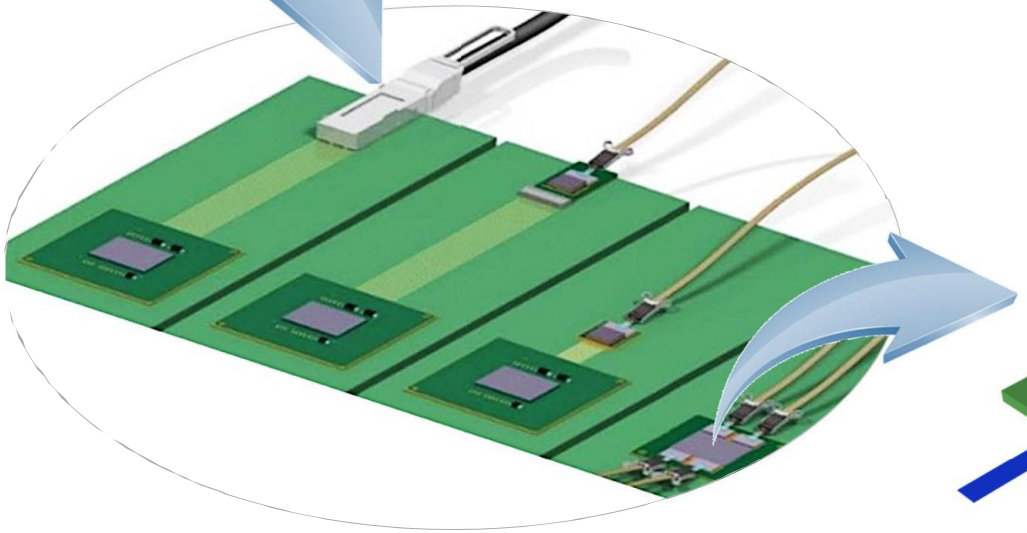
25.6 Tb/s Today

- Switch bandwidth evolution and outlook over the years with four generations.
- Inset pictures show commercially available pluggable transceivers from Intel and a 2.5D co-packaged PICs and switch from Broadcom.
- The year indicates when the technology is first deployed.

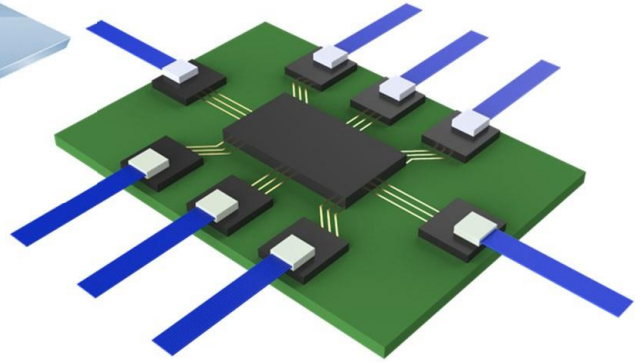
From Pluggable to Co-Packaged Optics

Pluggable Optics

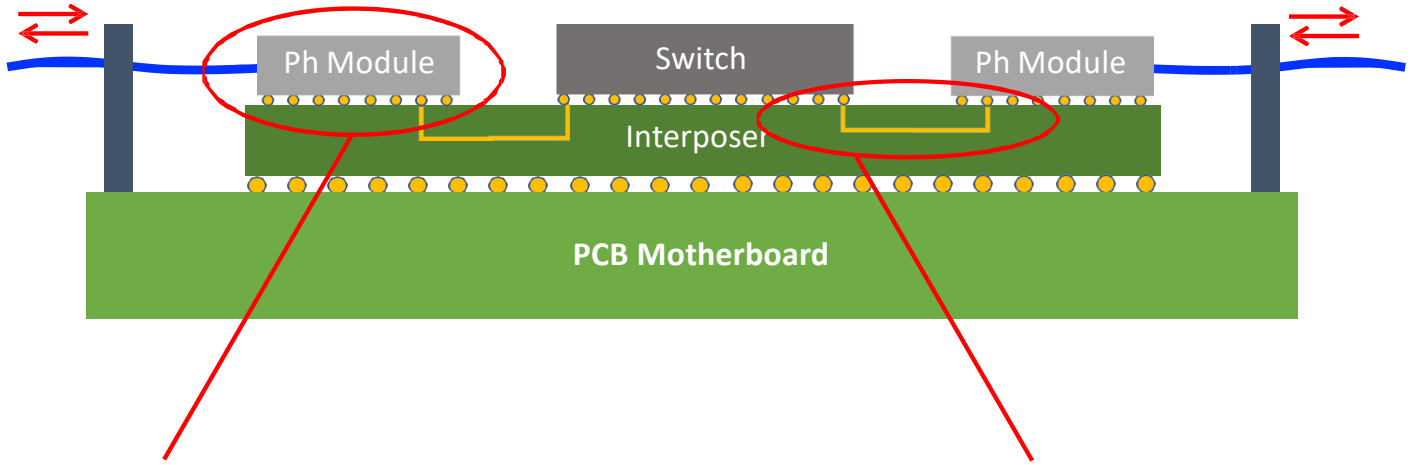
- **Optical Fiber Packaging** (shoreline density)
- **Laser Integration** (external or internal laser)
- **Electrical Packaging** (2.5D integration & interposers)
- **Assembly Sequence** (manufacturing & yield)



Co-Packaged Optics



Co-Packaged Optics (Packaging Challenges)



Photonic Module/Engine

- Photonic & Electronic Devices
- Optical Fibre Packaging
- Laser Integration
- Electrical Packaging
- Assembly Process Sequence

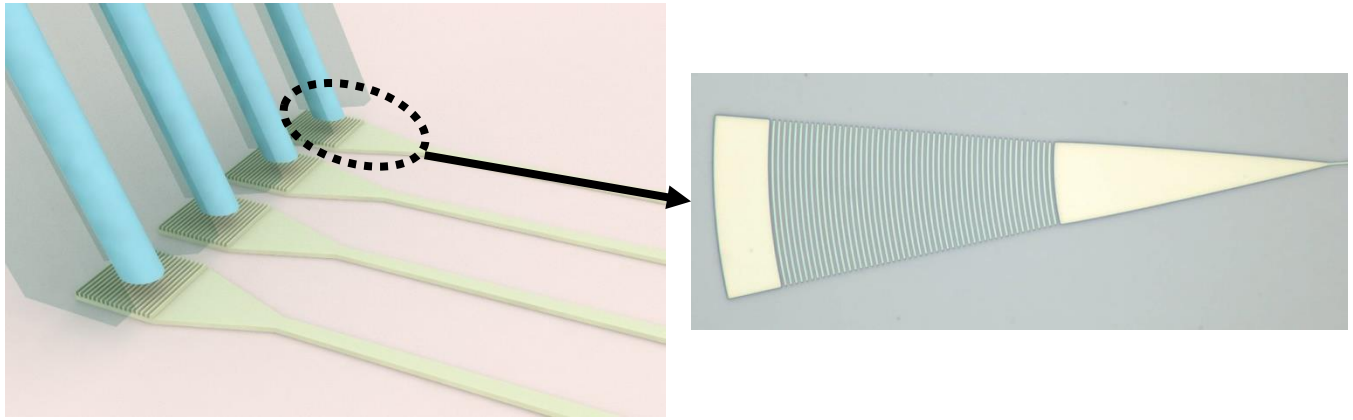
Co-Packaging with Switch

- Heterogeneous Integration
- 2.5D Packaging
- Electrical Interposer Technology
- EMIBs

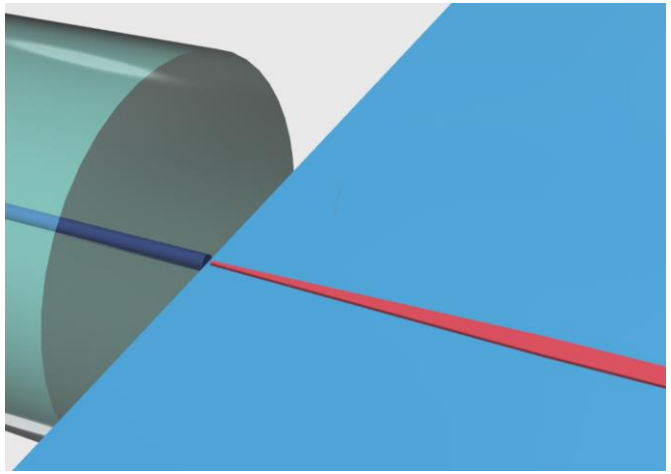
Getting Light on and Off the chip

Silicon Photonic Coupling Challenges Overview

- Optical fibers have a mode field diameter of 10 µm. This makes it challenging to couple light into the sub-micron Silicon photonic waveguides.
- Two techniques for coupling from fiber-to-chip are inverse tapers and grating couplers:
- Grating couplers allow light to be coupled into the surface of the chip (which is advantageous for testing) and is more tolerant to misalignment than inverse tapers.
- Inverse Tapers match the optical mode of the Silicon waveguide to the mode of the fiber (i.e. the mode becomes larger), which realizes better optical coupling.



Representation of a fiber-to-chip grating coupler

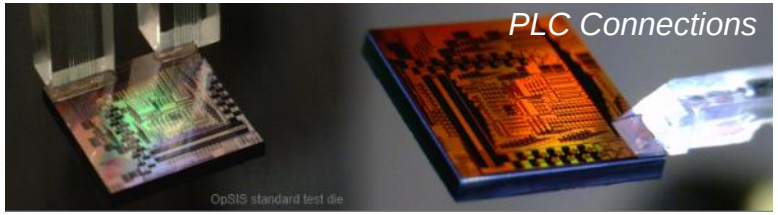


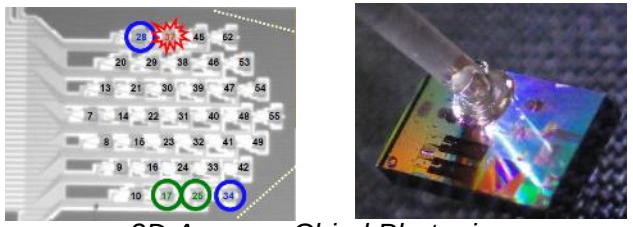
Representation of a fiber-to-chip using an Inverse Taper

Grating vs Inverse Taper Coupling

Grating Coupling

- Advantages:
  - Easy alignment (±1 µm)
  - High Density of Channels (100's – 2D)
  - Wafer level coupling (no dicing)
- Disadvantages:
  - High coupling loss (Typ. 3-4 dB)
  - Low bandwidth (<100 nm)
  - Polarization handling is challenging – requires special designs (high loss)
  - Surface normal packaging

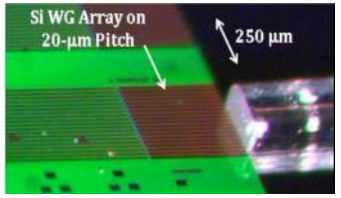




2D Arrays – Chiral Photonics

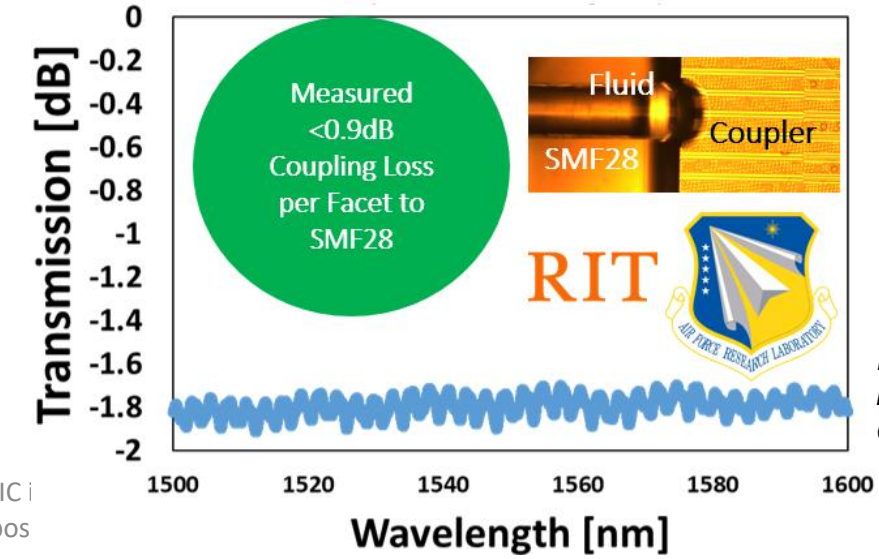
Inverse Taper Coupling

- Advantages:
  - Low coupling loss (1-2 dB)
  - Broad bandwidth (>100 nm)
  - Polarization maintaining
- Disadvantages:
  - Poor alignment tolerance (evanescent coupling can solve)
  - Lower channel density (10's – 1D)
  - Requires edge preparation (etch or polish)
  - Efficient coupling to SMF28 requires thick BOX or Silicon substrate removal/undercut



Chiral Photonics

PLC Connections

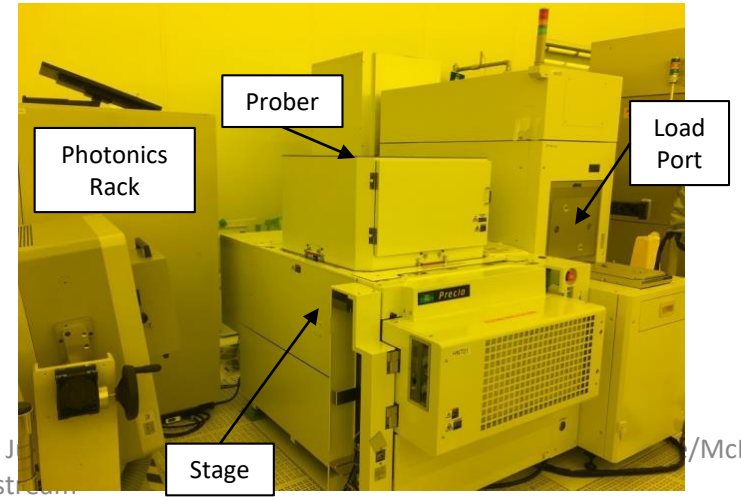


Recent AIM Photonics' inverse taper results. Courtesy of RIT Preble

On-site capability

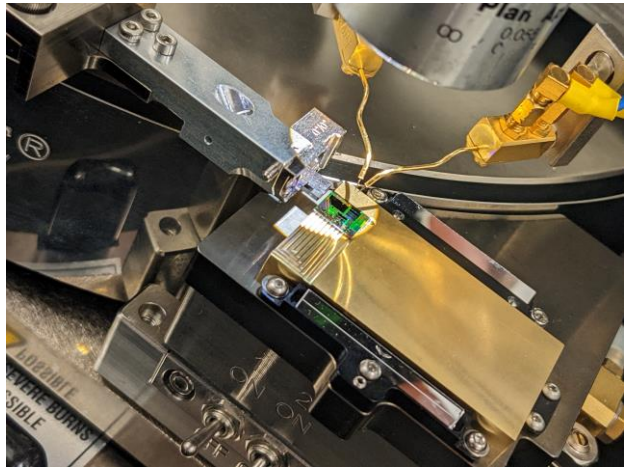
Grating Coupling

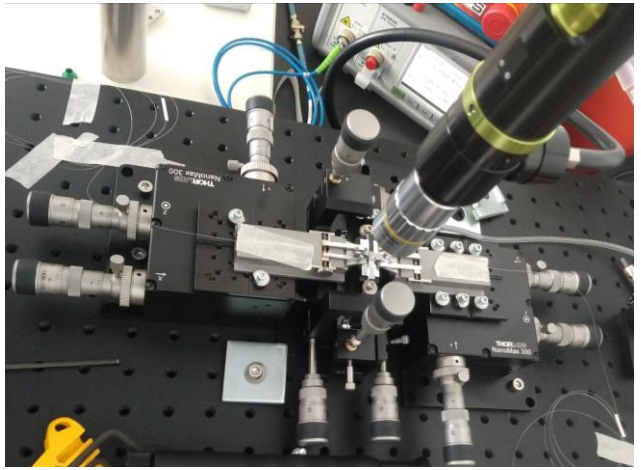
- Both inline and offline probers
- Wafer Quality Control:
  - Waveguides, Passives, Actives
  - Process/Line Control
  - Module monitoring
  - Continuous improvement
- Measurements
  - O,C,L – band
  - Polarization – full Miller matrix analyzed
  - DC electrical signals applied and read
  - Fully automatic alignment of multiple optical channels (8-12) and electrical probers



Inverse Taper Coupling

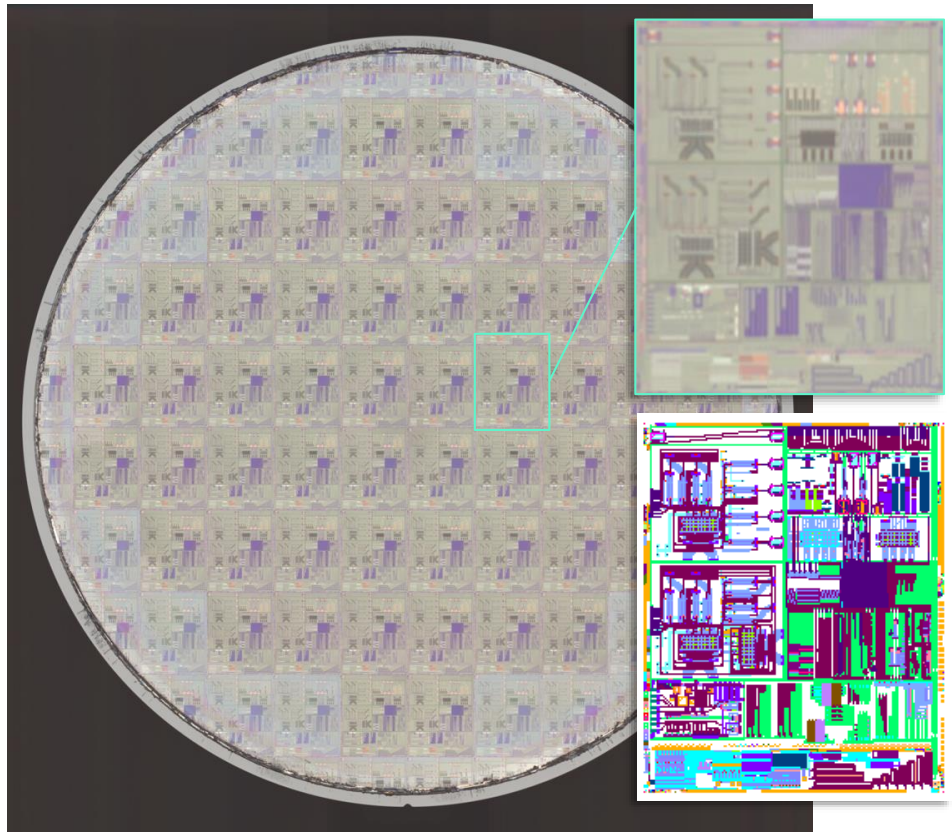
- Offline wafer-scale prober and microbench
- Die/chip Quality Control:
  - Waveguides, Passives, Actives
- Measurements
  - O,C,L – band
  - DC electrical signals applied and read

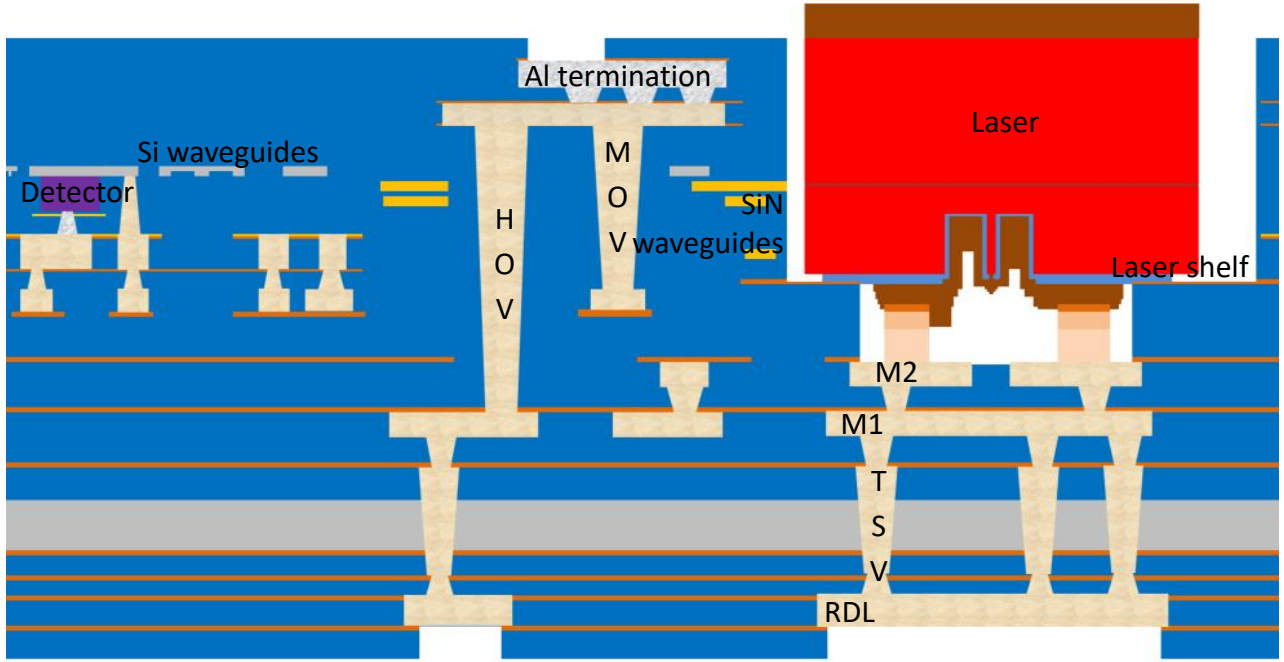


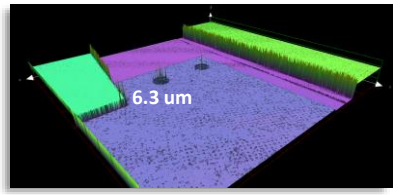


AIM Active Interposer a platform for Co-Packaged Optics

AIM Active Interposer with Integrated Laser





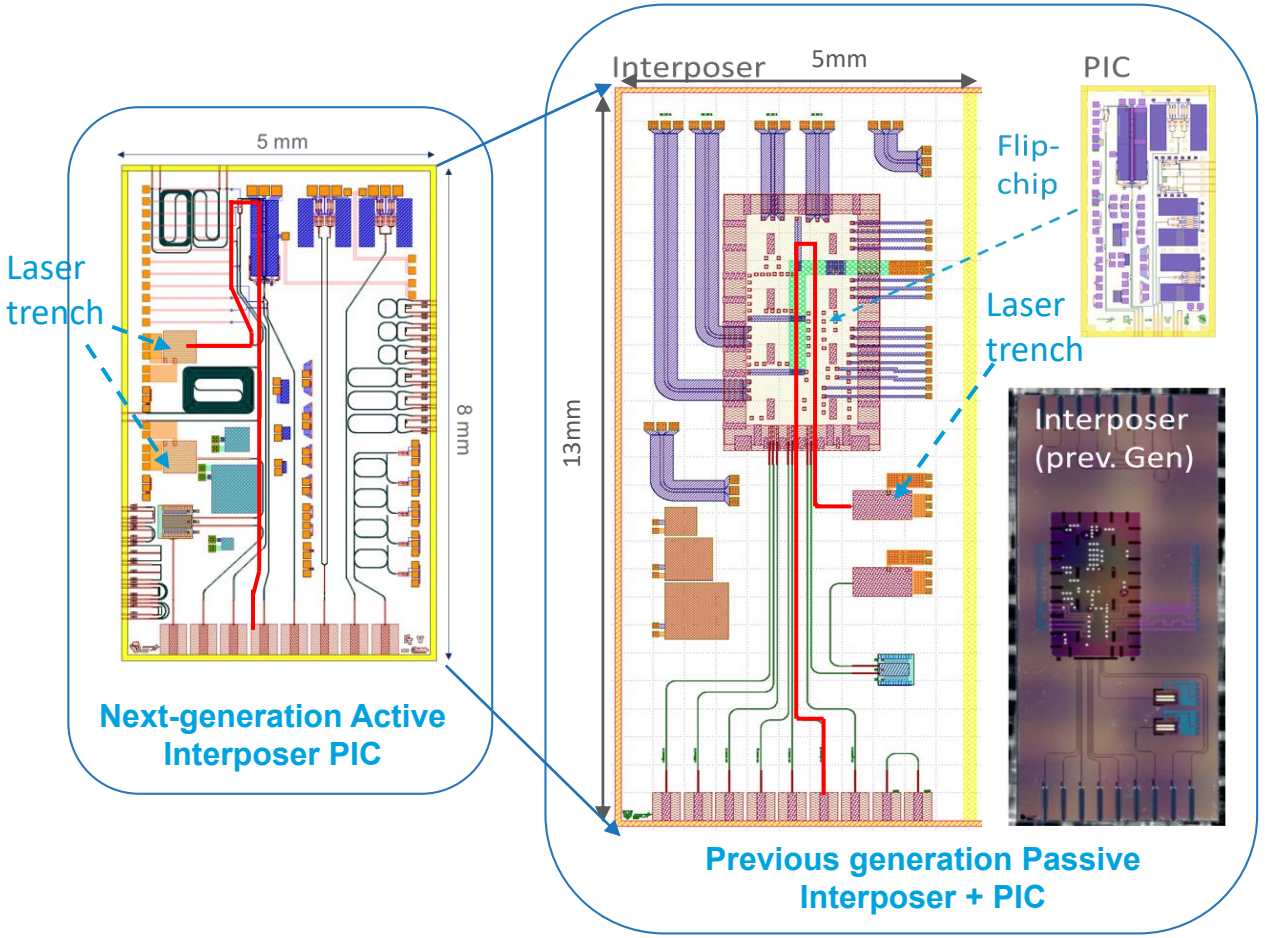


3D Profile of Laser Trench

Active Interposer is a platform for enabling co-packaged optics.

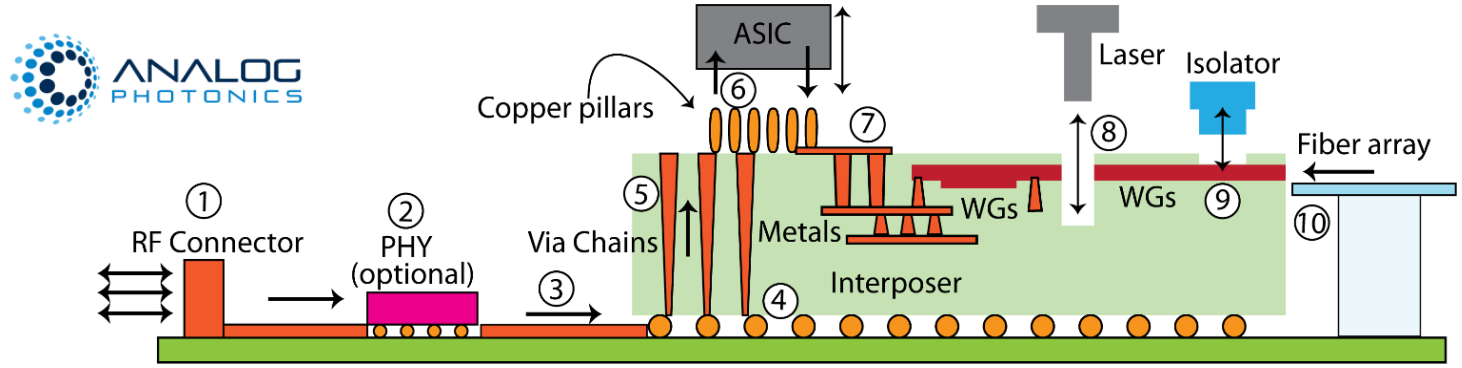
Evolution to the Active Interposer from Passive Interposer

- Active Interposer benefits:
  - Improved photonic subassembly
  - Removes 2 coupling facets from the current passive interposer for improved performance and manufacturability
  - Potential for reduced footprint
- Passive photonic interposer (Gen 2)
  - Accepts PIC, laser die
  - Fiber trenches for fiber attach
  - Waveguide routing between PIC, laser die, and fiber
  - RF transmission line traces
- Active photonic integrated circuit (PIC)
  - High-speed MZM and photodiodes
  - Integrated capacitor structures for DC blocking/ AC coupling
- Laser die (trench location indicated)



Courtesy of Lockheed Martin

Packaging PDK – An Optical Co-packaging Platform



Impact: Built a reference platform and PDK that…

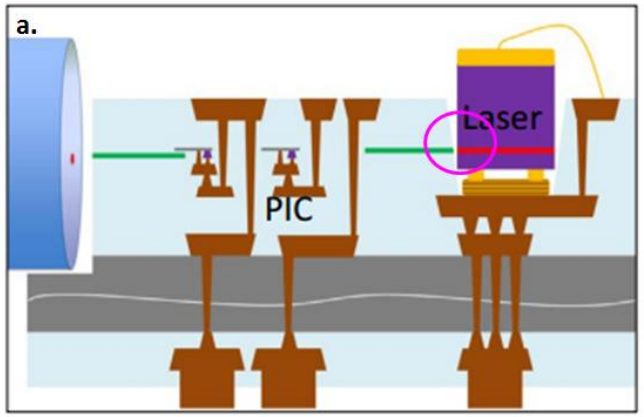
- includes Laser, PIC, ASIC, FAU, PCB, Electrical (RF, Mixed-Signal, Analog) verified Packaging PDK interfaces and component library.
- is reused to develop, verify and test packaging interfaces [1,3-8,10].
- provides steps using AI Platform with TSVs, TOVs and RDL.
- provides laser integration into the photonics (isolation, back-reflection, thermal issues).
- provides a template for reflowable electrical and optical interfaces.

PDKv1.0 Deliverables

		Model Type/Format			
Component Group	Components	Electrical/Optical	Thermal/Optical	Mechanical	Document
PIC to Board, IC, Fiber and Laser	Through silicon vias	.s2p or .sNp	N/A	N/A	Yes
	Through oxide vias	.s2p or .sNp	N/A	N/A	Yes
	Wirebonds	.s2p or .sNp	N/A	N/A	Yes
	Bumps and/or Copper Pillars	.s2p or .sNp	N/A	.dwg or .dxf	Yes
	Fiber to Chip Edge Couplers	EPDA	EPDA	N/A	Yes
	Fiber to Laser Edge Couplers	EPDA	EPDA	N/A	Yes
	Differential RF trace	.s2p or .sNp	N/A	N/A	Yes
	Single Ended RF trace	.s2p or .sNp	N/A	N/A	Yes
	IC Attach Pad	.s2p or .sNp	N/A	N/A	Yes
Reference Board	RF to Board connectors	.s2p or .sNp	N/A	N/A	Yes
	RF Board Trace	.s2p or .sNp	N/A	N/A	Yes
	RF Board SMT Bias Tee	.s2p or .sNp	N/A	N/A	Yes
	RF Board SMT Capacitor	.s2p or .sNp	N/A	N/A	Yes
	On Board IC attach rules (Optional)	N/A	N/A	N/A	Optional
	Design/Attach Rules for PIC (Optional)	N/A	N/A	N/A	Optional
Lasers or Gain Integration	Laser or Gain Abstract	.gds or .oas	EPDA	.dwg or .dxf	Yes
	Design/Attach Rules (Optional)	N/A	N/A	N/A	Optional
IC Attach (Optional)	Design/Attach Rules (Optional)	N/A	N/A	N/A	Optional
Fiber Attach	Fiber Array Unit	EPDA	N/A	.dwg or .dxf	Yes
	Single Fiber Attach	EPDA	N/A	.dwg or .dxf	Yes
	Epoxy and Attach Process (Optional)	N/A	N/A	N/A	Optional
	Software Tools	Lumerical, COMSOL, Solidworks or EPDA partner specified			

Heterogeneous Laser Integration: Approach and Challenges

Heterogeneous Laser Integration Approach



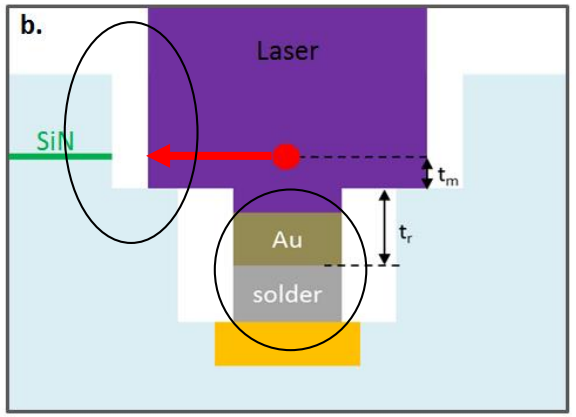
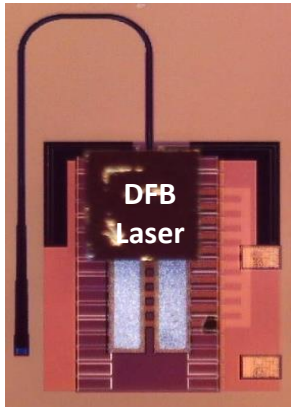
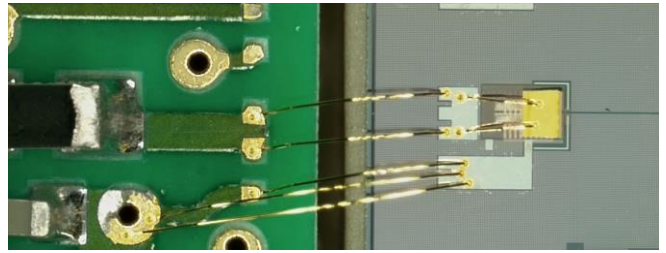
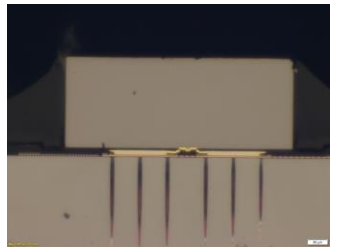


Figure 1. Cross-section of the active interposer with a flip-chip attached III-V laser source. **b.** Detailed structure of laser reference layer to output mode (t_m), reference layer to Au bond pad (t_r), and dielectric shelves for laser placement.





Laser on Interposer wired out to PCB



TSVs as thermal vias

- Flip-chip laser attach in edge coupling
  - More broadband than grating coupler
  - Higher coupling efficiency
  - Polarization insensitive
- Utilizing Known-Good-Die (KGD) to maximize yield
- Platform flexibility: laser trench formation and waveguide layers
- Heat sinking with thermal vias possible

- <u>Packaging Challenges</u>
  - Robust solder joint
  - High coupling efficiency
    - Mode matched edge coupler design
    - Laser alignment
  - Thermal management
  - Throughput

Die and flip-chip bonding tools

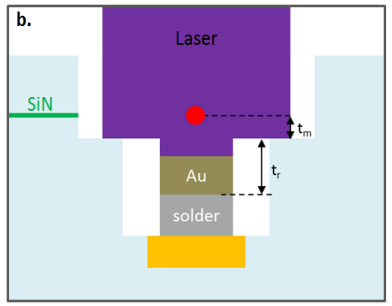
Finetech FINEPLACER Femto2 (TAP)

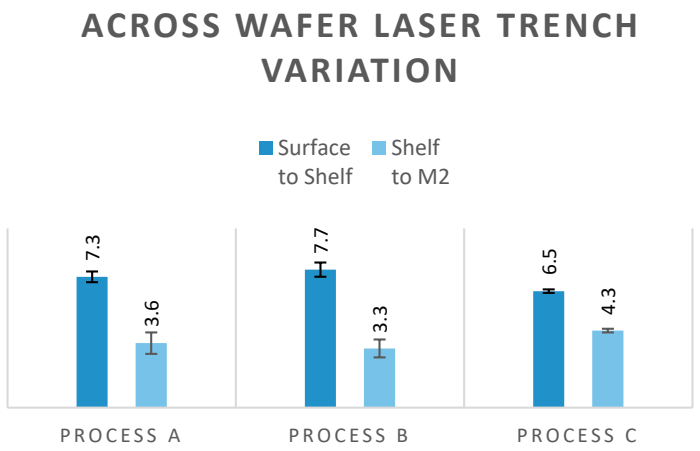
- Accuracy ±0.3µm @ 3sigma
- Bond force up to 40 N
- Min Cycle Time 20 sec
- Assembly of chip and micro-optics (WDM, optoelectronic components, micro-lenses, micro- mechanics)
- Epoxy dispense, flux dip station, automated die flip station
- Eutectic bonding via heating plate and heated tool vacuum tip
- Passive alignment
- UV cure

ASM Amicra NANO (Albany)

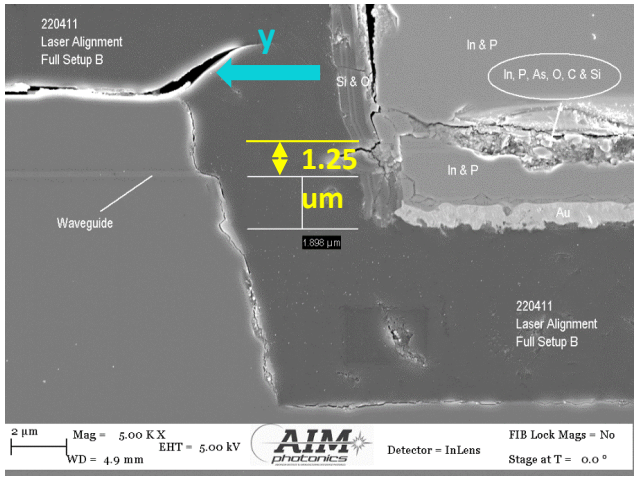
- 300mm wafer handling
- Accuracy ±0.2µm @ 3sigma
- Cycle Time < 35 sec
- Assembly of chip and micro-optics (WDM, optoelectronic components, micro-lenses, micro-mechanics)
- Epoxy stamping and dispensing
- Eutectic bonding via diode-laser or heating plate
- Passive alignment
- UV cure

Vertical Laser Alignment – Trench

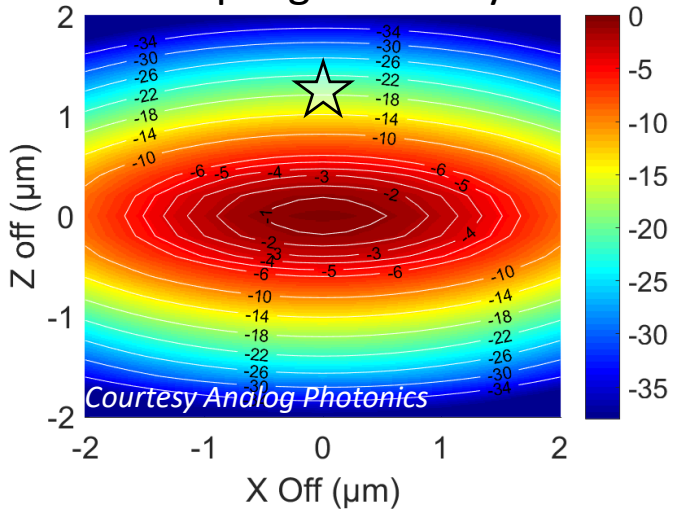




Misaligned Laser Example

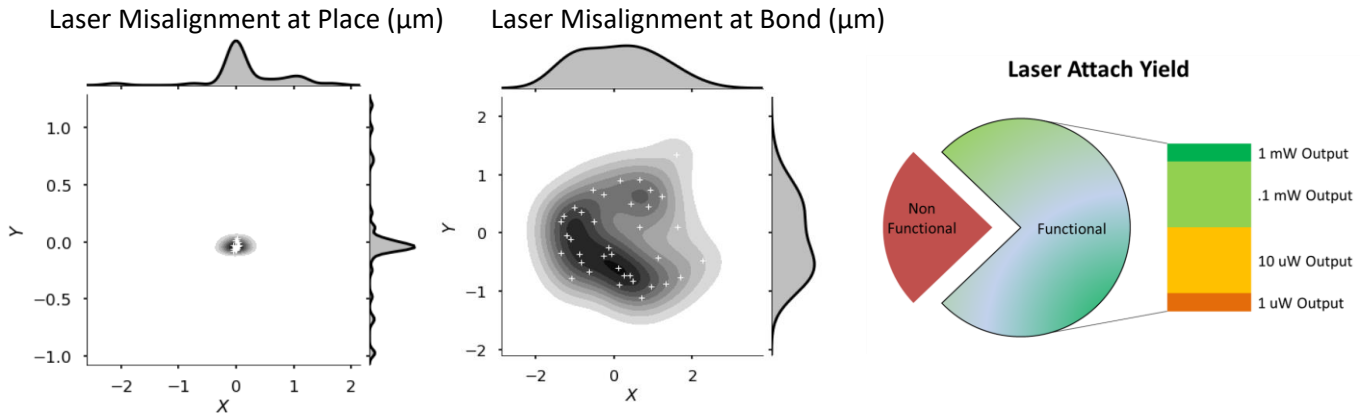


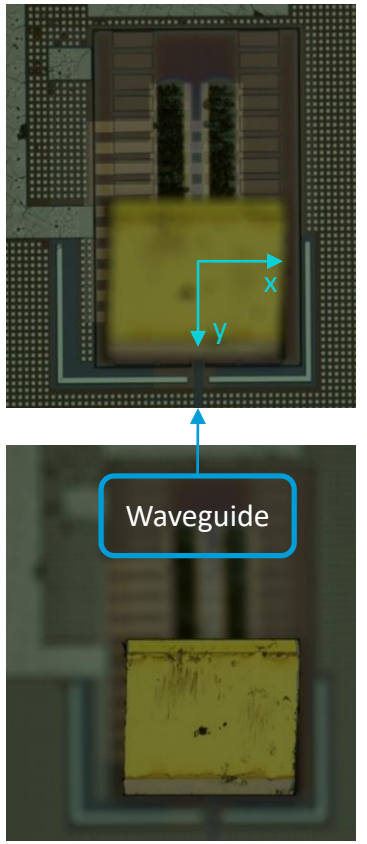
Coupling Efficiency

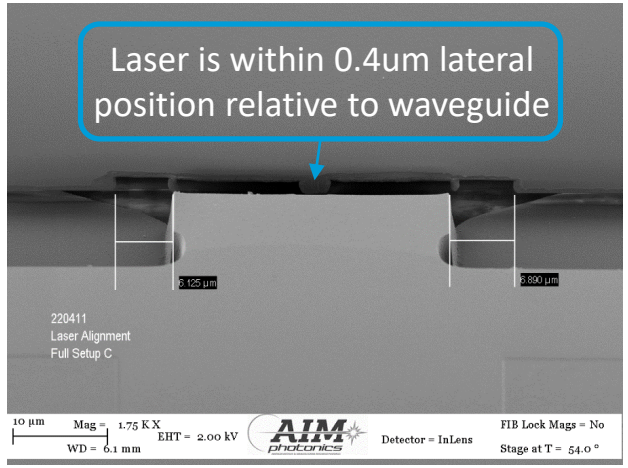


- An asymmetric laser mode profile of lasers means coupling efficiency is most sensitive to vertical misalignment
  - Spot size converters can help by increasing the mode size
- Vertical alignment is set by the layer stack structure, allowing for <0.5um across wafer uniformity
- Optimizing etch process and etch stop materials is key for yield

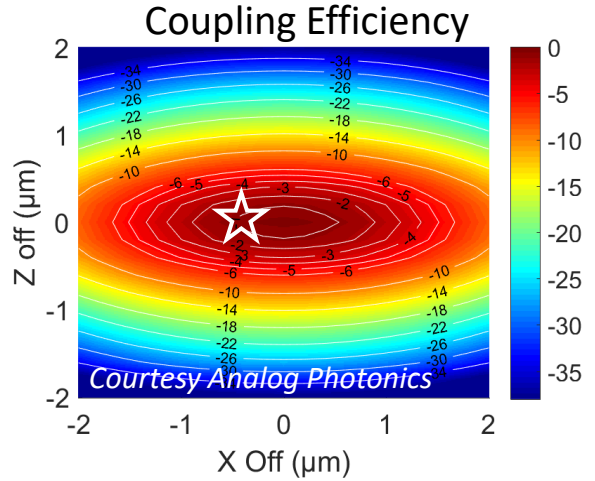
Horizontal Alignment – Die Bond Tool







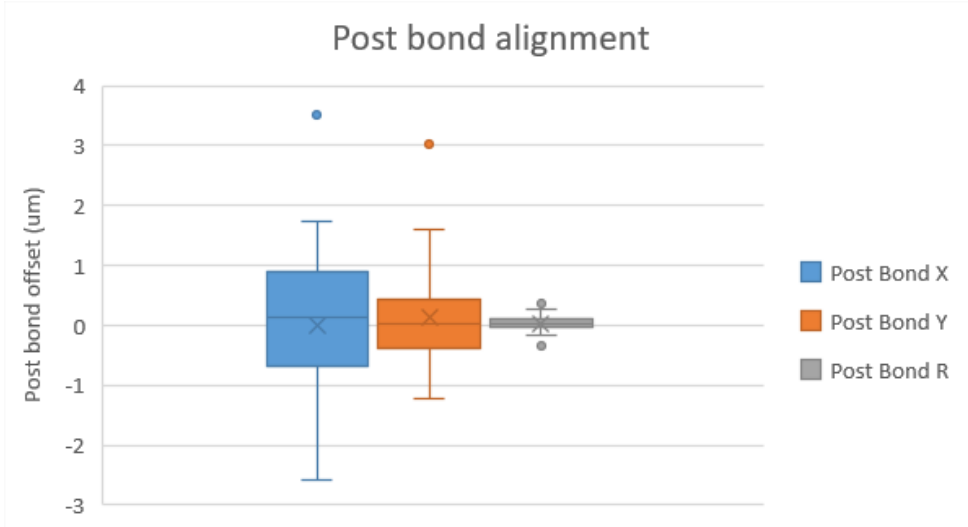
- The larger horizontal laser mode provides some tolerance to horizontal misalignment
- Horizontal (x/y) alignment is controlled by the pick and place tool (<0.5um claimed accuracy)
- Our experiments show cold placement meets tool spec, but after heating and solder reflow alignment accuracy increases to 1um
- Further study required to understand root cause of laser shift during heating



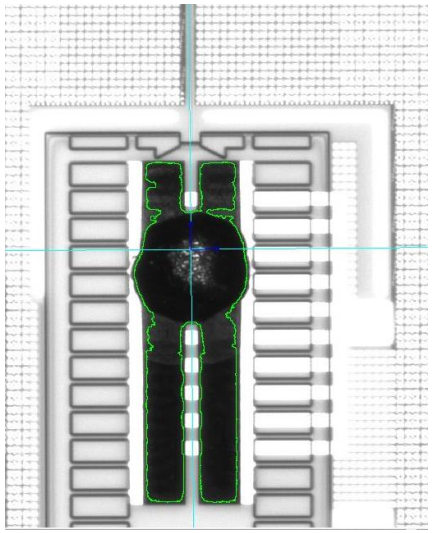
Heterogeneous Laser Integration: Solder Paste Stamping

Solder Stamping Alignment

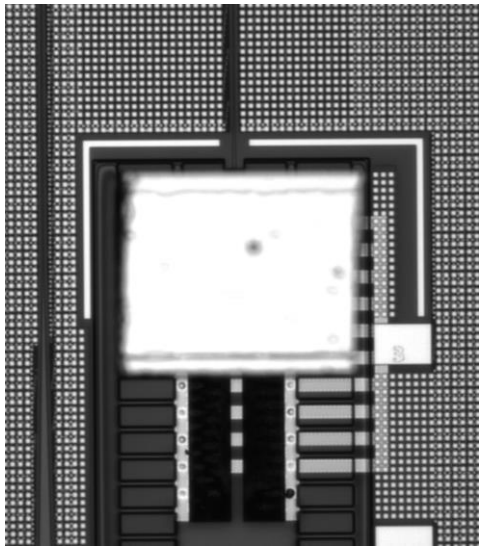
- Solder stamping system successful for 4 configurations of active interposer designs
- Post-bond alignment is <1um deviation in X/Y directions
- Working on improving post-bond x-alignment to <0.5um (tool spec limit)



Solder paste spot



Laser in trench



Total coupling loss @ 100mA: 1.86 dB
(optimization for process yield underway)
This is an improvement of previous coupling loss measurements of 3-4 dB
Driving toward 1dB coupling loss

Summary

Summary

- AIM Photonics has a end to end world class 300mm Silicon Photonics Accessible technology
  - The AIM Photonic Integrated Circuit (PIC) offerings: core MPW, Quantum, Sensors, and III-V.
  - Heterogeneous integration with electronic-photonic interposers, wafer to wafer bonding, hybrid bonding, and dense bumping is also available.
  - AIM Test Assembly and Packaging (TAP) specializes in electronic photonic packaging
- Datacom performance scaling is dependent on co-packaged optics
- Getting light on and off the chip currently depends on fiber attach and gratings. New, lower cost methods are being sought.
- Integration of lasers on chip by 2.5D is shown.
- Standards in electronic photonic packaging are needed to reduce costs

Summary