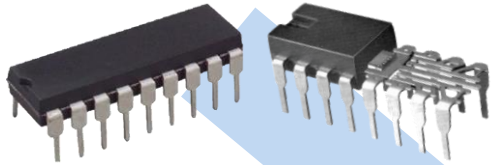
NCCAVS User Groups

ESPAT

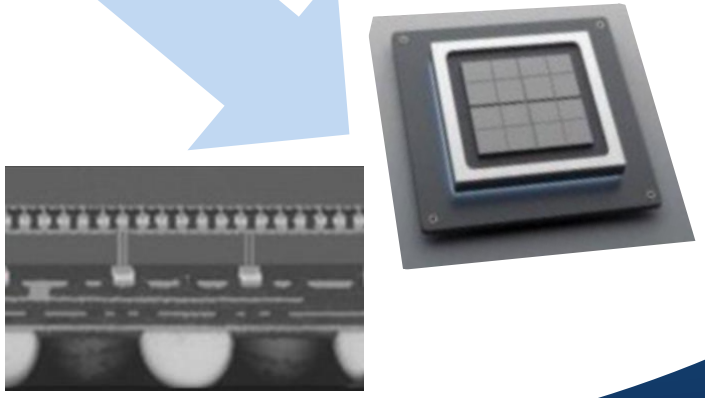
AVS Science and Technology of Materials, Interfaces, and Processing

Source: "Microcontroller PIC16F88 in DIP PTH Package,", Blue Sky Components Limited, UK



"Packaging Advances in the OSAT, Foundry, and MEMS Markets with a Highlight on Europe"

Source: "Intel FOVEROS Architecture" Packaging IFTLE 421 - July 2019, Phil Garrou (Courtesy of Intel)



JUN/29, 2022

NCCAVS Joint User Group Meeting (CMPUG, PAG, & TFUG)
"Semiconductor Packaging Outside the Mainstream" / Zoom-Meeting

NCCAVS User Groups

Science and Technology of Materials, Interfaces, and Processing

NCCAVS Joint User Group Meeting
June 29th, 2022

AGENDA

1) Introduction ESPAT-Consulting
2) Semiconductor Packaging Evolution
3) Semiconductor Market and Ecosystem
4) Current Supply Chain Situation
5) Semiconductor Packaging Market
6) Highlight on Packaging in Europe
7) Trends in Advanced Packaging

1) Introduction ESPAT-Consulting

Vision Statement ("What")

To enhance and strengthen the European Semiconductor Eco-System by supporting the growth of Advanced Packaging and Test development and manufacturing.

Source: Advidera GmbH & Co. KG – Website Blog, 2022

Mission Statement ("How")

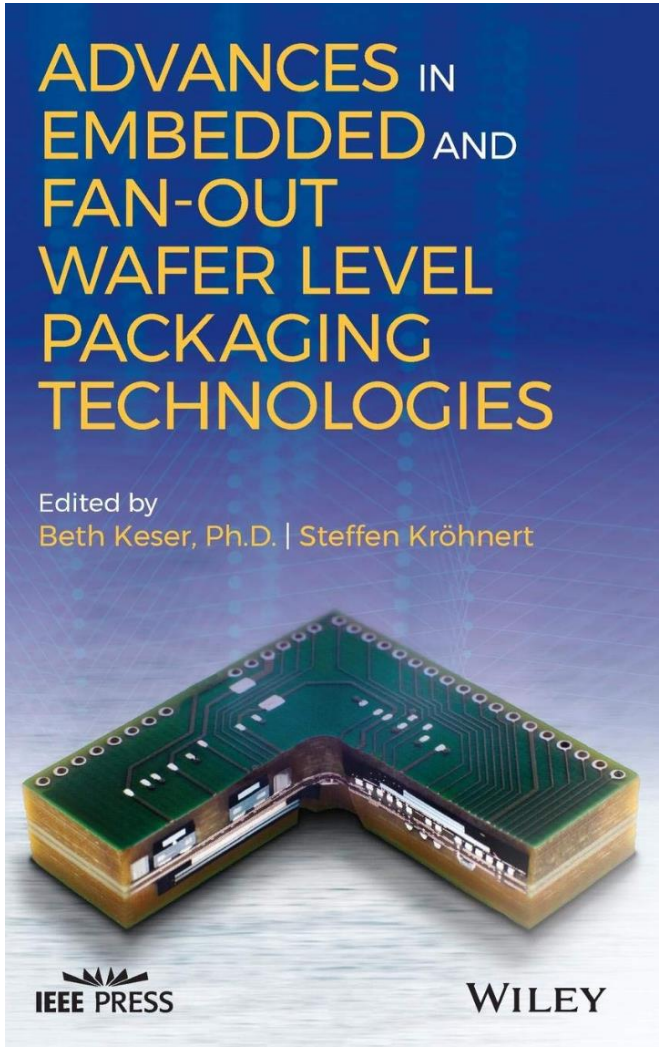
To be the knowledgeable, trusted and well-connected problem solver and influencer for Advanced Packaging, and Test in Europe; highlighting the importance of Semiconductor package design, assembly, interconnect, packaging, and test as integral part of the Semiconductor Supply, and Value Chain; promoting the need for co-design, and co-development; being the partner of choice for authorities, and decision makers, research institutes, manufacturers, and innovators in the field, and their customers; building bridges, and bringing them together in order to develop leading-edge solutions, increase their business, and grow together.

This includes but is not exclusively intense networking, packaging technology scouting, roadmapping, strategic advice, and alignment, opportunity identification, initiation of co-operations, promoting, lobbying, and training in the field of Advanced Packaging, and Test.

Background

Chemnitz	Hatfield (UK) Reutlingen	Regensburg	Dresden	Porto		Dresden/Porto		Dresden			- LOCATION -
1991	1997	1999	2002	2006	2010	2012	2017	2018	2019	2020+	- YEAR -

Recommended Reading by the Co-Editor



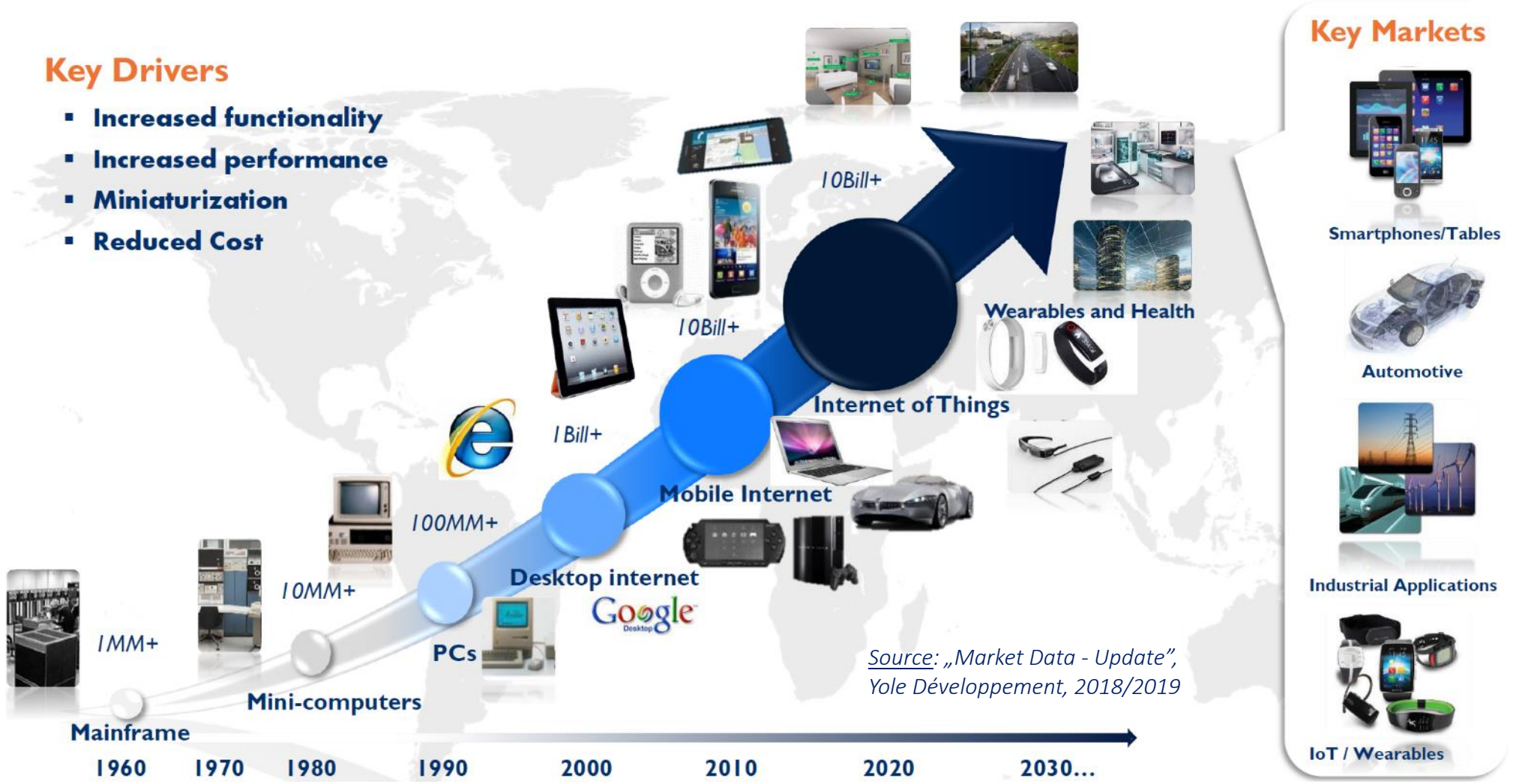
Published February 2019

Published December 2021

Stay tuned for more to come in 2023/2024

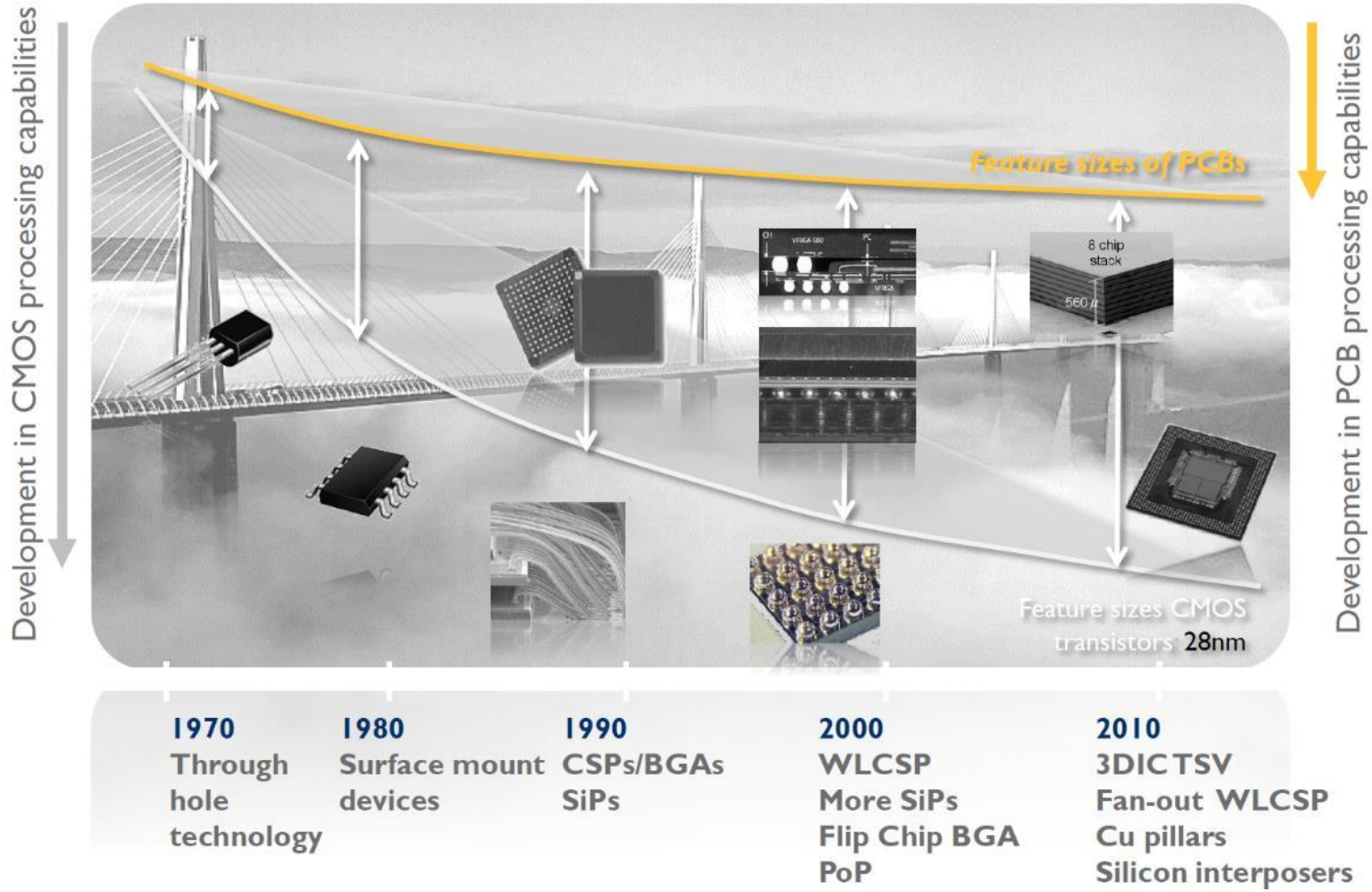
2) Semiconductor Packaging Evolution

Computing Trends + Today's Key Markets & Drivers



Source: „Market Data - Update", Yole Développement, 2018/2019

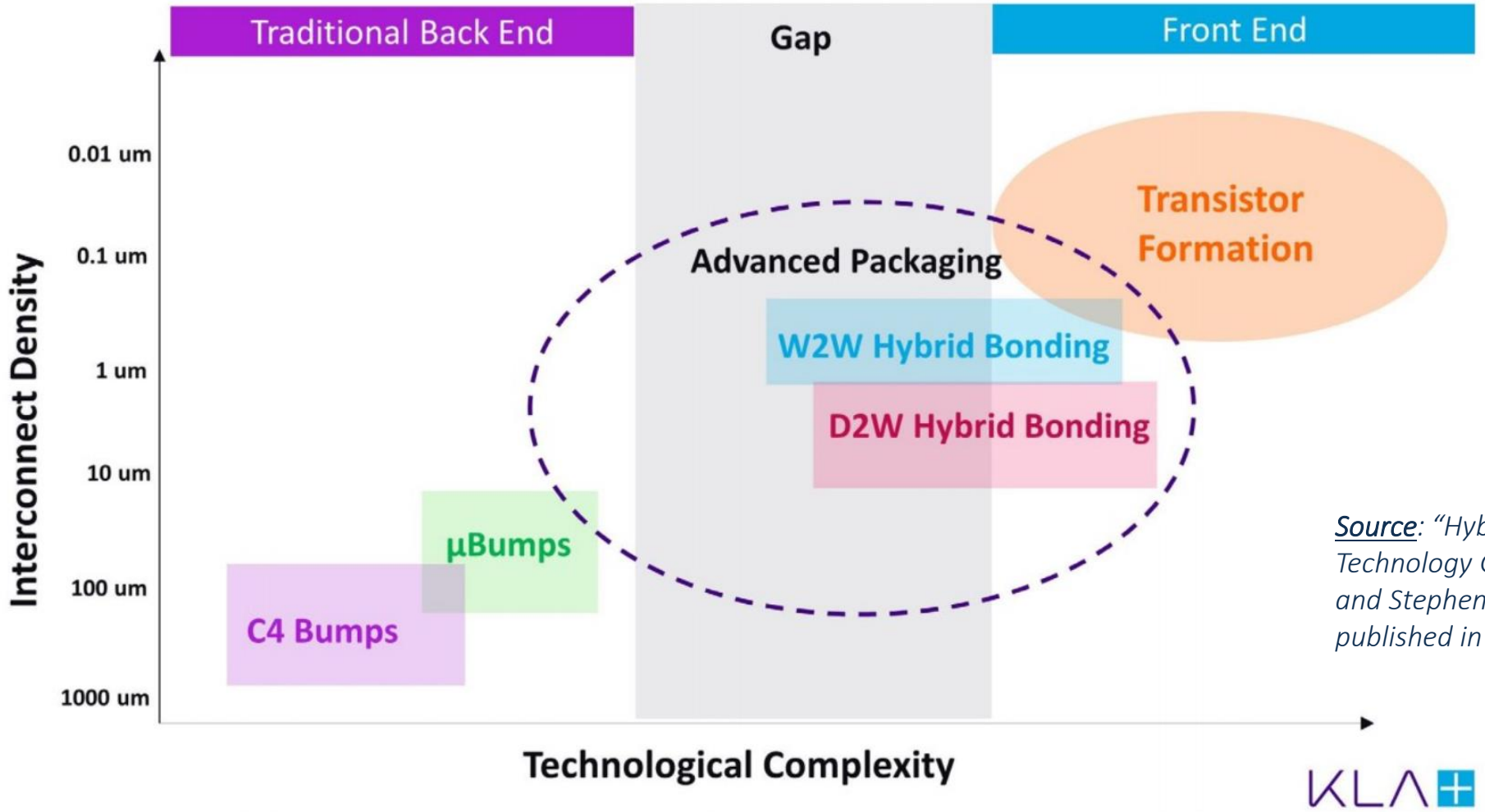
The Evolution of Semiconductor Packaging



- Packaging fills the gap in between ICs and PCBs
- Different speeds of improvement between CMOS and PCB features

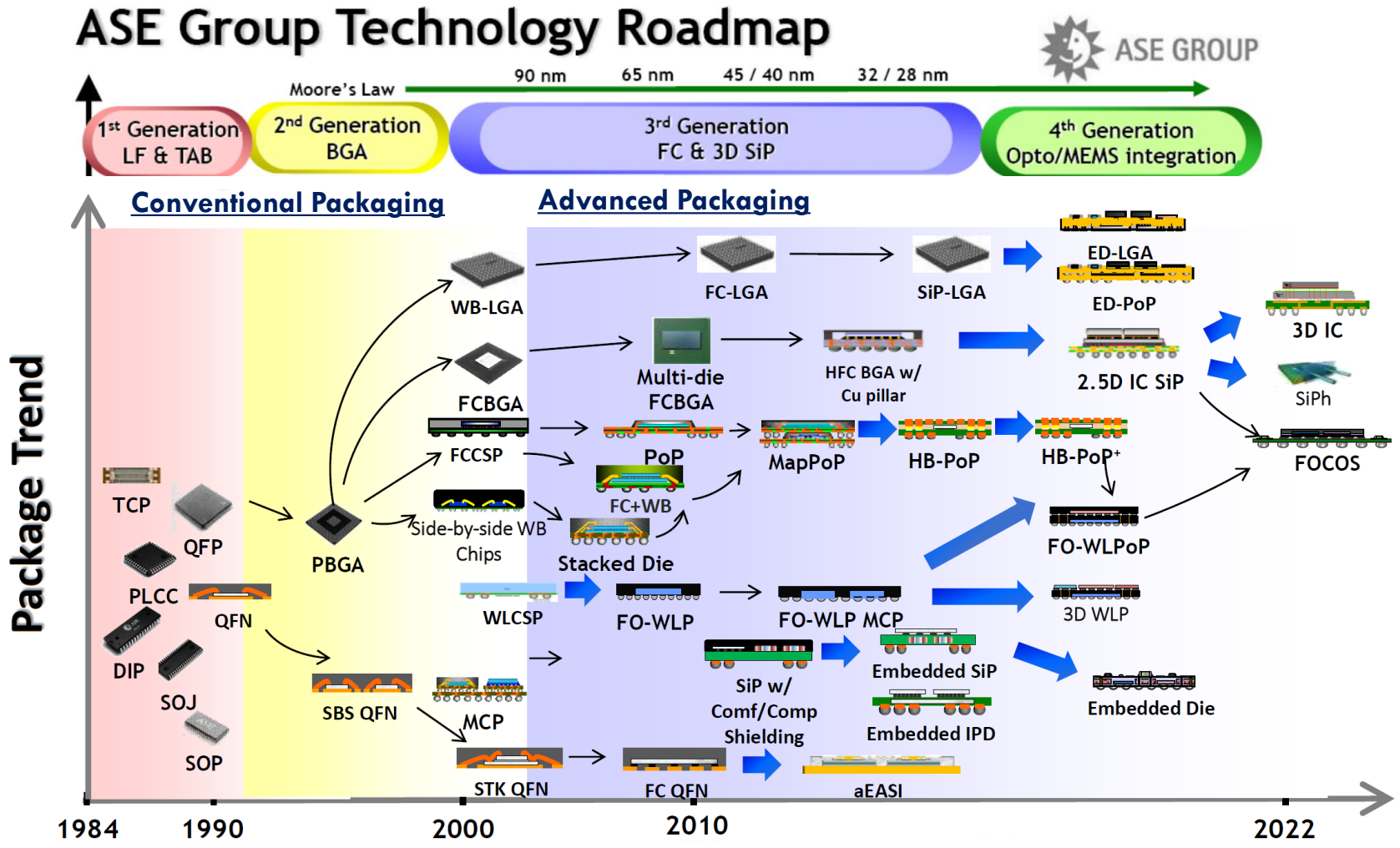
Source: „Market Data - Update", Yole Développement, 2018/2019

Technology Gap between Traditional BE and FE



Source: "Hybrid Bonding Bridges the Technology Gap", Swati Ramanathan and Stephen Hiebert, KLA Corporation, published in 3D InCites 2021 Yearbook

Packaging Roadmap of Leading OSAT Company



Source: "ASE & Jisso,presented by FhG IZM "Next Generation of electronic systems: Challenges and Solutions for Microelectronic Packaging", 2010

Marketing and Technology Promotion ASE Group (ESPAT-Consulting, received from ASE Group on request FEB/24, 2021)

The Role of Packaging is Changing

Finally, The Industry Recognizes the Importance of Packaging

- **Economic advantage of silicon scaling is gone**
  - High cost of moving to next silicon node
  - High cost of fabrication includes design, mask, and fab process
  - Only a limited number of foundries can afford to participate for the limited number of companies at advanced nodes
- **Heterogeneous integration provides an opportunity to achieve economic advantages lost with end of pure silicon scaling**
  - Many options for the package including silicon interposers, FO on substrate, chiplets, and variations of 3D stacking
- **Heterogeneous integration (especially chiplets) offers improved SI, PI, lower inductance and thermal resistance, form factor advantages**
- **Co-design of silicon and package essential**

Source: „Outlook for 2021: Are There Supply Limitations to Growth?“ TechSearch International, Jan Vardaman, MEPTEC Semiconductor Industry Speaker Series, 13.01.2021

NCCAVS User Groups

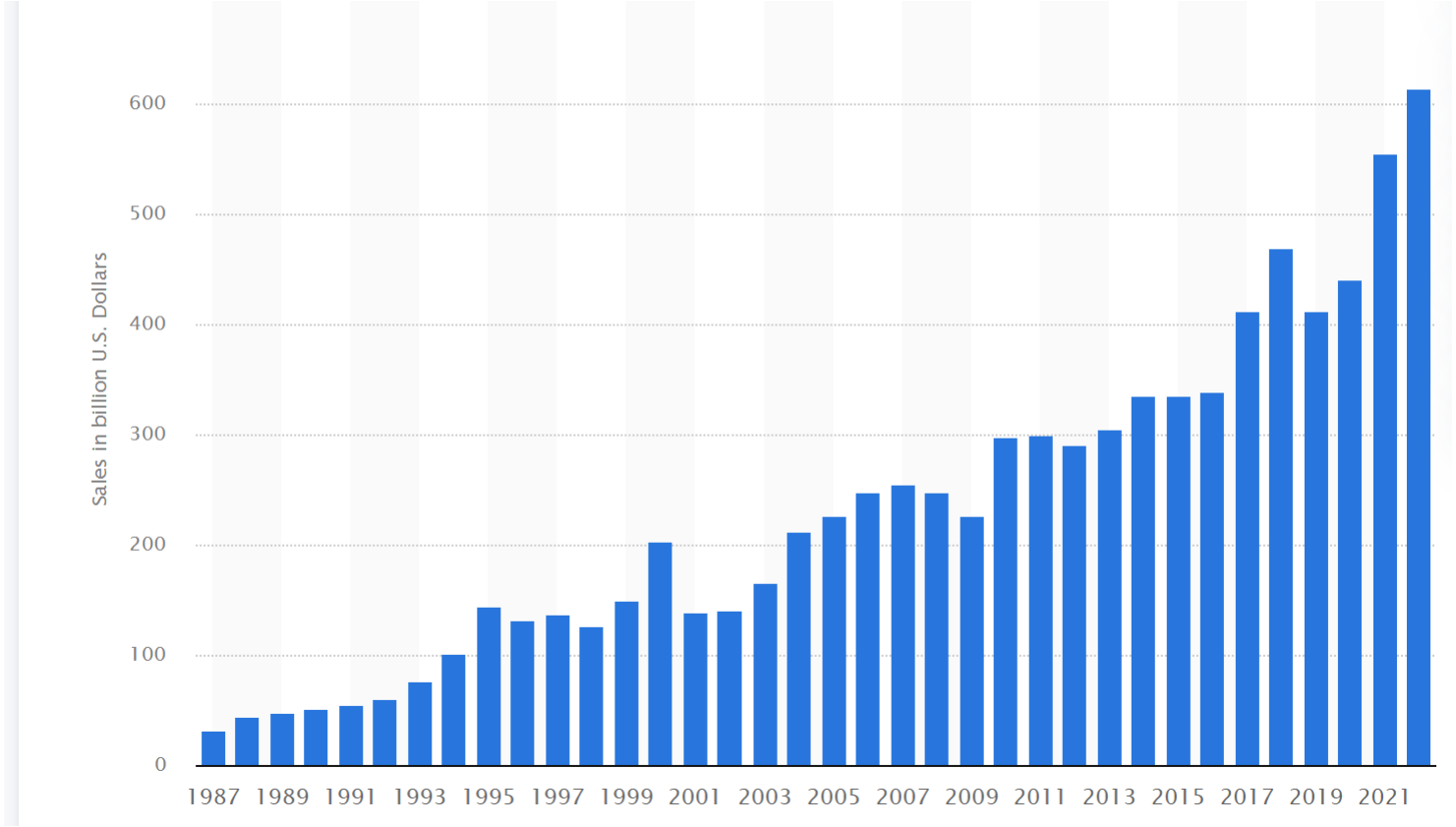
Science and Technology of Materials, Interfaces, and Processing

NCCAVS Joint User Group Meeting
June 29th, 2022

3) Semiconductor Market and Ecosystem

Global Semiconductor Market

After 2 successive high growth years, global semiconductor market growth decline 12% YoY to reach ~$412B in 2019. The decline is attributed to the cyclicality in product pricing, sluggish phone demand and global trade unrest.



$440 B in 2020
$556 B in 2021 (all time high)
$613 B in 2022 (forecast)

Source: „Semiconductor market size worldwide from 1987 to 2022", Statista Website 06/2022

Growth 2020 +5.1% ($433B) and 2021 +8.4% ($470B)

- Almost all major product categories contribute

  Memory **+12.2%/+13.3%**
  Sensors +7.4%/ +7.8%
  Logic +6.5%/ +7.1%

- Regional ranking

  America **+18.7%/+9.5%**
  Asia Pac +3.8%/+8.7%
  Japan -0.6%/+5.8%
  Europe -8.4%/+5.7%

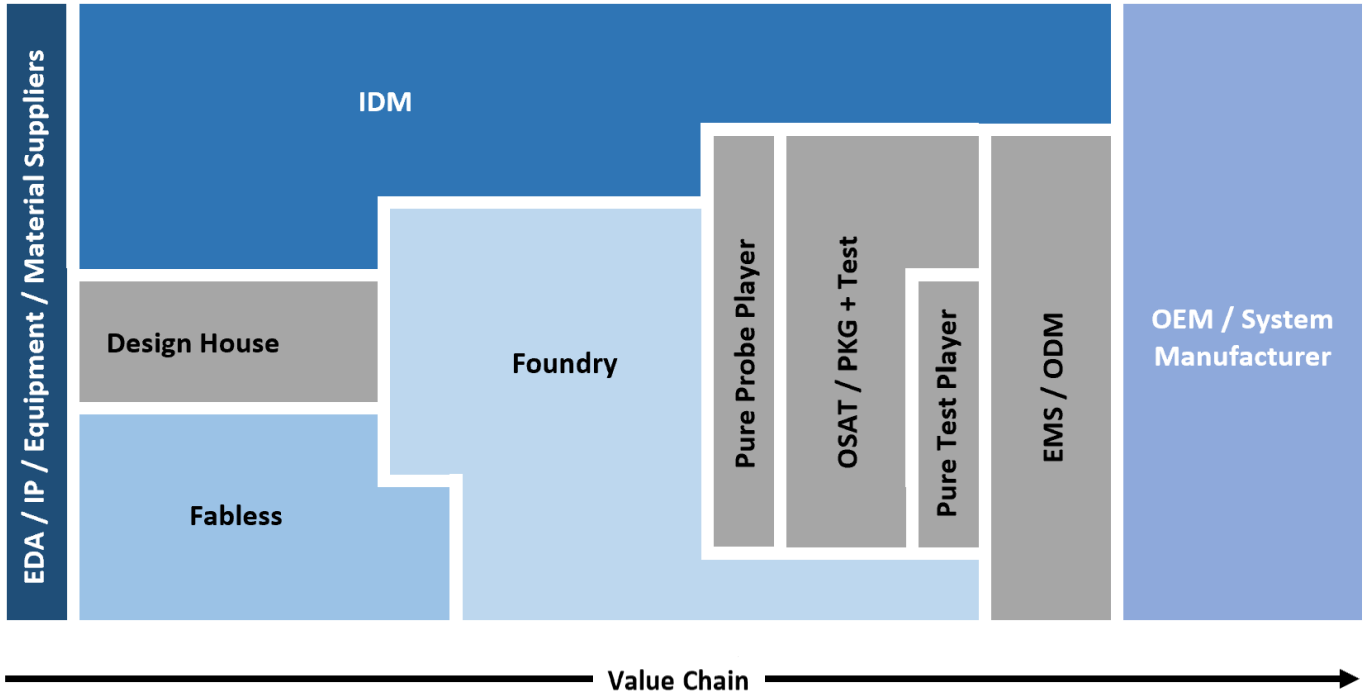
Fall 2020	Amounts in US$M			Year on Year Growth in %		
	2019	2020	2021	2019	2020	2021
Americas	78,619	**93,343**	**102,164**	-23.7	18.7	9.5
Europe	39,816	**36,452**	**38,543**	-7.3	-8.4	5.7
Japan	35,993	**35,759**	**37,841**	-9.9	-0.6	5.8
Asia Pacific	257,879	**267,590**	**290,854**	-8.8	3.8	8.7
Total World - $M	412,307	**433,145**	**469,403**	-12.0	5.1	8.4
Discrete Semiconductors	23,881	**23,593**	**25,292**	-0.9	-1.2	7.2
Optoelectronics	41,561	**40,481**	**44,628**	9.3	-2.6	10.2
Sensors	13,511	**14,515**	**15,642**	1.2	7.4	7.8
Integrated Circuits	333,354	**354,556**	**383,840**	-15.2	6.4	8.3
Analog	53,939	53,954	58,578	-8.2	0.0	8.6
Micro	66,440	67,744	68,444	-1.2	2.0	1.0
Logic	106,535	113,419	121,507	-2.5	6.5	7.1
Memory	106,440	119,440	135,311	-32.6	12.2	13.3
Total Products - $M	412,307	**433,145**	**469,403**	-12.0	5.1	8.4

Note: Numbers in the table are rounded to whole millions of dollars, which may cause totals by region and totals by product group to differ slightly.

Source: WSTS (World Semiconductor Trade Statistics), Article in „Markt & Technik" 1-3/2021 (22.01.2021) pp. 16-17

Semiconductor Eco-System

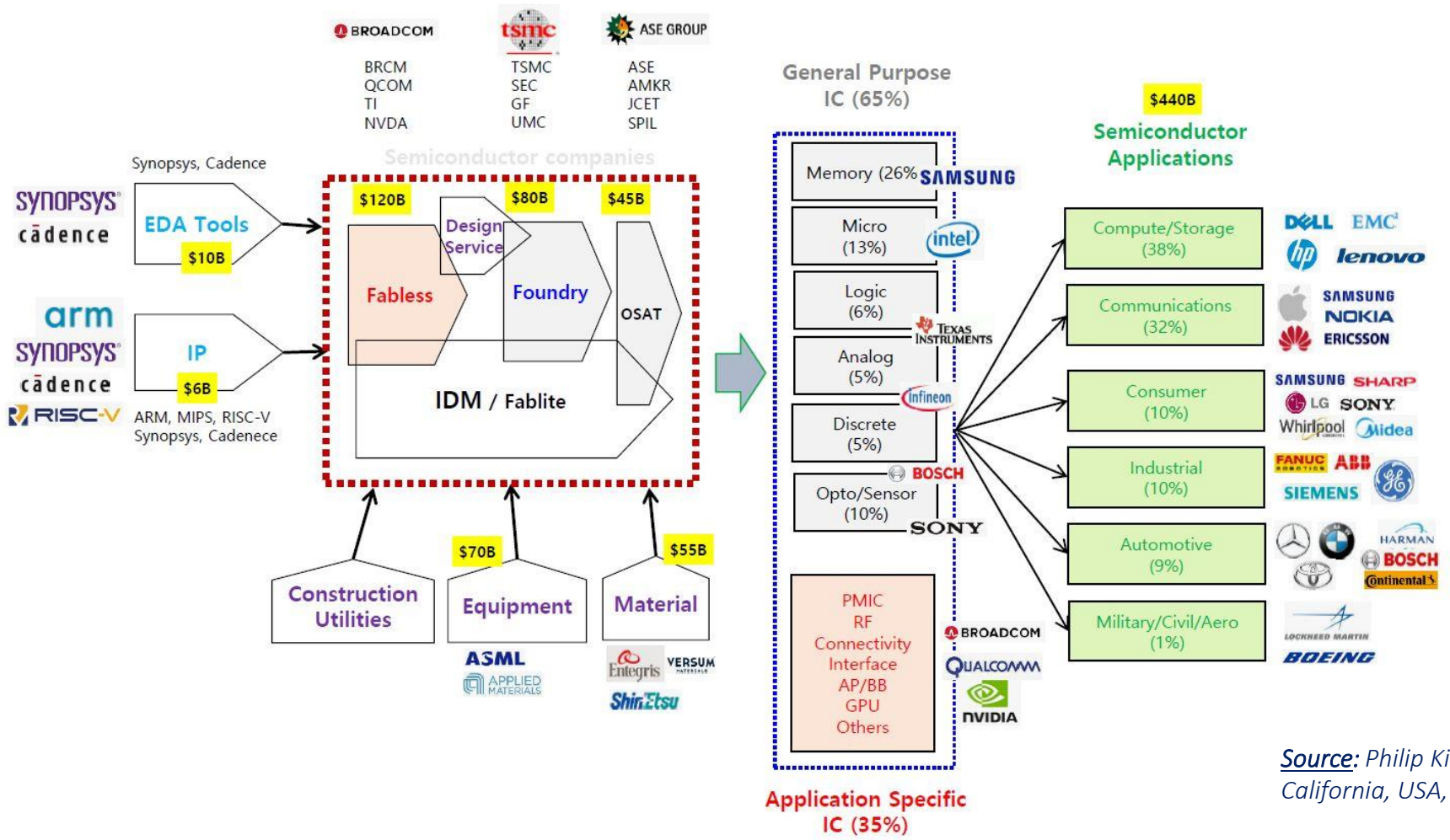
Business Models in the Value Chain / Product Development Flow



EDA – Electronic Design Automation
IDM – Integrated Device Manufacturer
OSAT – Outsourced Semiconductor Assembly and Test
EMS – Electronics Manufacturing Services
ODM – Original Design Manufacturer
OEM – Original Equipment Manufacturer

Semiconductor Eco-System

Business Models in the Value Chain

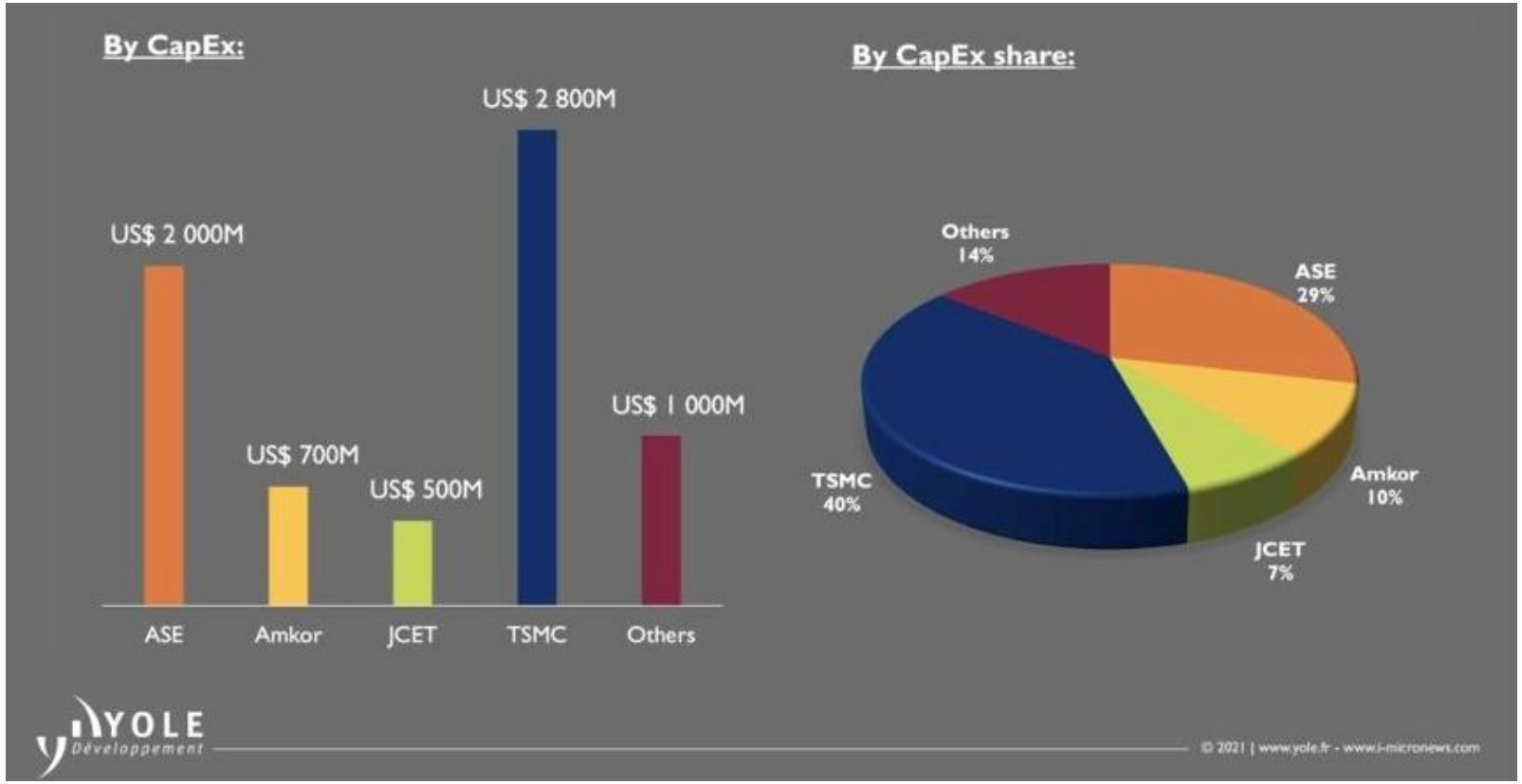


The global semiconductor market size was $433 billion in 2020.

Source: Philip Kim, CEO at IBG Construction, Inc., California, USA, LinkedIn Post, MAY/24, 2021

Global Packaging Market and Shares

Unprecedented CAPEX Investment in 2021



In the race for Heterogeneous Integration, key players, such as ASE (w/ SPIL & USI), TSMC, Intel, Amkor, and JCET have announced unprecedented CAPEX investment in 2021.

Driven by a pandemic boom, the Semiconductor Industry continues to see robust demand driven by the work-from-home ethic and increased demand for automotive and datacenter.

FY 2021 is shaping up to become a "Banner Year" for key OSATs and IDMs/Foundries such as TSMC.

Source: Advanced Packaging Quarterly Market Monitor, Q1/2021, Yole Développement

4) Current Supply Chain Situation

Market Overview – Current Supply Chain Situation

Supply Crunch means longer wait time for components (lead time)

Category	Currently	Normally
Power management chips	24-52 weeks	4-8 weeks
Microcontroller chips	24-52 weeks	4-8 weeks
CPUs *(Central processing units)*	12-16 weeks	4-8 weeks
Memory chips	14-15 weeks	4-8 weeks
Wi-Fi chips	24-30 weeks	4-8 weeks
Consumer LCD screens	16-20 weeks	12 weeks
Substrate materials	52 weeks	20 weeks
Chip packaging services	12 weeks	2-4 weeks

Source: Nikkei Asia - Analysis of Companies' Data, May 2021

Market Overview – Current Supply Chain Situation

Advanced Packaging System-in-Package

- The current global supply chain situation, its advantages, disadvantages, and the challenges are well summarized, for instance, in a recent article published by the Boston Consulting Group *):

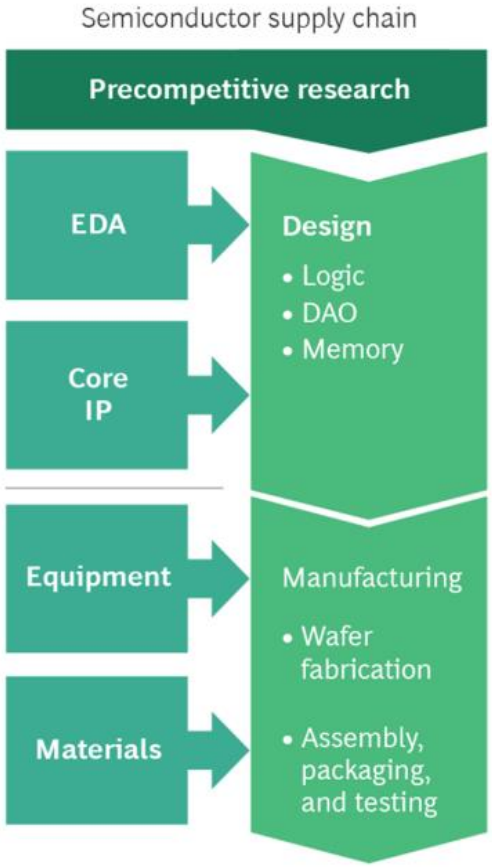
  > "The widespread shortage of semiconductors that began in late 2020 highlighted how indispensable these specialized components are in today's economy. Semiconductors are used to power a vast array of electronic devices - everything from smartphones and cloud servers to modern cars, industrial automation, and critical infrastructure and defense systems.
  >
  > **The global structure of the semiconductor supply chain, developed over the past three decades, has enabled the industry to deliver continual leaps in cost savings and performance enhancements that ultimately made possible the explosion in information technology and digital services.**

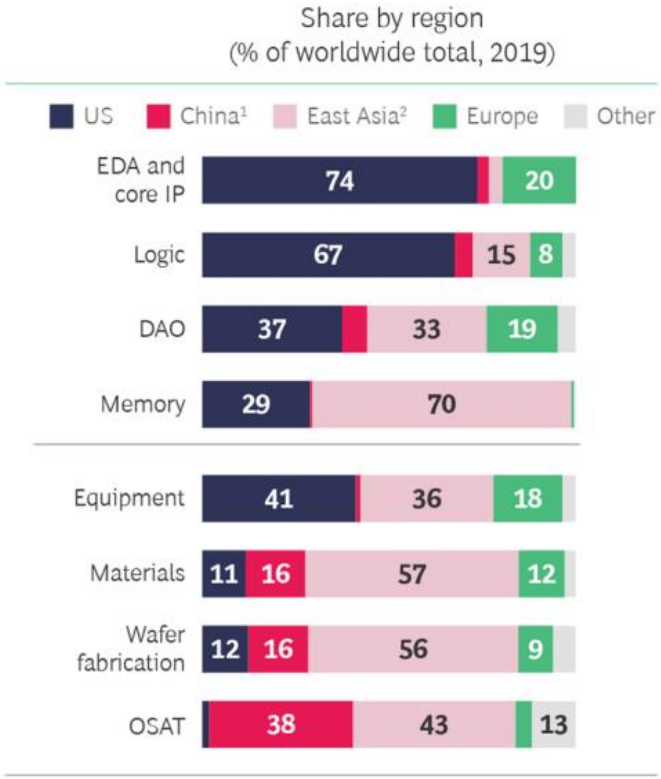
- In the past few years, however, several new factors have emerged that could put the successful continuation of this global model at risk. Addressing these vulnerabilities requires a combination of carefully designed actions from policymakers, including targeted incentives to encourage domestic production in order to address strategic gaps."

*) Source: "Strengthening the Global Semiconductor Supply Chain in an Uncertain Era", Varas, Antonio; Varadarajan, Raj; Ramiro Palma, Jimm (Boston Consulting Group (BCG), APR/01, 2021

Market Overview – Current Supply Chain Situation

Benefits of Global Supply Chain versus Fully Localized Supply Chain





Costs avoided vs. fully localized "self-sufficient" supply chains

$0.9–1.2T
avoided upfront investment

$45–125B
annual cost efficiencies

35–65%
enabled reduction in semiconductor prices

DAO = Discrete, Analog, and Other (including optoelectronics and sensors);
EDA – electronic design automation);
1) Mainland China, 2) East Asia including South Korea, Japan, and Taiwan.

Source: "The Global Semiconductor Supply Chain based on Geographic Specialization"
(Source: BCG analysis / 2019)

NCCAVS User Groups

Science and Technology of Materials, Interfaces, and Processing

NCCAVS Joint User Group Meeting
June 29th, 2022

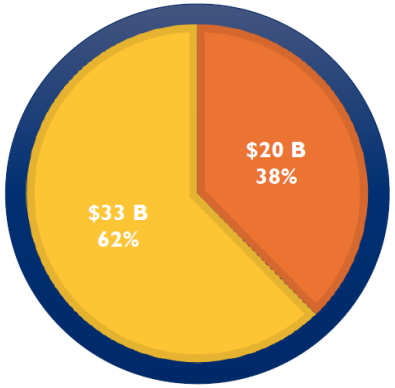
5) Semiconductor Packaging Market

Global Packaging Market and Shares

Growth in both sectors: Traditional and Advanced Packaging

2014

$53 B



Global Packaging

CAGR 4%

Advanced Packaging

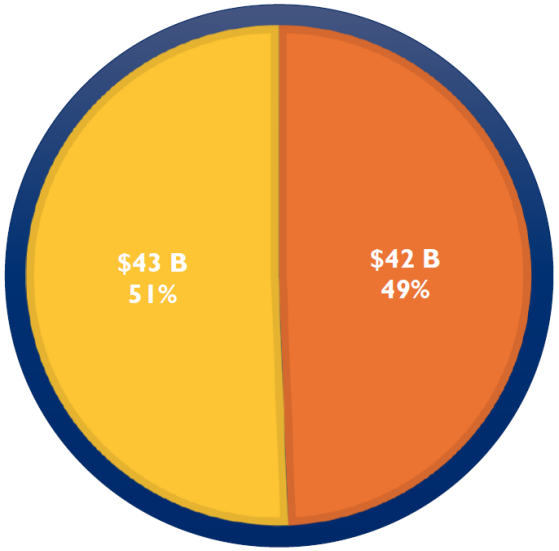
CAGR 7%

Conventional Packaging

CAGR 2%

2025

$84 B - (New Data: > $100 B)

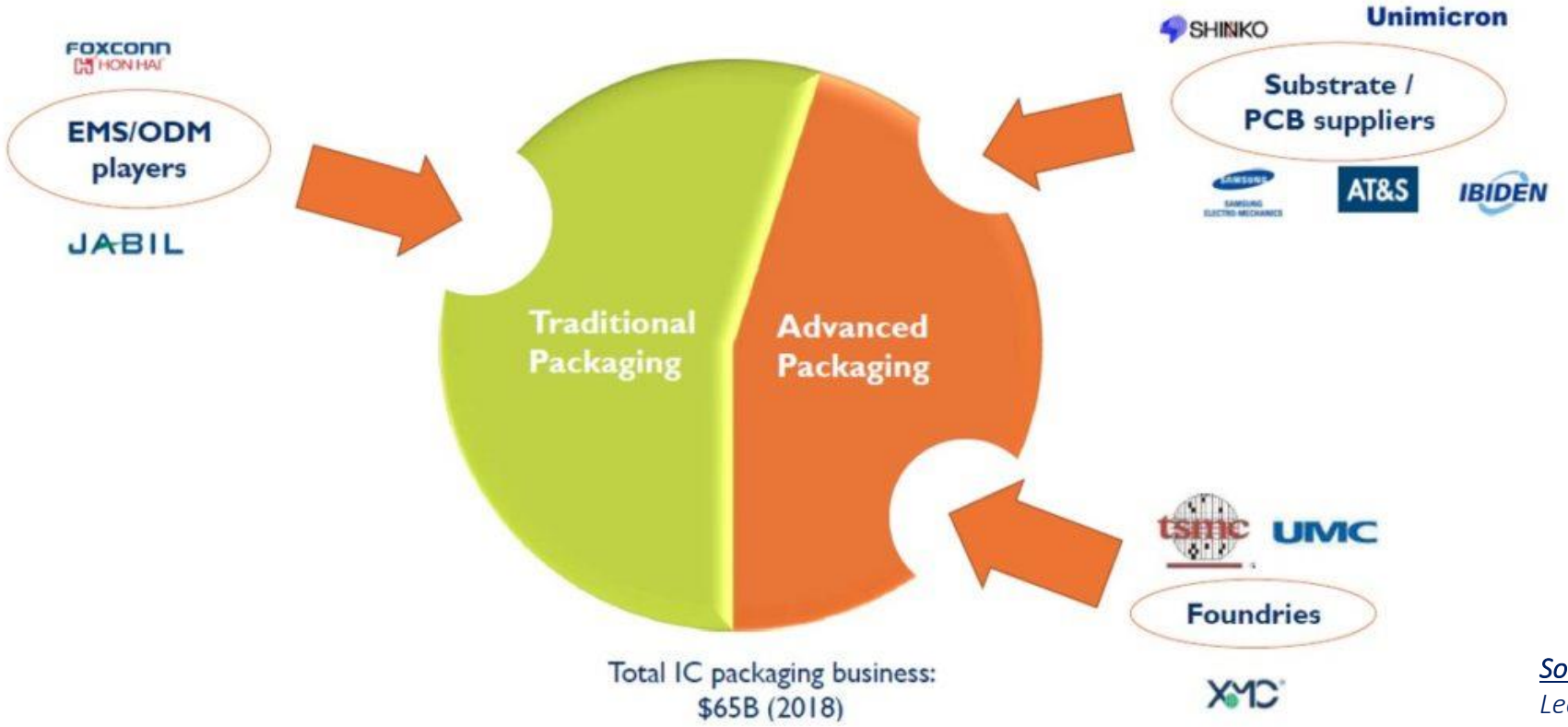


Advanced Packaging Platform	Revenues CAGR 2019 – 2025
3D Stacking	21,3%
Flip-Chip	5,1%
Fan-Out	15,9%
Fan-In	3,2%
Embedded Die	18,1%

Source: "Trends in Advanced Packaging and transition towards Heterogeneous Integration", Yole Developpement, Advanced Packaging Forum @ SEMI Technology Unites Global Summit, FEB/16, 2021

Global Packaging Market and Shares

Growth in both sectors: Conventional and Advanced Packaging



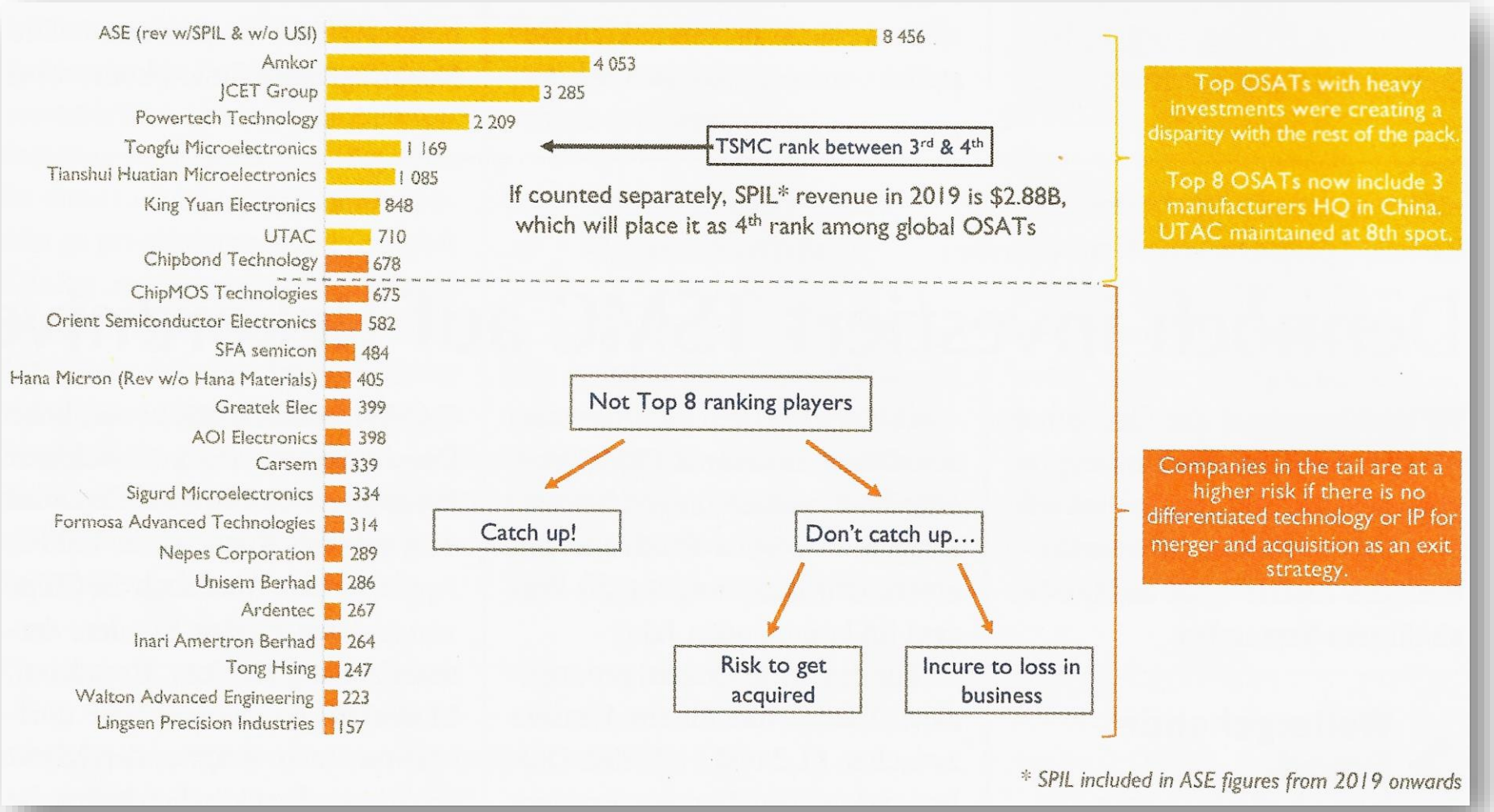
Packaging is a very competitive market

Trend:
Foundries, IDM, EMS, ODM, IC-Substrate and PCB Suppliers are taking more and new shares of the AdvPkg market from the OSATs

Source: IFTLE 451: Advanced Packaging is Leading Electronics into the 2020s, 3DInCites Blogs, Packaging IFTLE by Phil Garrou, JUN/01, 2020

Independent Packaging Players Worldwide

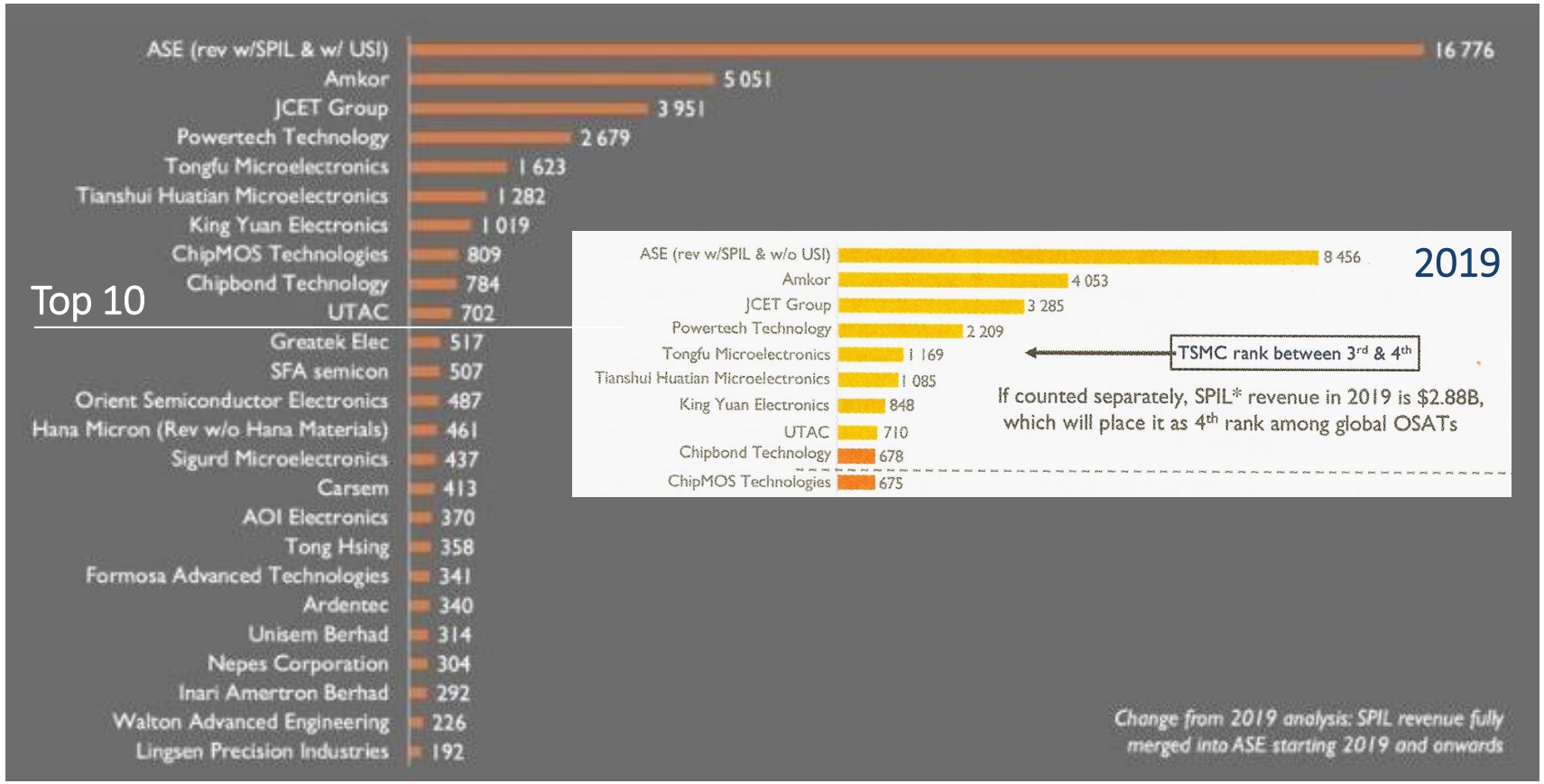
Leading OSATs in 2019 with Revenues in Mio$ - **No European Company**



Source: „Advanced Packaging - Fast Growth, Chances for Foundries and IDMs", Heinz Arnold, Markt & Technik Magazin, 32/2020, AUG/07, 2020

Independent Packaging Players Worldwide

Leading OSATs in 2020 with Revenues in Mio$ - **No European Company**



Top 25 OSAT ranking 2020 Revenues

The Semiconductor Industry in 2020 was resilient and experienced strong growth as the top OSATs, showed unprecedented growth in Q4/2020 and, in fact, throughout 2020 as the global pandemic took shape. Many OSAT, IDM & OEM experienced **15-20% growth in revenue and increased gross margins compared to 2019**.

Source: Advanced Packaging Quarterly Market Monitor, Q1/2021, Yole Développement

NCCAVS User Groups

Science and Technology of Materials, Interfaces, and Processing

NCCAVS Joint User Group Meeting
June 29th, 2022

6) Highlight on Packaging in Europe

Overview European OSAT Landscape

Based on “Worldwide OSAT Manufacturing Sites Database, 2019 Edition”

Key Highlights

Tracking advances in packaging technology, which directly affects chip performance, reliability, and cost, requires the understanding of company offerings by location. Key features of the updated report include:

- 2019 edition includes over 30 new facility additions compared to 2018 report
- The world's Top 20 OSAT companies in 2017 and 2018
- More than 120 companies and up to 360 facilities
- Over 200 facilities with Test capabilities
- Over 90 facilities offering leadframe CSP
- Over 50 bumping facilities, including over 30 with 300mm wafer bumping capacity
- More than 50 facilities offering WLCSP technology
- New facilities offering FOWLP and FOPLP
- Over 100 facilities in China, around 100 in Taiwan, and 43 in Southeast Asia

96%

Companies and facilities outside Europe

Overview European OSAT Landscape

Based on “Worldwide OSAT Manufacturing Sites Database, 2019 Edition”

Worldwide OSAT Manufacturing Sites Database, updated October 2019

Region: Europe

Capabilities

Status: 3-4 years

	Company Name	Ownership	Ownership HQ	Plant Site	Approximate Facility Area (I	City	State/ Province/ Prefecture	Country	Region	abilities						
										WLP	TSV	Modules/SiP/MCP	MEMS/ Sensors	CMOS Image Sensors/Opt	Specialization	Date Last Updated
1								Israel	EUR							
2																
3																
4																
5																
6																
7																
8																
9																
10																
11																
12																
13																
14																
15																
16																

The Database includes for Europe: ∑ 15 Companies / 16 Facilities

→ Ongoing study: Currently 74 companies/facilities with OSAT/PAT-SP character/profile identified
(62 w/o facilities in UK, and 59 w/o UK and Israel)

Markets Mainly Served by European OSAT/PAT-SP

Independent companies w/o PAT in IDM, Foundry, EMS, ODM, OEM

Typically, **High-Value Markets,**
Low/Medium Volumes,
Specialized, Customized, Niches.

- Medical, Healthcare & Life Science
- Automotive & Mobility
- Industrial & Automation
- IoT, IIoT
- Telecommunication Infrastructure
- Aerospace & Aviation
- Military & Defence

- Sensors & MEMS
- Opto-electrical
- Photonics
- Hi-Rel
- High Voltage, Power

Packaging Technologies up to FlipChip (FCBGA, fcCSP)

- Rarely Transfer/ Compression Molding
- No Wafer Level Packaging (Fan-In, Fan-Out, 2.5D, 3D)

Source: ESPAT-Consulting

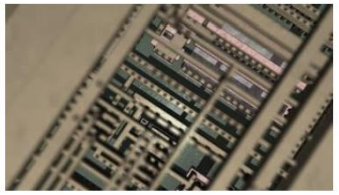
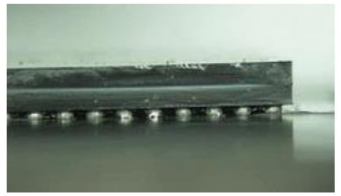
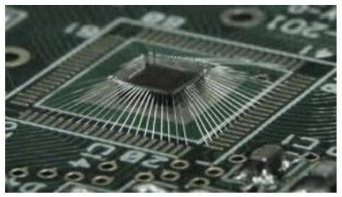
European OSAT/PAT-SP Capabilities

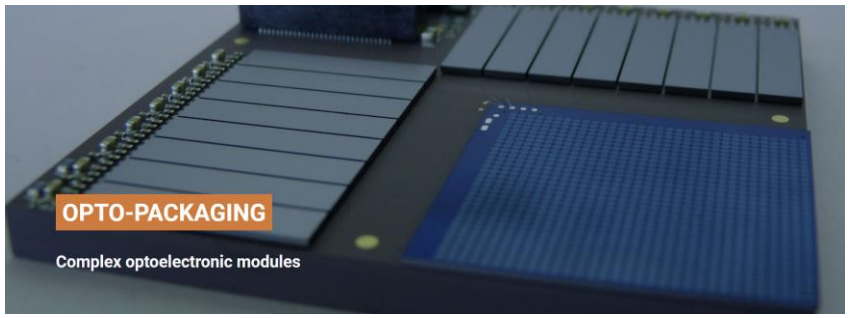
w/o PAT in IDM, Foundry, EMS, ODM, OEM

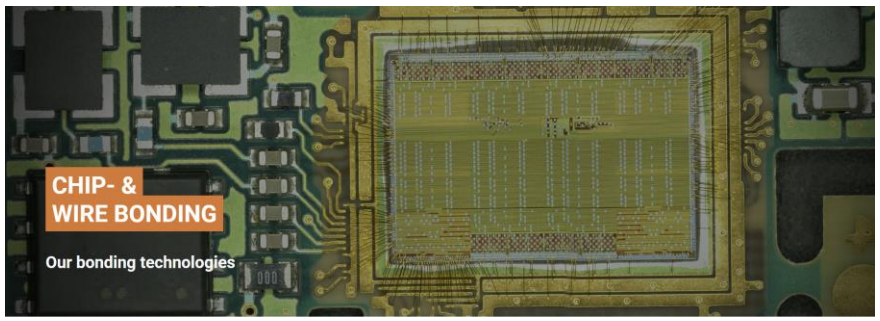
Examples

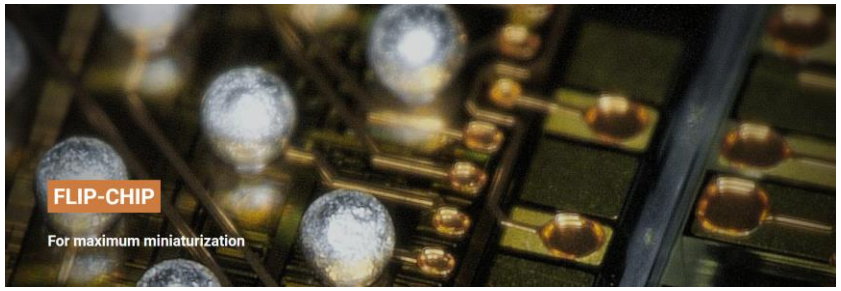
High-Value Markets
Low/Medium Volumes
Specialized, Customized, Niches

Wafer back-end	High-precision packaging & testing		Positioning, soldering, testing	Module & product assembly
UBM, balling, dicing	Flip chip	Chip on board	Surface-mount technology	Box-build







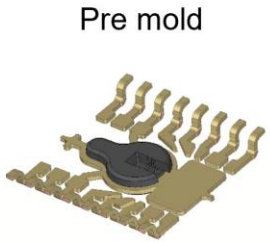
Source: AEMtec, Germany

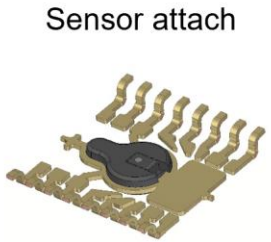
European OSAT/PAT-SP Capabilities

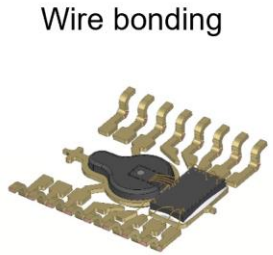
w/o PAT in IDM, Foundry, EMS, ODM, OEM

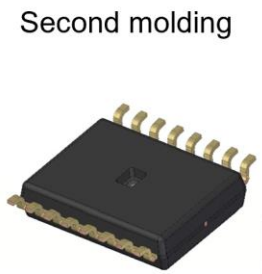
Examples

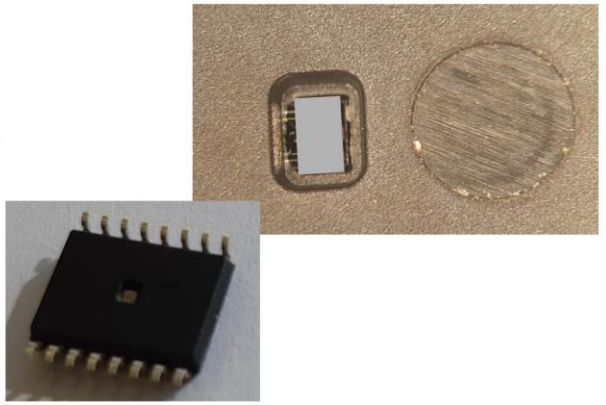
High-Value Markets
Low/Medium Volumes
Specialized, Customized, Niches

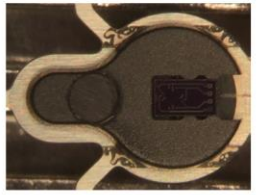


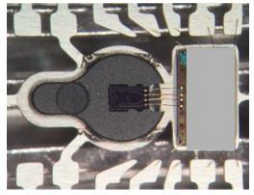


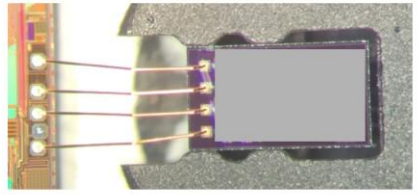






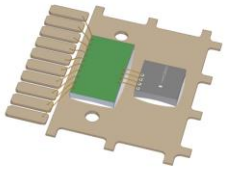


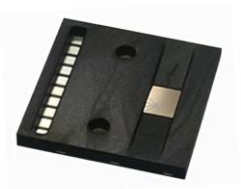




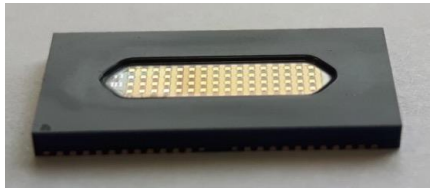
Pressure Sensor

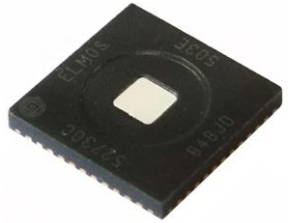
Bio-Sensors

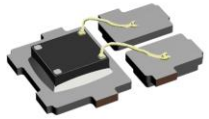


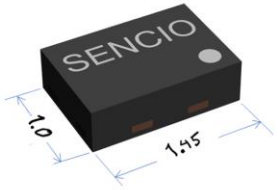


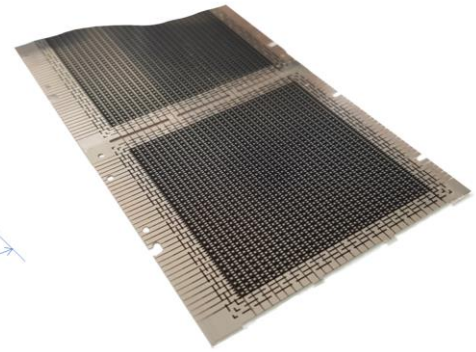
QFN Packages
Leadframe-based











Miniaturization
Leadframe-based

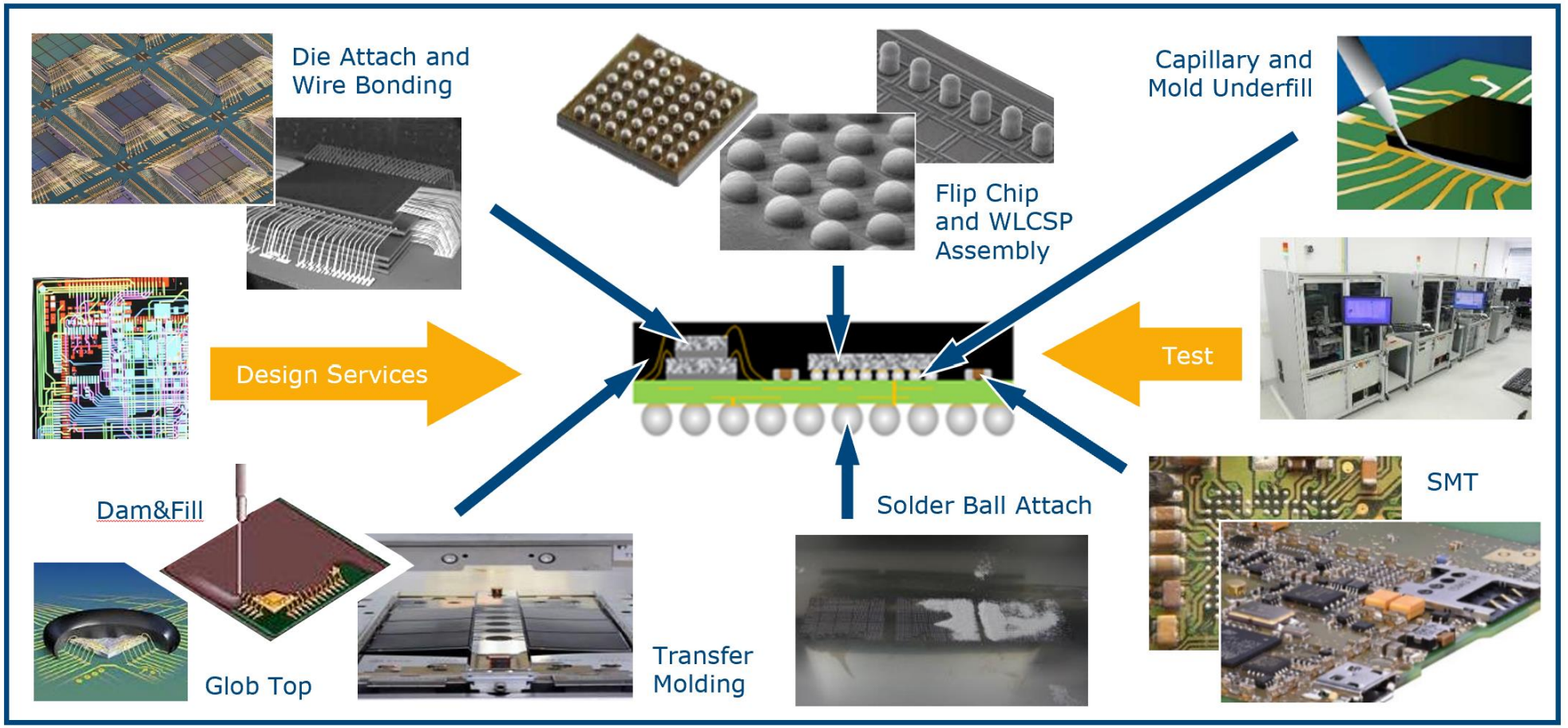
Source: Sencio, Netherlands, Functional Packaging Center

European OSAT/PAT-SP Capabilities

w/o PAT in IDM, Foundry, EMS, ODM, OEM

Examples

High-Value Markets
Low/Medium Volumes
Specialized, Customized, Niches



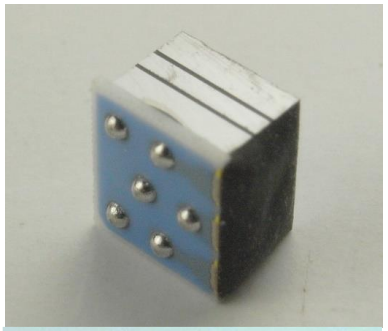
Source: MST Group, MSE, Berg, Germany, Teaser, May 2021

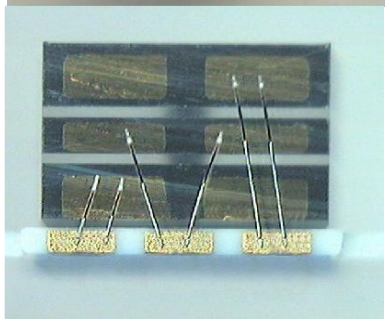
European OSAT/PAT-SP Capabilities

w/o PAT in IDM, Foundry, EMS, ODM, OEM

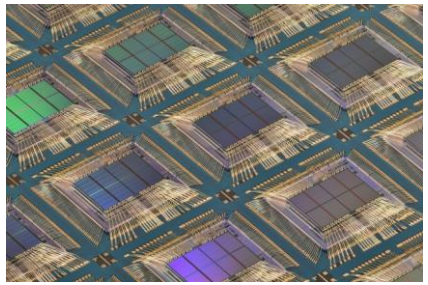
Examples

High-Value Markets
Low/Medium Volumes
Specialized, Customized, Niches

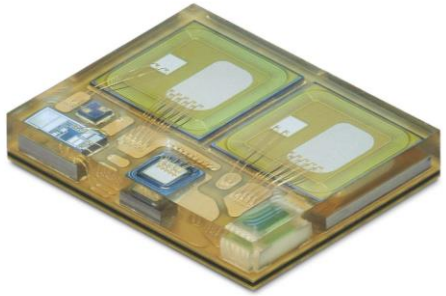




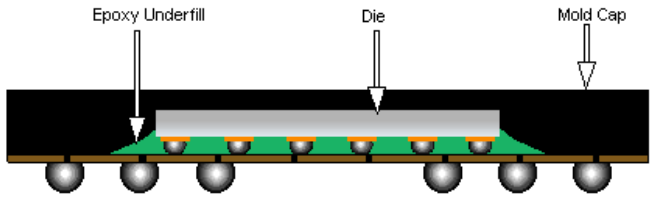
Ceramic (LTCC) Package
e.g. Accelerometer

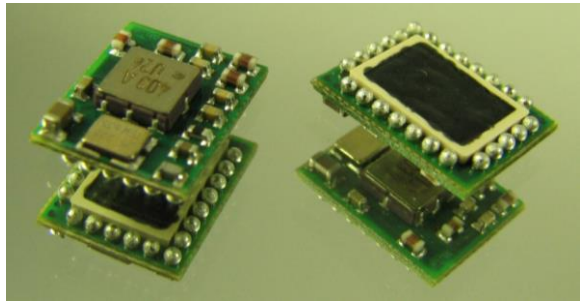


WB-BGA, LGA, Stacked Die

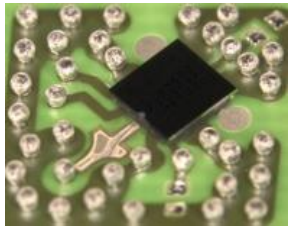


High Voltage SiP

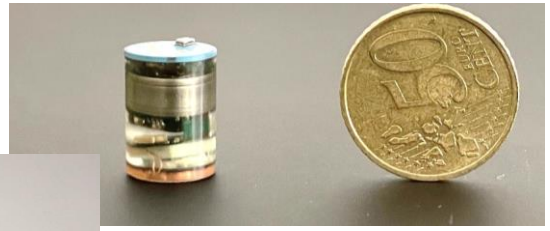


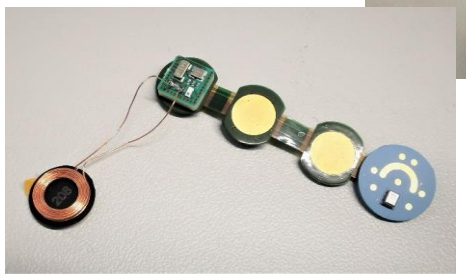


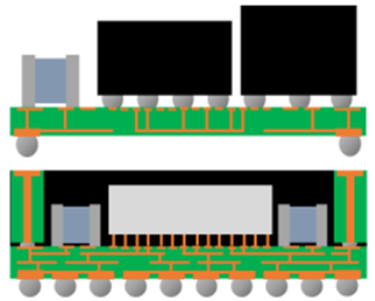
FC-SiP, FCBGA, fcCSP



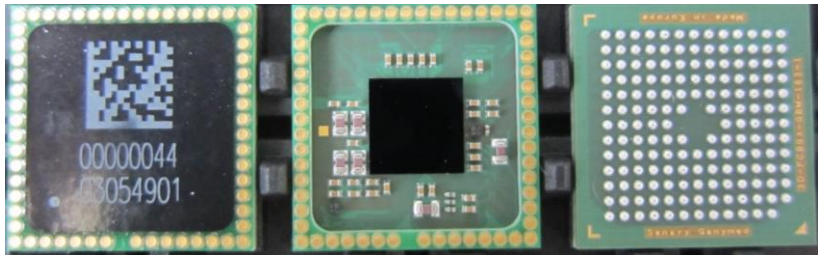
System-in-Package
Demonstrator IoT







System-in-Package
e.g. IoT-Module



Source: MST Group

Addressable Market by European OSAT/PAT-SP

Independent companies w/o PAT in IDM, Foundry, EMS, ODM, OEM

2014 - 2025

European Market Share ↗

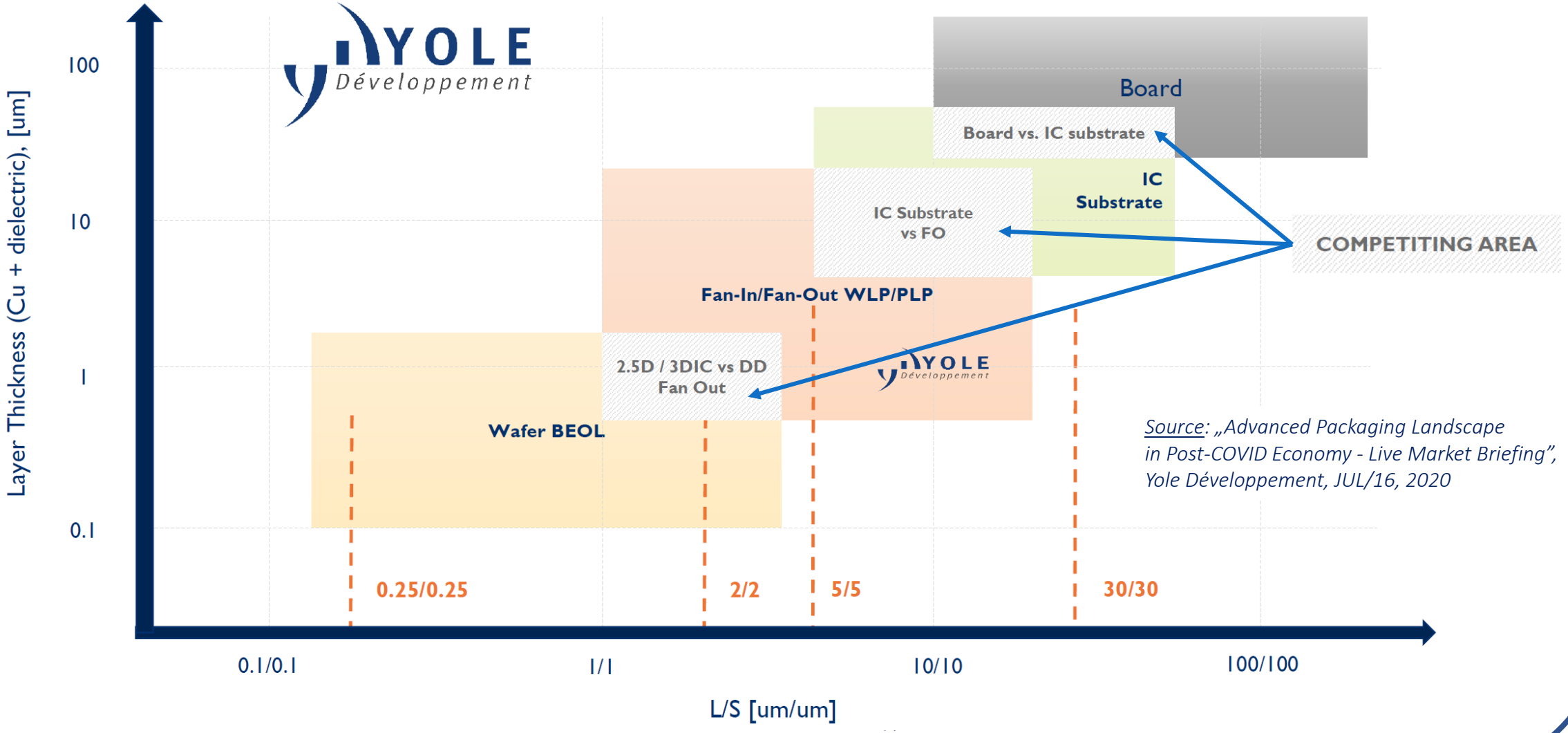
- Total Packaging Market 2021: $75 B
  → 2025: $85 B (New Data: > $100 B)
- 2021 European share estimated at 3-4 % ~ $2.62 B
- **OSAT/PAT-SP addressable ~10-20 % = $262-524 M**
- 2025 European share estimated at 4-5 % ~ $3.82 B
- **OSAT/PAT-SP addressable ~10-20 % = $382-764 M**
- Revenues of the few large European OSAT/PAT-SP
  (if not independent: 3rd party/external/OSAT business only)
  at the range of $40-60 M/year per company

Source: ESPAT-Consulting

7) Trends in Advanced Packaging

- Heterogeneous Integration
- System-in-Package
- Chiplets Assembly
- Hybrid Bonding

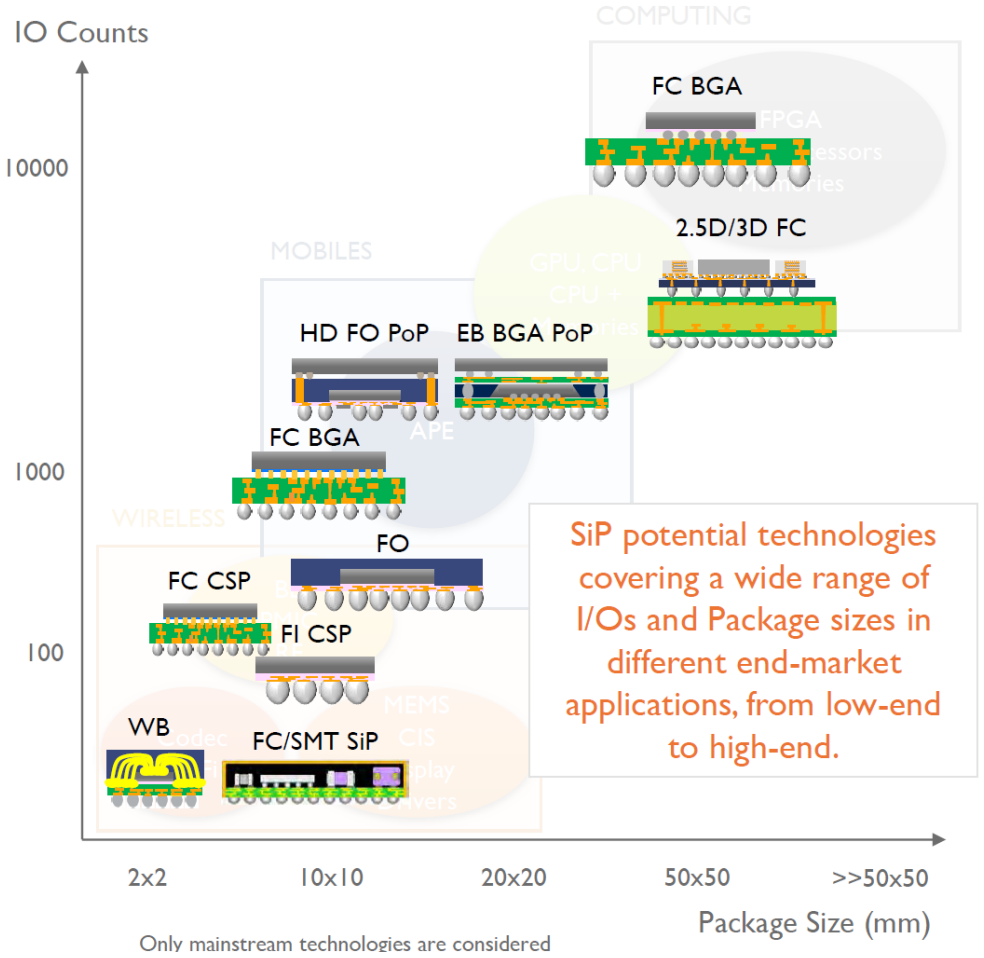
Advanced Packaging Technology



Source: „Advanced Packaging Landscape in Post-COVID Economy - Live Market Briefing", Yole Développement, JUL/16, 2020

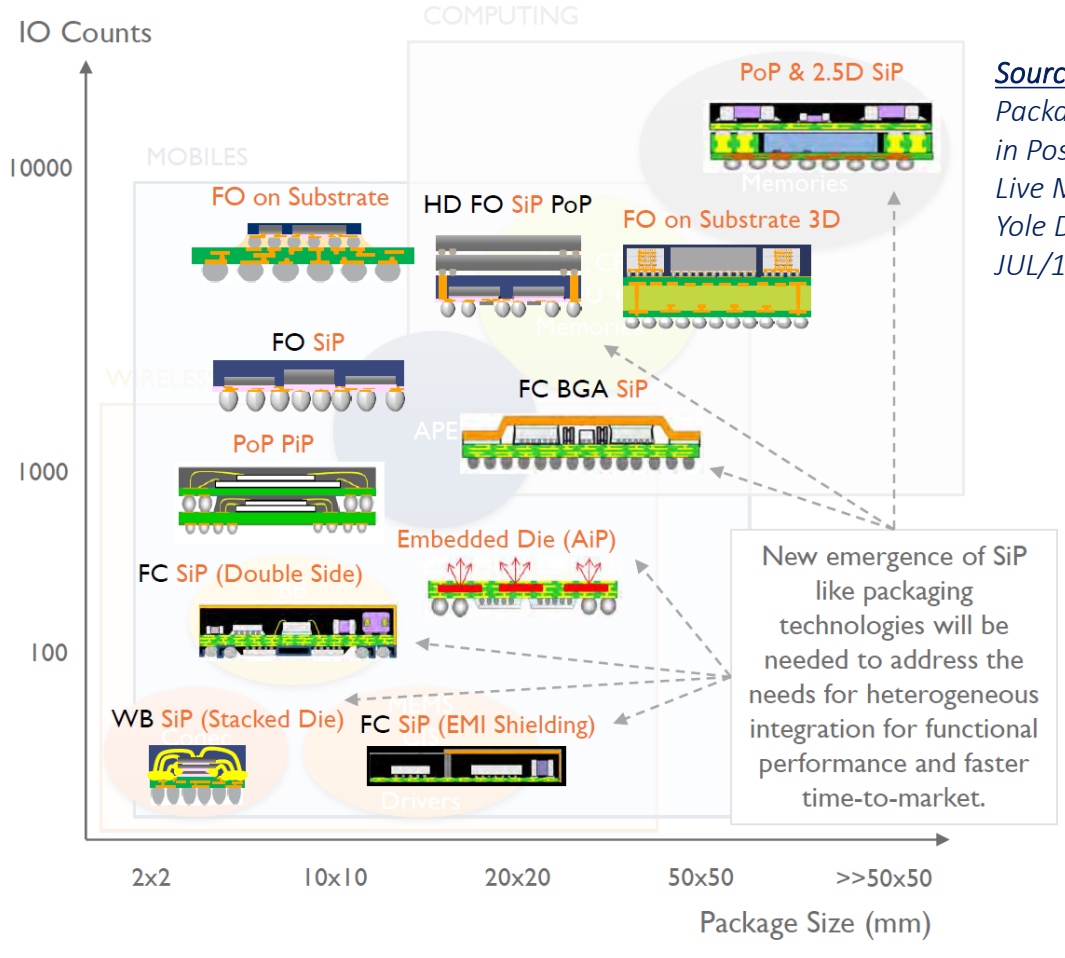
Advanced Packaging: Yesterday and Today

< 2019 : Packaging Technologies



Only mainstream technologies are considered

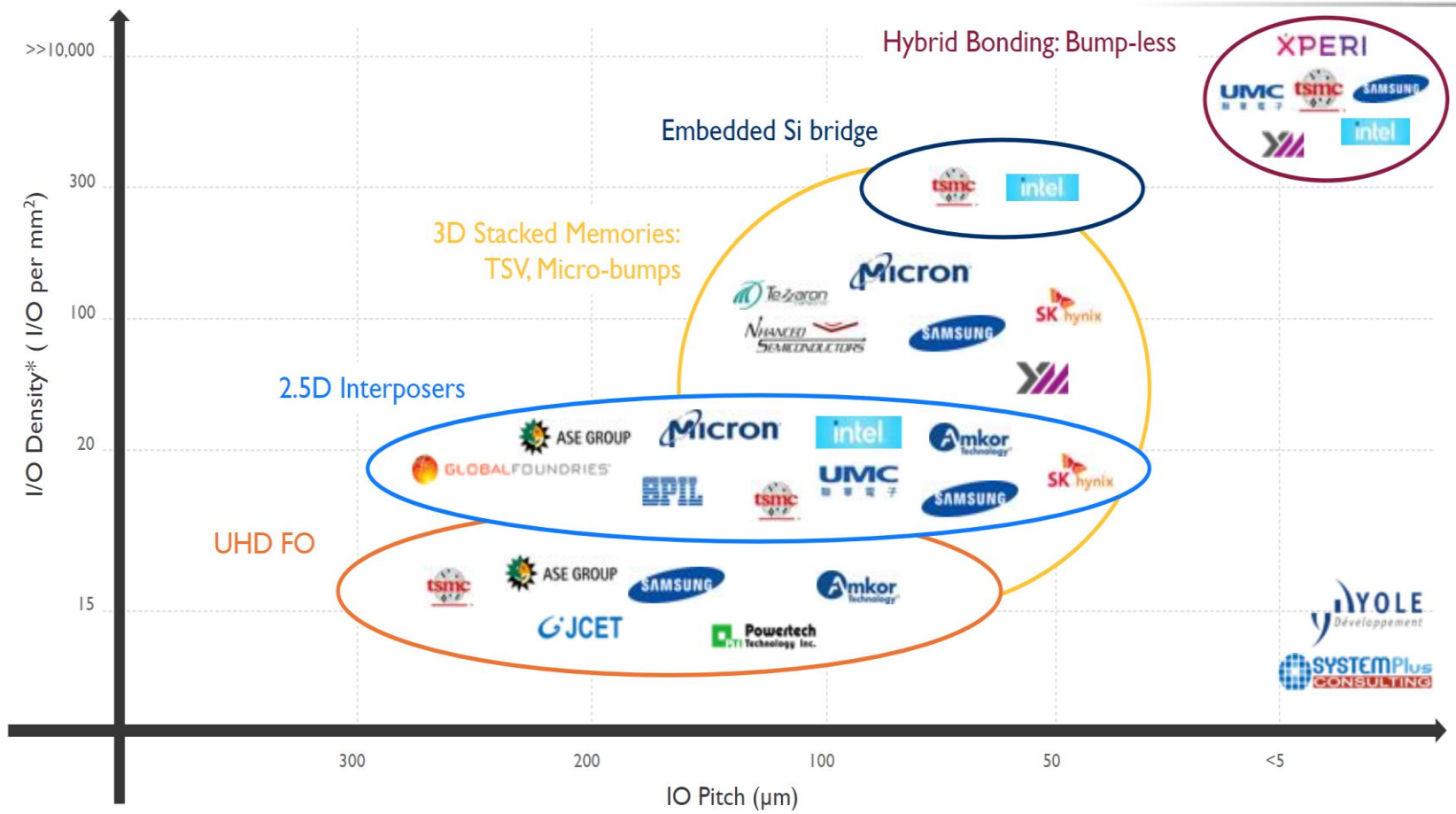
2019 - 2030 : New capabilities needed for multi-die solution



Source: „Advanced Packaging Landscape in Post-COVID Economy, Live Market Briefing", Yole Développement, JUL/16, 2020

2.5D/3D Integration - Packaging Landscape

Mapping of Players based on Technology



Chiplet Assembly in SiP

Disintegrated SoC
Chiplets = Functional blocks

D2W, W2W
SbS and 3D-Stack w/ TSV

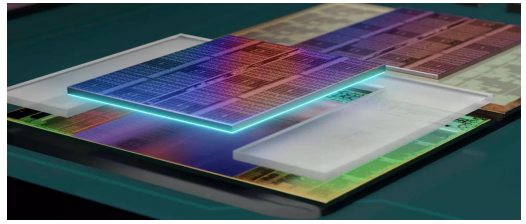
→ Smallest Pitch
→ Shortest connection

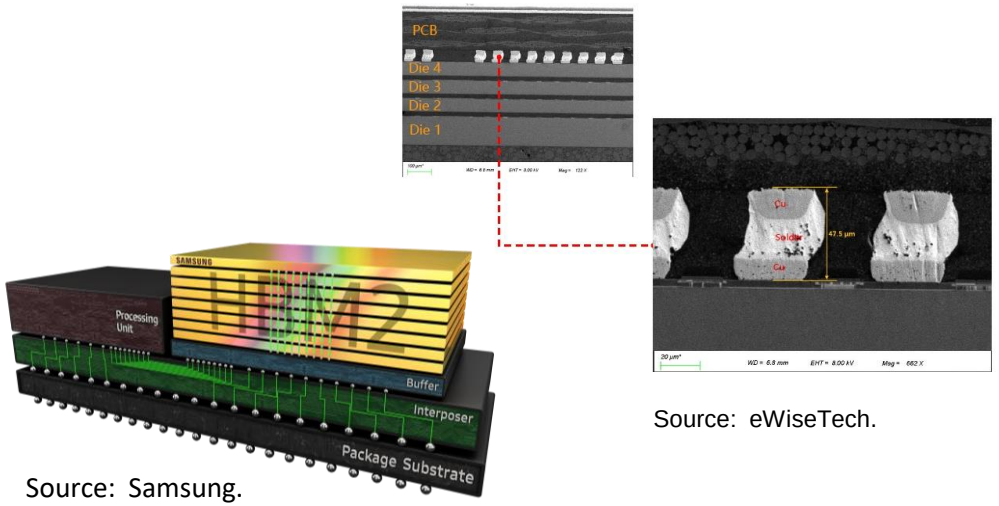
Source: Yole Développement Webinar "3D Packaging is transforming the world of Semiconductor Packaging", MAY/27, 2021

The Arrival of 3D IC

Available Solutions Today

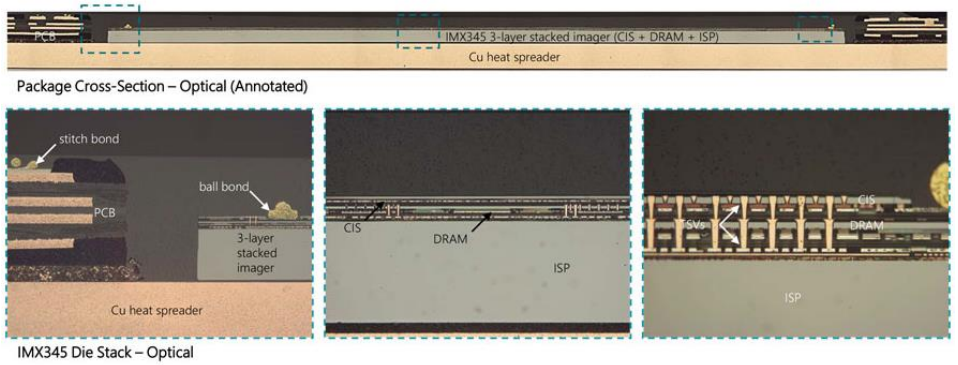
- **3D IC in production today**
  - CMOS image sensors
  - MEMS
  - High Bandwidth Memory (HBM) with µbumps
  - DDR DRAM with µbumps
  - NAND Flash (stacking cells)
- **3D IC attempts**
  - Mobile (Wide IO) with DRAM on logic stack
  - Considered but did not move into HVM due to thermal and business issues
- **3D IC moving into a new era—hybrid bonding**





Source: Samsung.

Source: eWiseTech.



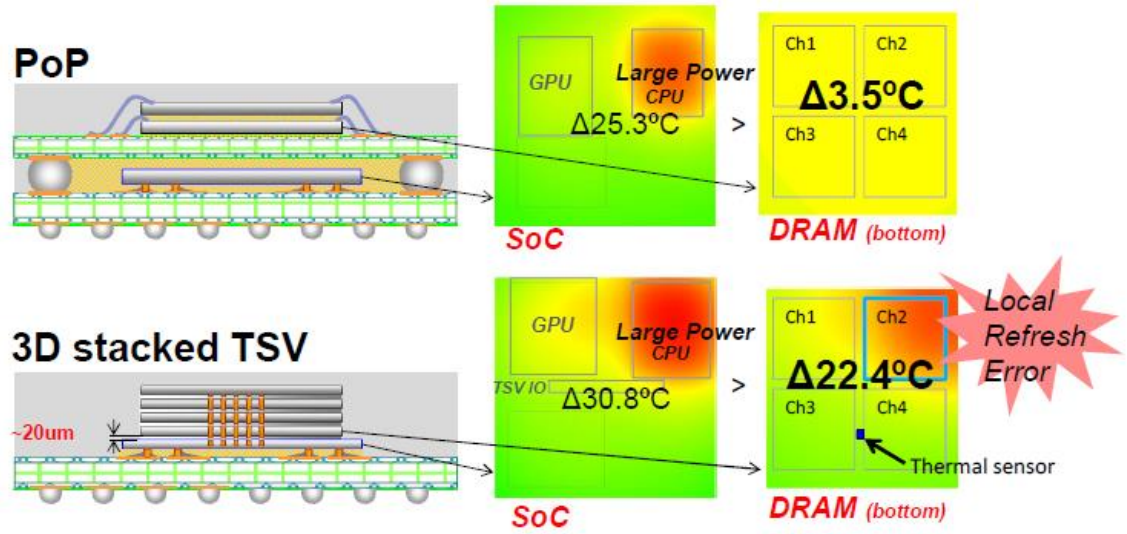
Images courtesy TechInsights.

Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

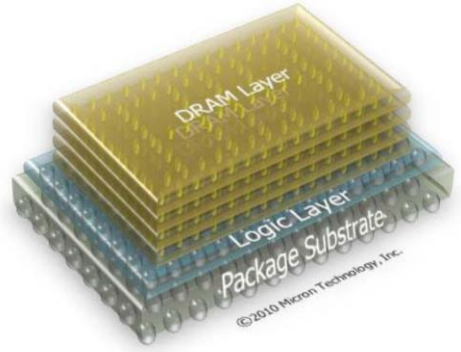
3D IC (Wide IO) Issues for Mobile Applications

Learnings About Thermal from Micron's HMC

- **Wide IO for mobile did not happen**
  - 3D IC process yield was low
  - Infrastructure and supply chain were not ready
  - More expensive/more risk than PoP
- **Thermal issues: 3D circuits increase total power generated per unit surface area**
  - Chips in the stack may overheat of cooling is not provided
  - Space may be too small for cooling channels (very small gap for fluid flow)
  - Thinning chips creates extreme conditions for on-chip hot spot



Source: Renesas.

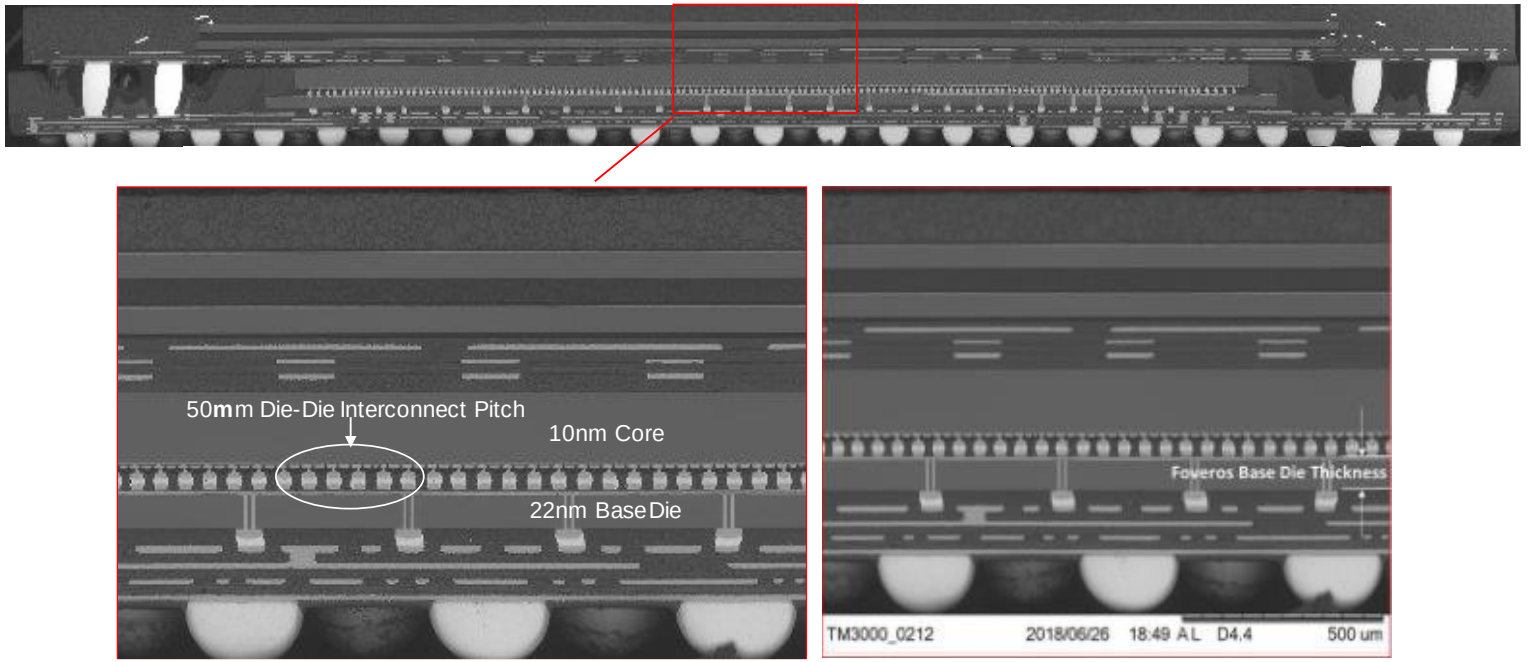


Source: Micron.

Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

Arrival of 3D IC: Chiplets!

Intel Foveros Technology: Stacking Chiplets with µBumps



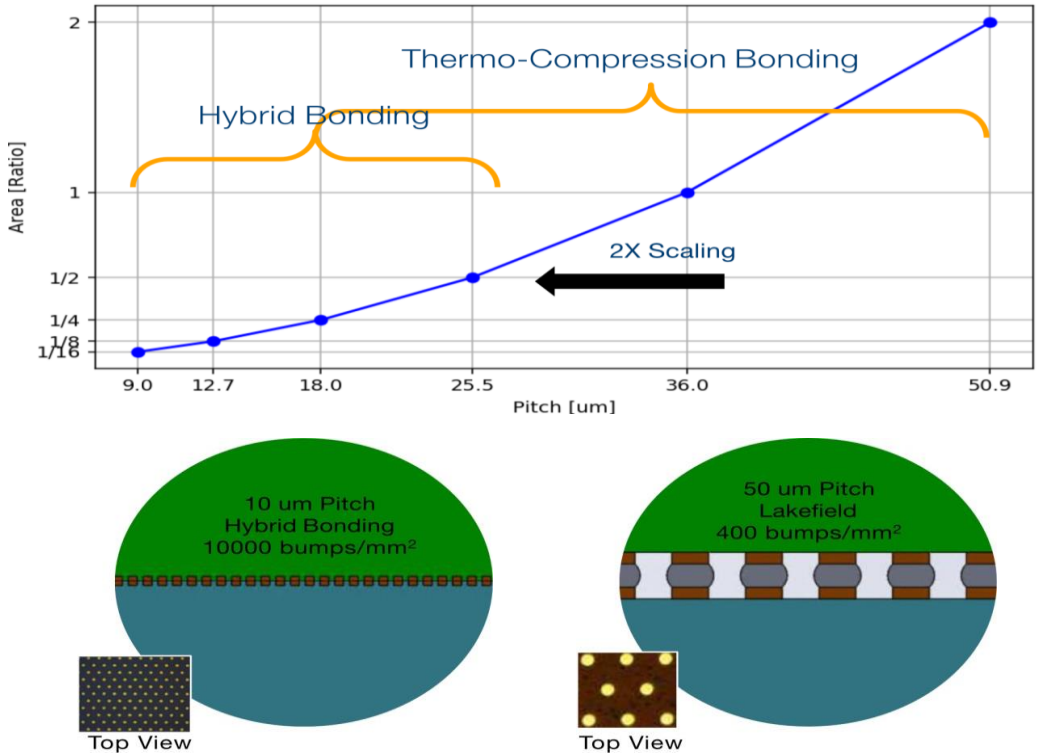
Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

- **Intel's Foveros 3D technology chiplets stacked with ~50µm pitch micro bumps, going to 36µm pitch**
  - Base chip can include power management features, voltage regulators, DC/DC converters (design flexibility to mix & match IP)
  - Die are co-designed, need to be floor-planned together to manage power delivery and thermals
  - Performance and size advantages

Arrival of 3D IC: Chiplets!

Higher Density and Performance Drives Move to Hybrid Bonding

- **Intel developing hybrid bonding interconnect (HBI) process for its Foveros technology (Foveros Direct)**
  - Investigating a pad pitch <10 µm providing low resistance interconnects
- **Hybrid bonding offers higher density**
  - Potential for a pad pitch of a few microns
  - Area scales with bump pitch
- **Performance advantages**
  - Low resistance interconnects

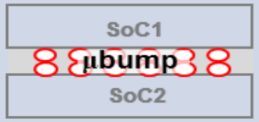


Source: Intel

Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

Arrival of 3D IC: Chiplets!

SoIC™ by TSMC Compared to 2.5D Interposer and 3D IC

Technology	2.5D	3D-IC	SoIC
Structure cross-section			
Interconnect	µbump + BEOL	µbump	SoIC bond
Chip Distance	**~100 µm**	**~30 µm**	**0**
Bond-pad Pitch	**36µm (1.0X)**	**36µm (1.0X)**	**9µm (0.25X)**
Speed	0.01X	1.0X	**11.9X**
Bandwidth Density	0.01X	1.0X	**191.0X**
Power Efficiency (Energy/bit)	22.9X	1.0X	**0.05X**

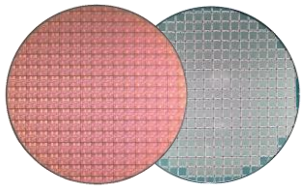
Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

- **With SoIC there is virtually no distance between integrated chips, and a very small bond-pad pitch of 9 µm provides good scalability**
- **Short die-to-die connections provide smaller form-factor, higher BW, better power integrity, signal integrity, and lower power consumption**

Arrival of 3D IC: Chiplets!

3D Stack with Hybrid Bonding ≠ Package

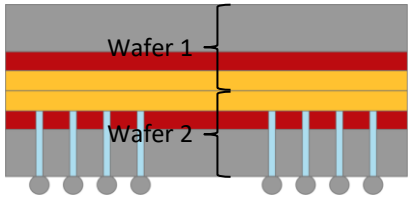
Wafer Fab



Silicon Wafers Processed

3D Stack with Hybrid Bond

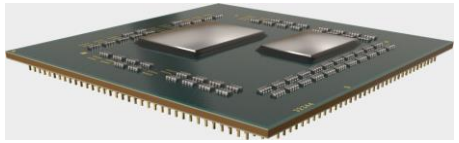
Takes place in cleanroom before BEOL



Bumping and Testing Prior to Assembly in Package

Package Assembly

Laminate Substrate BGA/PGA

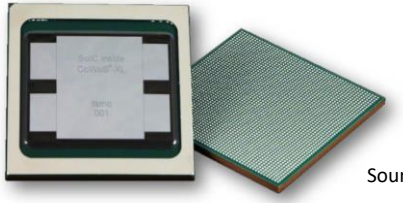


Source: AMD

Fan-Out on Substrate

Source: ASE

Silicon Interposer



Source: TSMC

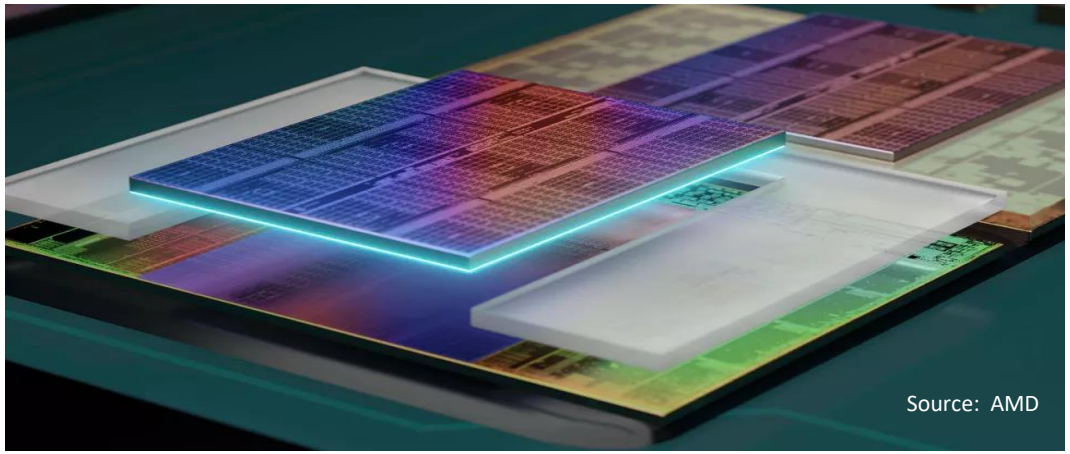
- **3D stack with hybrid bonding is not the package; it goes into a package**
- **Extension of the wafer fab process, treated like a wafer/ die**
- **Hybrid bonded 3D structure fabricated and transferred to BEOL for package assembly**

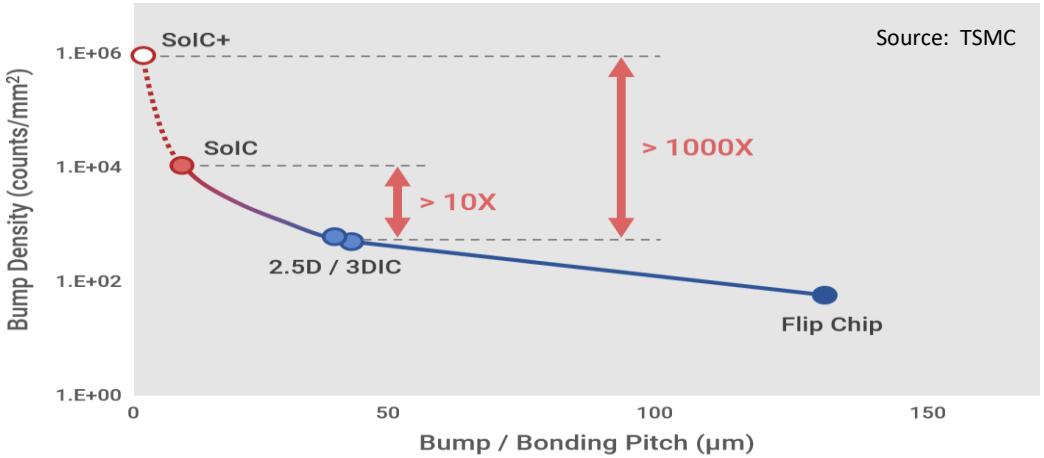
Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

Arrival of 3D IC: Chiplets!

Future Possibilities for 3D with Hybrid Bonding: The Beginning!

- **Future promises many new 3D stacking configurations**
  - Including W2W DRAM stacking
- **Enable realization of integration schemes not possible with monolithic designs**
  - Full die-to-die options, including logic on logic, core on core, macro on macro, circuit level slicing
- **Continue work is required**
  - Design
  - Process
  - Test
  - Thermal





Source: "The Arrival of 3D IC", Jan Vardaman, TechSearch International Inc., Keynote at "SEMI 3D & Systems Summit" in Dresden, Germany, JUN/14-15, 2022

NCCAVS User Groups

AVS Science and Technology of Materials, Interfaces, and Processing

NCCAVS Joint User Group Meeting
June 29th, 2022

Thanks for your attention !

steffen.kroehnert@espat-consulting.com

www.espat-consulting.com

ESPAT