CMP Process Challenges for mmWave Si Technology

Hong Jin Kim, Willie Lee, Lynn Covolo, Bryan Egan

GLOBALFOUNDRIES®

Time to reach 50 million users — adoption time reduced >99%!

38 | 13 | 4 | 3

Years

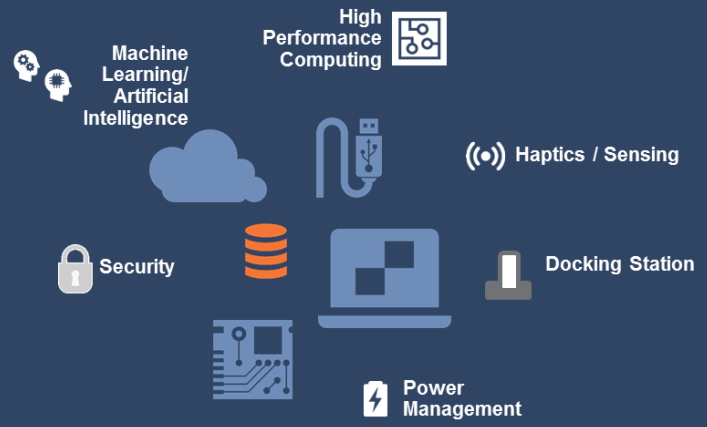
~3 months

+ COVID19 accelerate adoption time dramatically

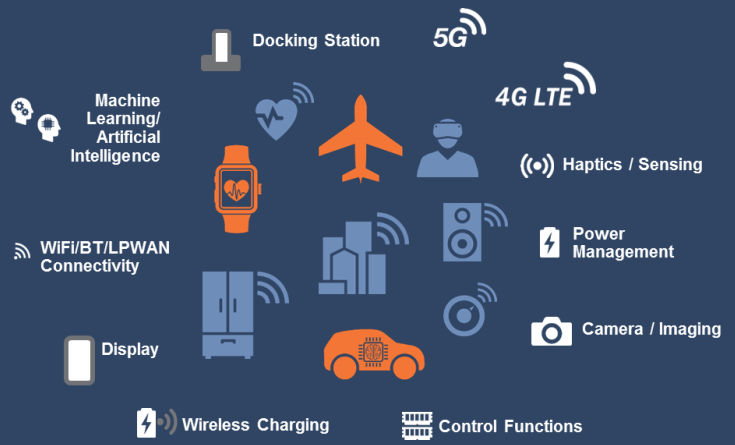
"The adoption of technology that would normally have taken a decade happened in one year in 2020 because of COVID-19," – T. Caulfield

High-growth market segments

Computing & wired infrastructure (CWI)

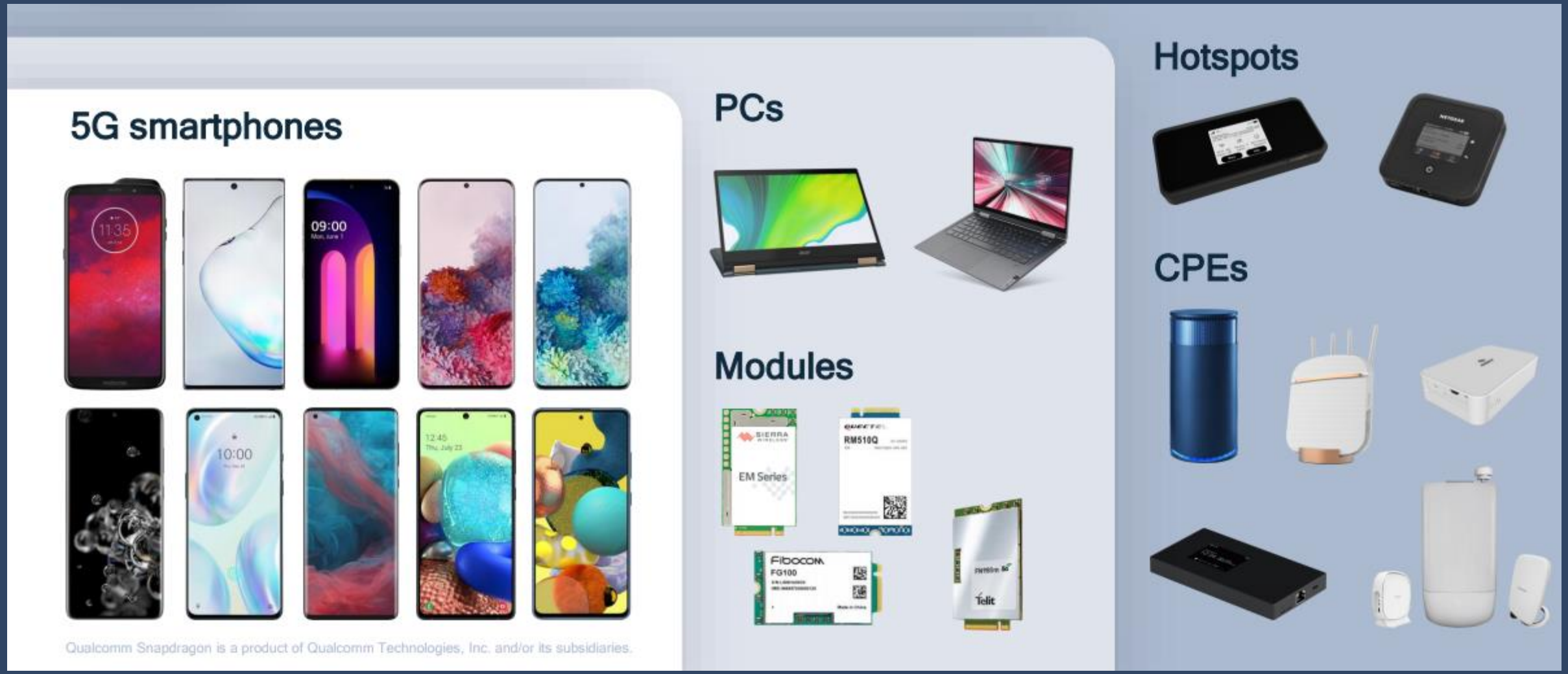


Auto, industrial & multi-market(AIM)



Mobile & wireless infrastructure (MWI)

mmWave commercial product example

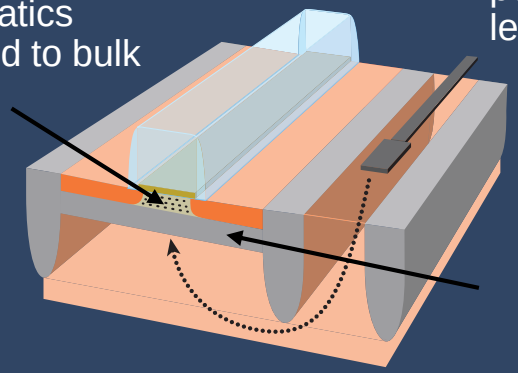


Source: Qualcomm blog post - https://www.qualcomm.com/media/documents/files/deploying-mmwave-to-unleash-5g-s-full-potential.pdf

RF Silicon-On-Insulator technologies

FDSOI

Fully **D**epleted
Channel for
superior FET
electrostatics
compared to bulk



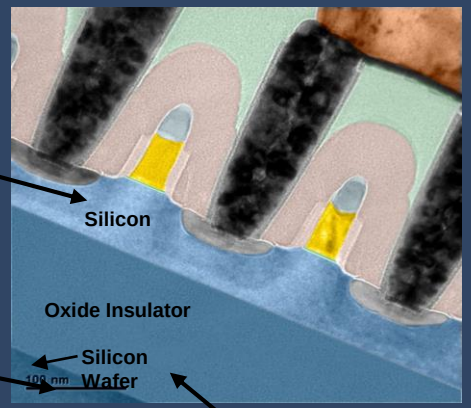
Back Gate Bias
to maximize
performance /
leakage

Ultra-thin Buried
Oxide Insulator for
back gate control

PDSOI

Partially **D**epleted
Channel for
Low Capacitance
compared to bulk

High Resistivity
Substrate for low
coupling loss



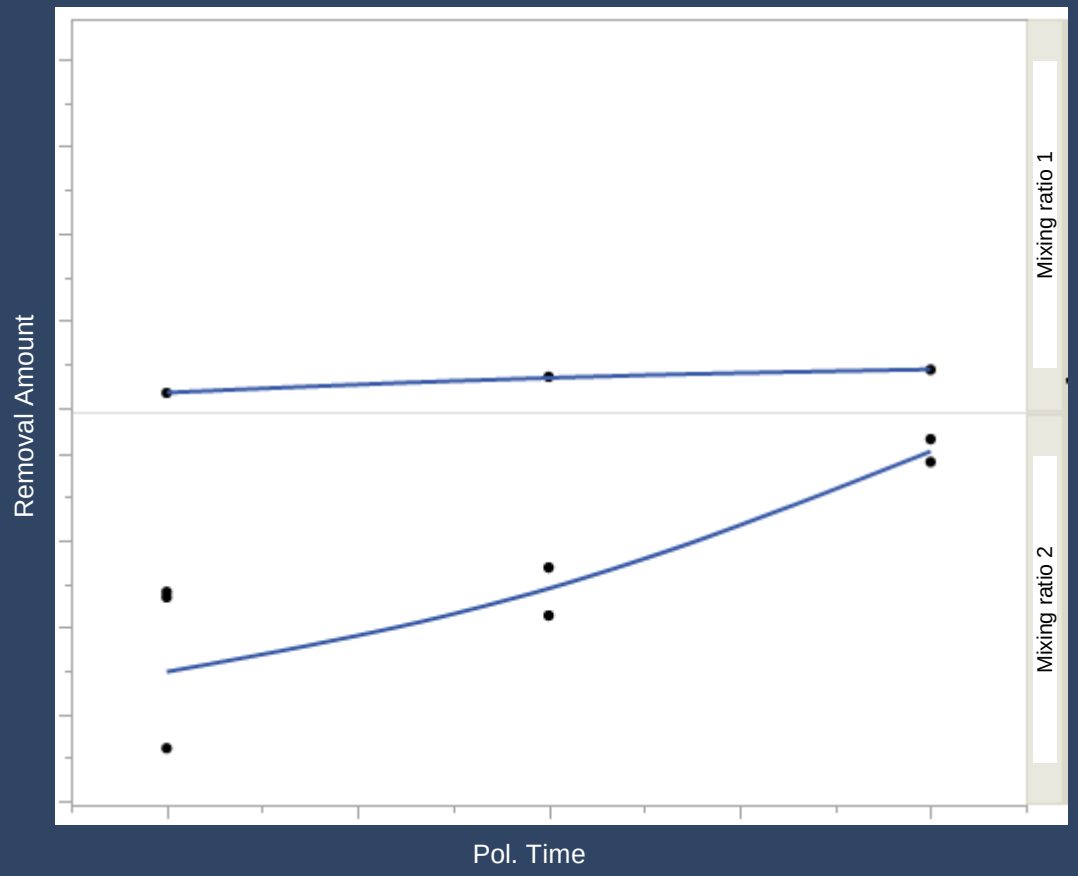
Thick Buried Oxide for
substrate isolation

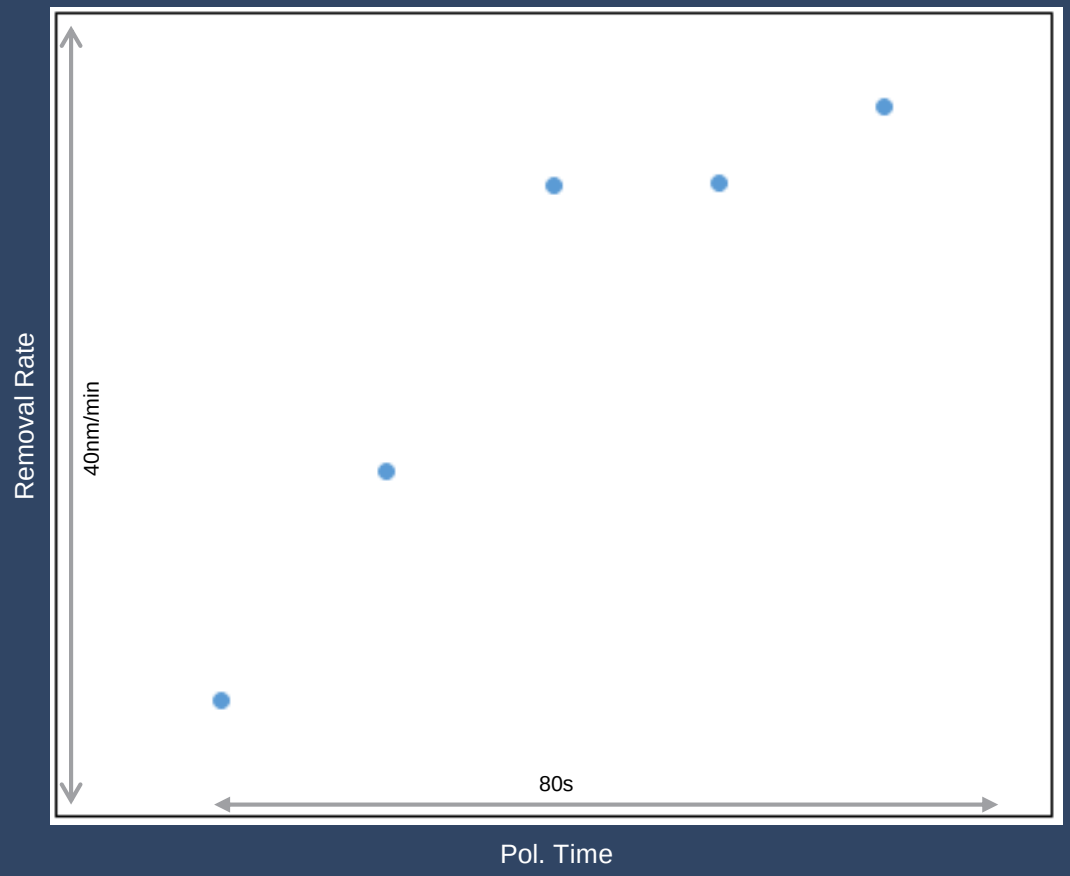
Source: N Cahoon, 2021IEEE Radio Wireless Week (RWW)/ Silicon monolithic Integrated Circuits (SiRF)

45RF SOI process flow and CMP steps

- STI CMP: Stop on nitride CMP. Dielectric polishing behavior is different depending on deposition process
- MOL oxide CMP: ILD CMP to planarize
- MOL W CMP
- Cu CMP

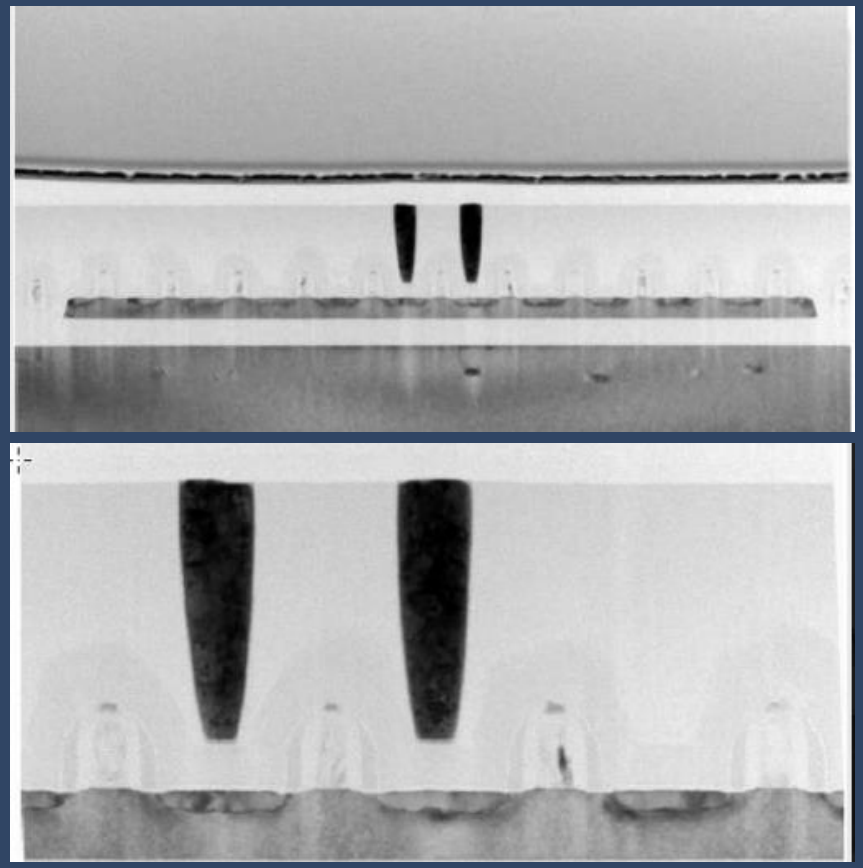
Loading effect – removal rate





Depending on slurries and film, CMP loading significantly influences oxide CMP in 45nm technology

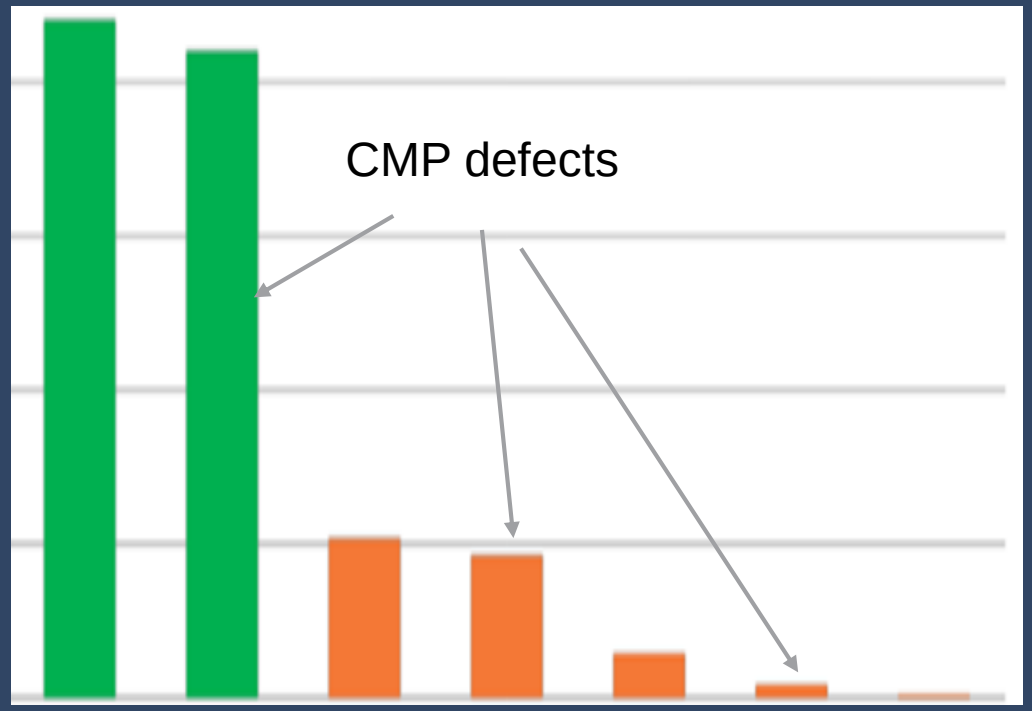
Oxide and W CMP



- Pattern density is lower than FinFET MOL
- Thicker oxide → high polish amount
- Planarization and uniformity is critical to oxide polishing
- High topography → easy to make residual W after W CMP
- Surface roughness control

Defects

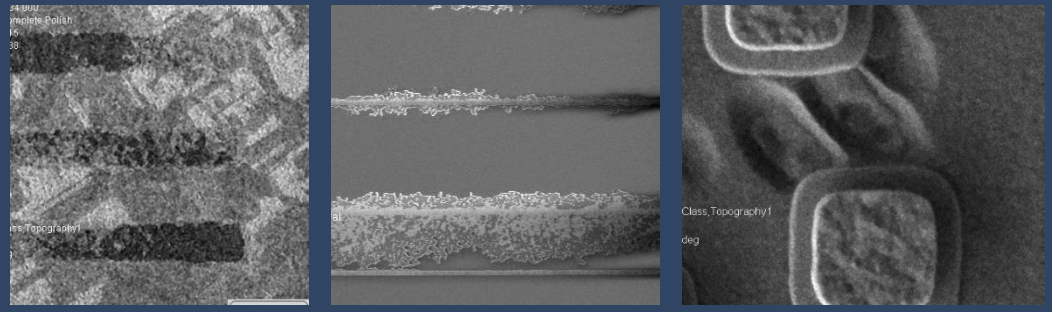
Defect pareto



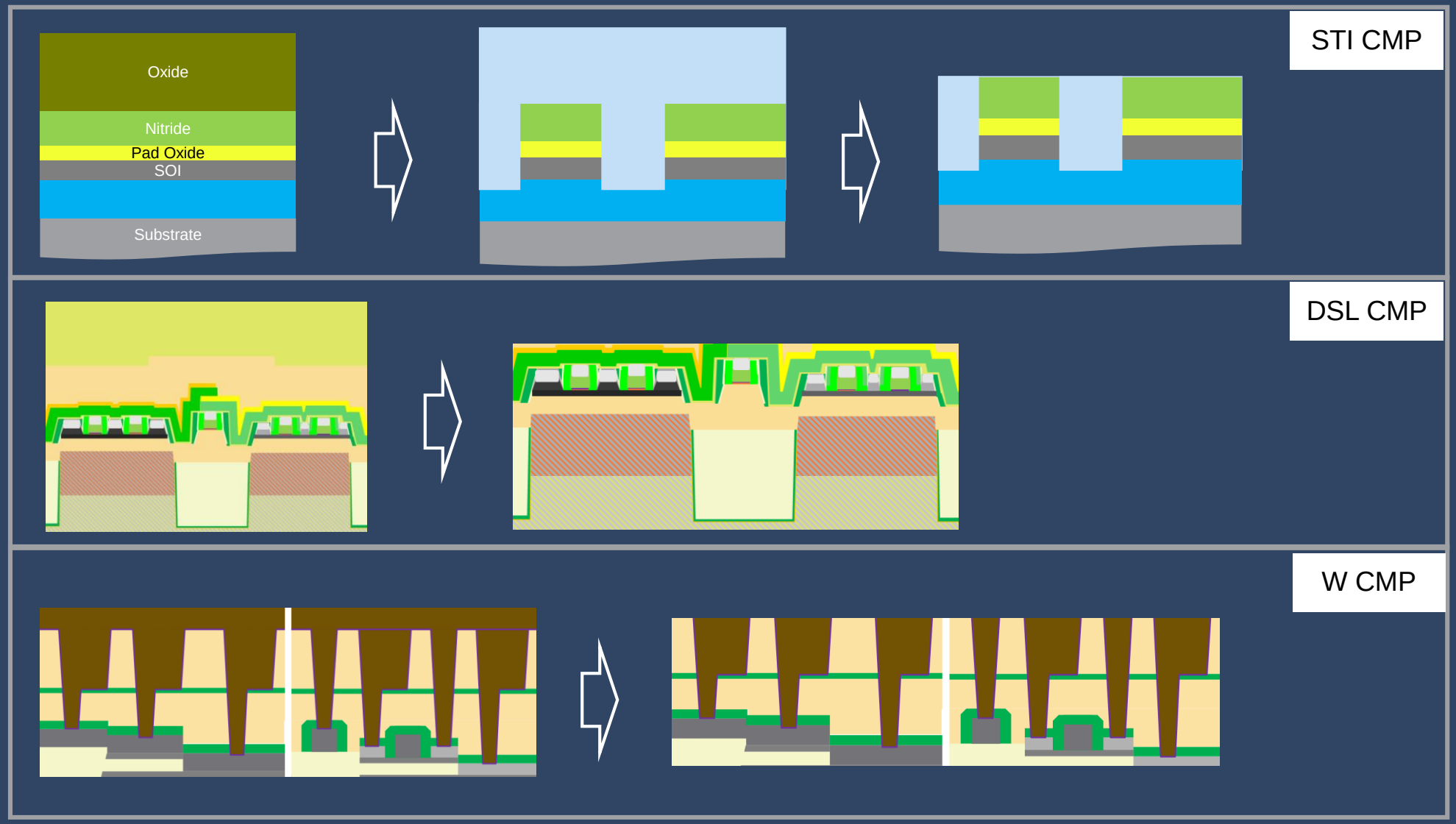
CMP-induced defects are yield detractors for all devices (ex. 3/7 DOIs are from CMP)

CMP DOIs for 45nm technology
1. Microscratch
2. Incomplete polish

*) Examples of CMP induced defects



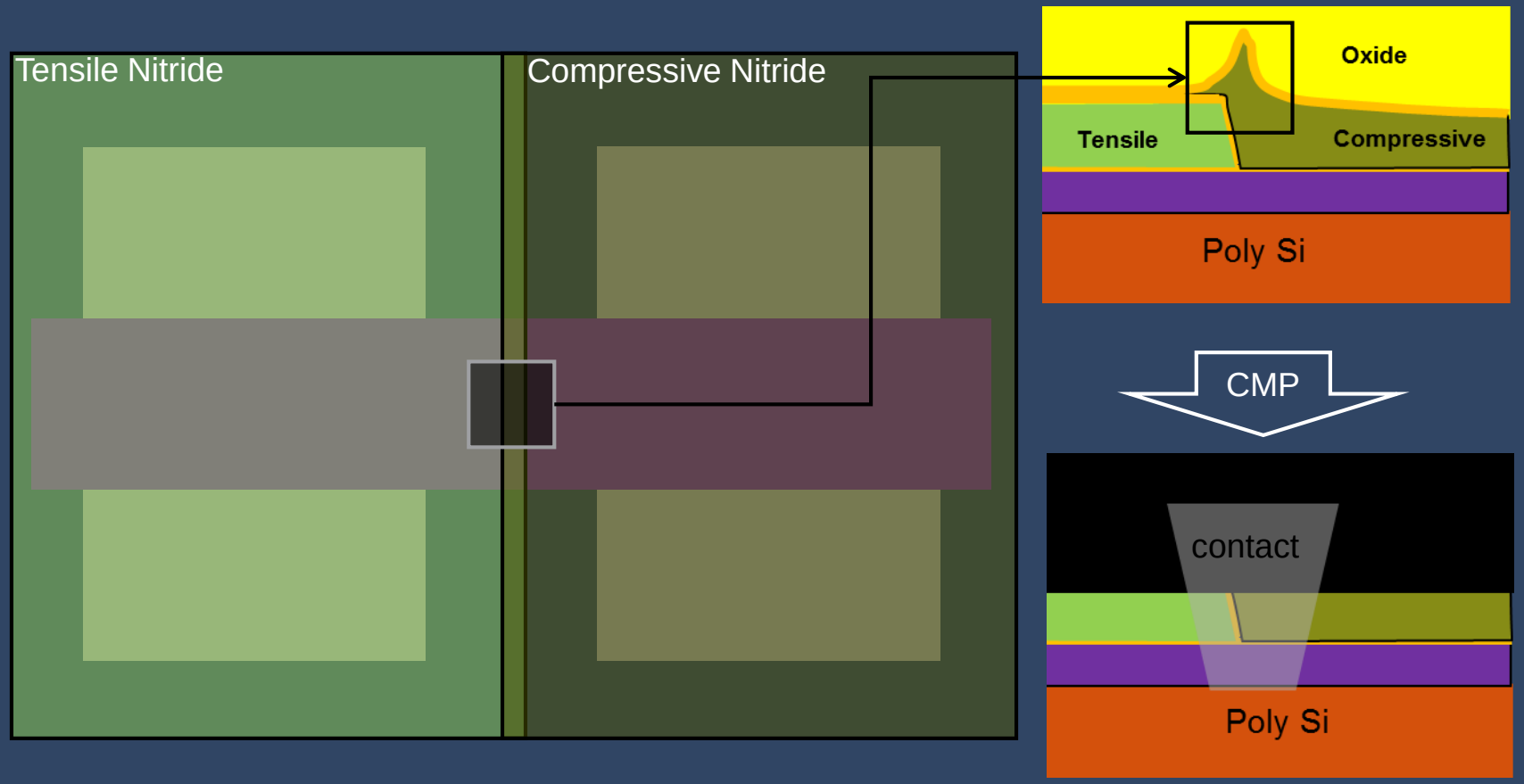
FD-SOI process flow and CMP steps

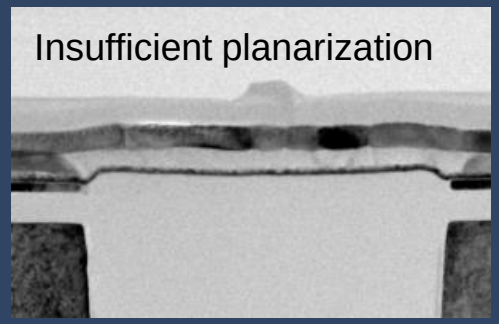


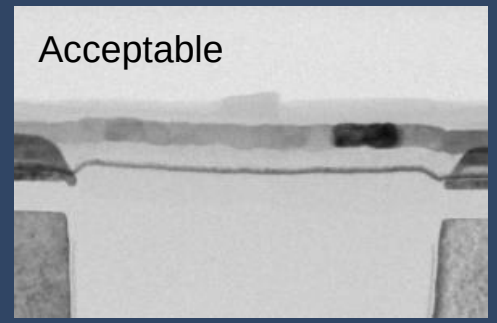
and Cu CMP

Dual stress liner process

Liner CMP: Nitride, but different stress



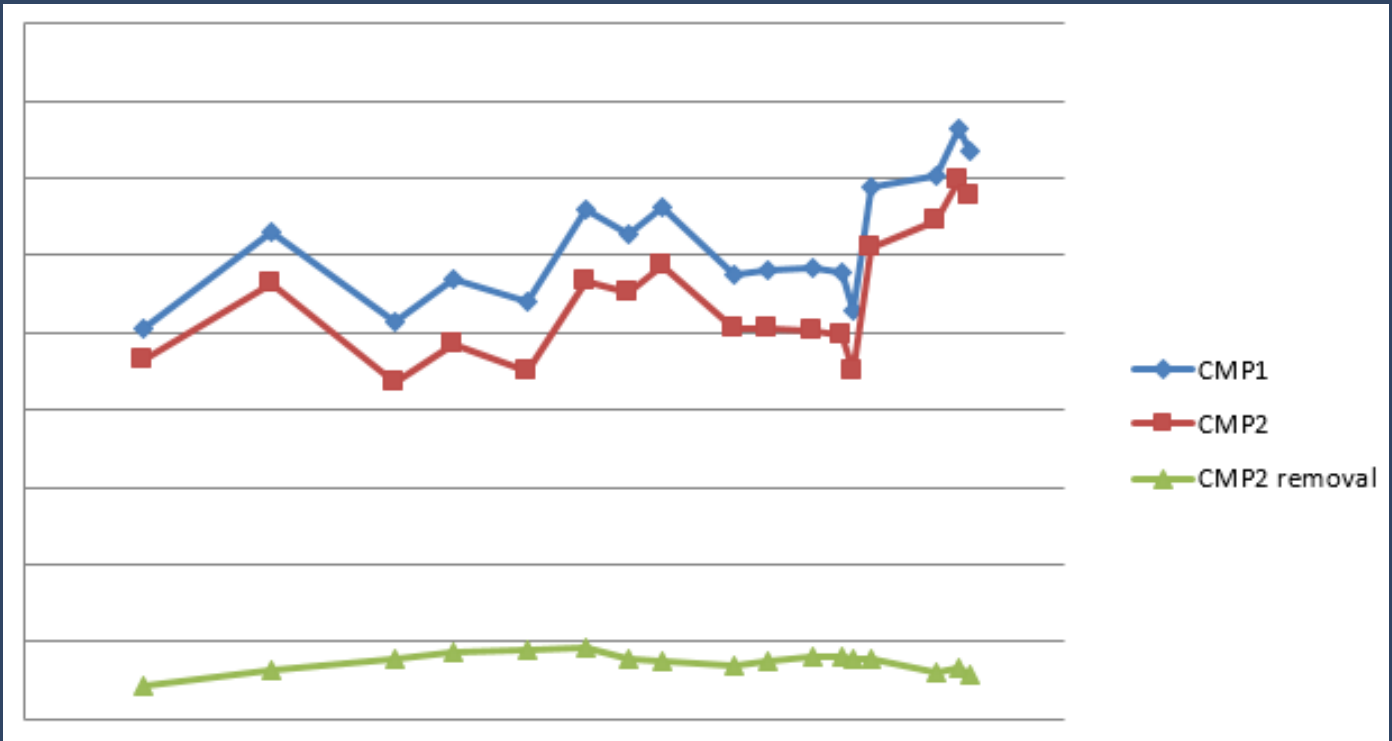




Source: H-J Kim, CAMP 2019

DSL CMP process challenge

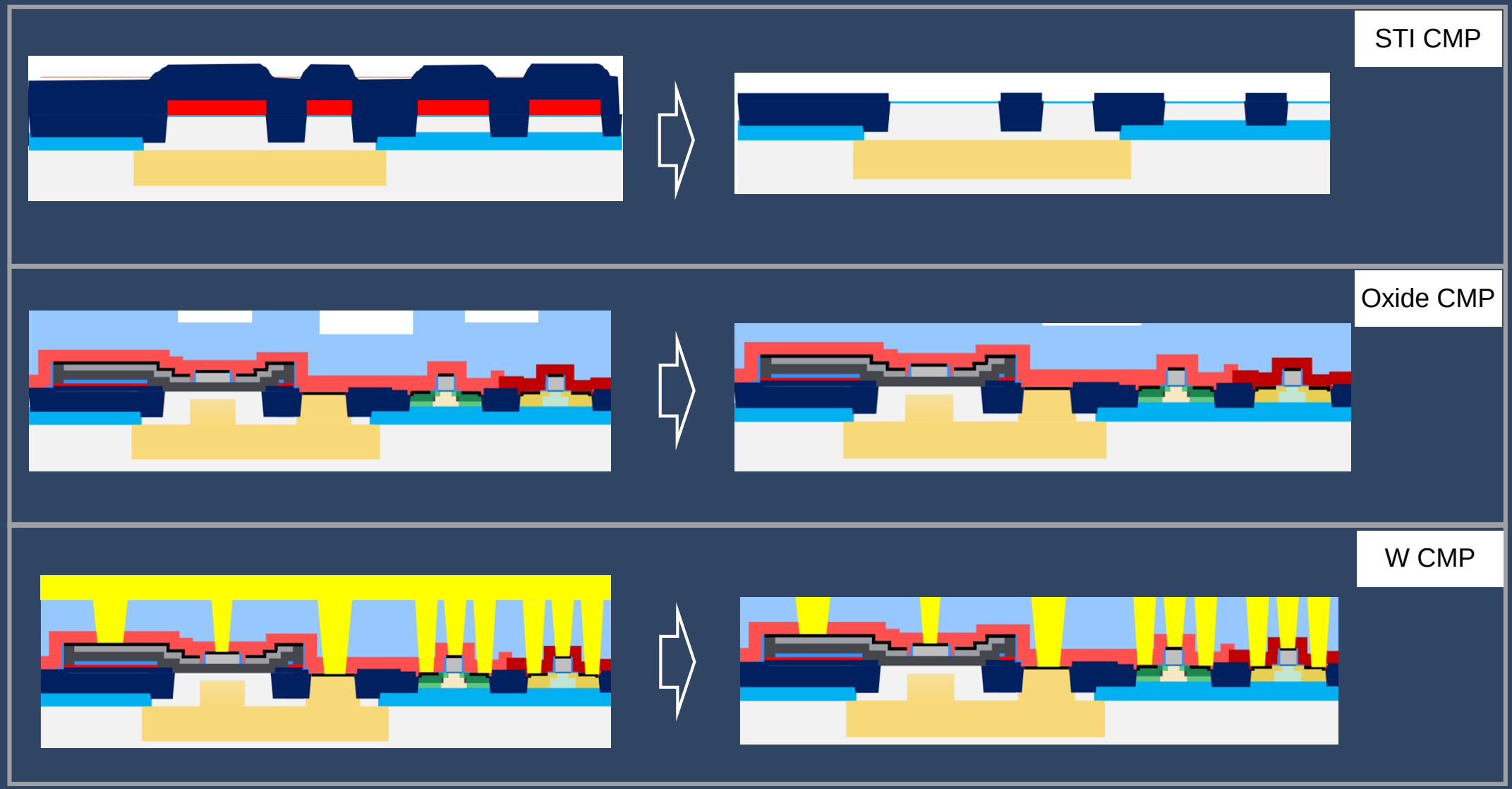
Post DSL CMP thickness profile



2 step CMP

1. CMP1: oxide CMP stop on nitride – high selective process and no residual oxide
2. CMP2: minimal oxide/nitride loss and bump nitride planarization

45nm SiGe BiCMOS CMP process



and Cu CMP

Summary

- STI CMP is covering all technologies for RX isolation
  - Different oxide depositions (material & process, ex: HARP/HDP...) have different polish behaviors, and loading effects impact polishing performance differently
  - Oxide removal rate stability – requires robust endpoint detection algorithm
  - Wider area and thicker nitride – requires controllable selectivity and dishing
- Oxide CMP is covering most derivatives
  - Planarization and uniformity
  - Edge control is critical
- W CMP for metal contact
  - Similar to advanced node tech., or legacy process
- Cu CMP
  - Similar to advanced node tech., or legacy process
  - Microscratch and arc-scratch are critical failure modes across the tech.
- Unique CMP – need fundamental understanding/CMP mechanism
  - Dual stress liner
  - EPI grown poly-Si