Ultra-Rapid Bulk Polishing of 150mm Silicon Carbide Substrate with Single Wafer CMP

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- SiC Technical terms
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Market Drivers
## Enabling Key Technology Inflections

<table>
<thead>
<tr>
<th><strong>IoT</strong></th>
<th><strong>Communications</strong></th>
<th><strong>Automotive</strong></th>
<th><strong>Power</strong></th>
<th><strong>Sensors</strong></th>
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<tbody>
<tr>
<td>Smart home</td>
<td>Mobile / smartphone</td>
<td>Autonomous vehicles</td>
<td>Datacenters</td>
<td>Wearable technologies</td>
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<tr>
<td>Industry 4.0</td>
<td>5G infrastructure</td>
<td>Infotainment and telemetry</td>
<td>Renewable energies</td>
<td>Voice and touch interfaces</td>
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<tr>
<td>Smart transportation</td>
<td>Increased data / video demand</td>
<td>Electric vehicle / Hybrid electric vehicle</td>
<td>Consumer and appliances</td>
<td>Gesture recognition</td>
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<tr>
<td>Building and automation / control</td>
<td>Silicon photonics</td>
<td>Faster battery charge</td>
<td>Emissions regulations</td>
<td>Facial recognition</td>
</tr>
<tr>
<td>Security and video surveillance</td>
<td>V2X communications</td>
<td></td>
<td>Higher efficiency systems</td>
<td></td>
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<tr>
<td></td>
<td>AR / VR</td>
<td></td>
<td>Smaller system solutions</td>
<td></td>
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</table>
SiC Substrate Wafer Size Inflections

~5 Years Between “Commercially Available” and Industry Adoption

Single Wafer Processing is the Future

Source: Yole 2018
SiC Report
Single Wafer SiC CMP
Mirra® Durum™

- ‘Hard’ or “Tough” in Latin

- Mirra®™ Durum™ is a high throughput, high quality polishing system designed for extremely hard materials such as Silicon Carbide. It is optimized for high volume manufacturing offering best in class throughput, quality, and uptime, with lowest cost of ownership.
Mirra® Durum™ Architecture

- 4 Membrane Polishing Heads
- 3 Platens
- 1 Loading/Unloading Station (Loadcup)
- “Cross” Assembly Rotates 270 degrees
- Simultaneous Polishing on 3 Platens while 4th Head is Unload/Load
- Robot “Flipping” Capability for Front + Packside Polishes (Si + C Faces)
- Active Platen Cooling + Active Process Temperature monitoring
- Integrated CRD + Precision Balance + OCR (Sept 2020)
**Mirra® Durum™ Competitive Advantages**

- Smallest Footprint
- Single Wafer/Independent Wafer Processing
  - Minimize Wafer Loss
- Membrane Carriers
  - No Setup for different wafer thickness
- Minimized Wafer Handoffs
- Faster Total Throughput
  - Load Cassettes (50 wafers) for Back → Front Polishing
  - Wafer Flipping
  - Automation
- Advanced Software for Wafer and Process Control
  - Wafer to Wafer Repeatability
- Proven platform in SiC production
  - >20,000 wafer polishes
Durum CMP System Consumables

- **Membrane head**
  - 3 – Zones of Pressure Adjustable up to 9psi
  - Independent Pressure Retaining Ring
  - Designed for Hard Material CMP Applications
- **Slurry**
  - Commercially available with Strong KMnO4 Oxidant
- **Pad/disk**
  - Commercially available Thermoplastic Polyurethane (TPU) Pads
  - Commercially available Diamond Disks;
SiC Technical Terms
SiC Substrate

- Hexagonal Single Crystal
- Semi-conducting
- Semi-insulating
- Si – Face
- C – Face
SiC Related Terms

- **Material Removal Rate (MRR)**
  - Removed thickness/ process time
  - Units = um/hr
- **Wafer-to-Wafer Uniformity (WTWNU)**
  - \((\text{Max THK} - \text{Min THK}) / \text{Stdev. \%}\)
- **Wafer Shape**
  - Total thickness variation (TTV)
  - Local thickness variation (LTV)
  - Units = um
- **Roughness**
  - Roughness average (Ra)
  - Units = nm
- **Defects**
  - Total scratch length
  - Units = mm
Batch CMP Comparison
SiC Single Wafer vs Batch Wafer CMP

- Batch CMP (20-24 Wafers) has Higher Inherent Defect Rates/Reduced Surface Quality
  - Average Results across all wafers
  - Material removed from one wafer affects other wafers
  - Requires Setup per Wafer Type
    - RF (350um) vs Power (500um)
- Single Wafer CMP Enables the Use of Stiffer Pads and High Performance Slurry
  - Higher removal rates (5.5um/hr vs 1.5um/hr)
  - Better surface roughness (Ra) results
- Single Wafer CMP is Highly Automated
  - Can run 50 wafer front/backside polish without operator intervention
  - Higher Throughput
  - Host download of recipe/recipe parameters
# SiC Single Wafer CMP vs Batch Wafer CMP

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Mirra Durum Single Wafer CMP</th>
<th>Batch CMP</th>
<th>Winner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Throughput (150mm) Si-side + C-side</td>
<td>~8 wafers per hour</td>
<td>~5-6 wafers per hour</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Throughput (200mm) Si-side + C-side</td>
<td>~8 wafers per hour</td>
<td>~3-4 wafers per hour</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Surface Quality</td>
<td>&gt;90% 5x5 Die Yield</td>
<td>&lt;90% 5x5 Die Yield</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Surface Roughness (Ra)</td>
<td>&lt;0.2nm</td>
<td>&lt;0.3nm</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Scratching &lt;20mm total length</td>
<td>&lt;20mm</td>
<td>&gt;20mm</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Factory Automation</td>
<td>50 wafer front/backside “lights out”</td>
<td>Manual operation</td>
<td>Mirra® Durum™</td>
</tr>
<tr>
<td>Wafer Breaks</td>
<td>1 wafer</td>
<td>All wafers</td>
<td>Mirra® Durum™</td>
</tr>
</tbody>
</table>
MRR Analysis
MRR – P*V Analysis

- SiC CMP exhibits Prestonian behavior
- Higher Platen Temperature increases MRR
Mirra Durum SiC CMP Repeatability – Bulk Polishing

- To removal rate: C-face is >3X faster than Si-face
- To WTWNU: both sides bulk polishing WTWNU is <3%

<table>
<thead>
<tr>
<th></th>
<th>WTWNU (%)</th>
<th>Avg RR (um/hr)</th>
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<tbody>
<tr>
<td>C-face</td>
<td>2.3</td>
<td>16.4</td>
</tr>
<tr>
<td>Si-face</td>
<td>2.9</td>
<td>5.1</td>
</tr>
</tbody>
</table>
SiC Surface Analysis
AFM Pre-Measurement (Ra)

Summary

- Durum CMP is capable of processing SiC wafers with various incoming roughness conditions
  - Group 1: Fine Lapping (Ra<1nm)
  - Group 2: Fine Lapping (Ra<2.5nm)
  - Group 3: Bulking Lapping (Ra:20-50nm)
- Identical 3 – Platen process will be utilized for both S-face and C-face

<table>
<thead>
<tr>
<th>Group</th>
<th>ID</th>
<th>AFM pre measurement Ra (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Si side                  C side</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Center</td>
</tr>
<tr>
<td>Group 1</td>
<td>1</td>
<td>1.43</td>
</tr>
<tr>
<td>Group 2</td>
<td>2</td>
<td>8.5</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>0.663</td>
</tr>
<tr>
<td>Group 2</td>
<td>4</td>
<td>1.4</td>
</tr>
<tr>
<td>Group 2</td>
<td>5</td>
<td>1.91</td>
</tr>
<tr>
<td>Group 2</td>
<td>6</td>
<td>1.32</td>
</tr>
<tr>
<td>Group 3</td>
<td>7</td>
<td>28.7</td>
</tr>
<tr>
<td>Group 3</td>
<td>8</td>
<td>35.1</td>
</tr>
<tr>
<td>Group 3</td>
<td>9</td>
<td>53</td>
</tr>
</tbody>
</table>
Summary:

- **Si face**
  - Ra <0.18nm
- **C face**
  - Ra <0.38nm
Mirra® Durum™ SiC CMP Defect Maps (after bulk polish)

Excellent Surface Finish/Particle Performance + No Scratches
SiC Shape Analysis
# Wafer Bow

## Summary

- **Positive pre Bow value → TTV increase after CMP**
- **Negative pre Bow value → TTV decrease after CMP**

## Graph Analysis

- **Group #1: positive Bow**
- **Group #2, negative Bow**

### Graph Details:

- **Pre CMP**
- **Post C-face CMP**
- **Post Si-face CMP**
<table>
<thead>
<tr>
<th>LTV Map Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Detection window = 5mm x 5mm</td>
</tr>
<tr>
<td>- EE = 0mm measurement</td>
</tr>
<tr>
<td>- 173 total measurement points</td>
</tr>
<tr>
<td>- 35 ea points at wafer edge area (R=65mm)</td>
</tr>
<tr>
<td>- 138 ea points at wafer center area</td>
</tr>
</tbody>
</table>

**Summary**
- LTV represents the thickness change within the detection window
- LTV analysis is usually focused on the wafer edge
- LTV edge performance can be modulated by polishing head setup
Summary
Summary Mirra® Durum™ CMP Performance

- High Material Removal Rate (MRR)
  - Si face = 5.5 um/hr
  - C face = 18.0 um/hr
- Wafer-to-Wafer Non-Uniformity (WTWNU)
  - WTWNU <5%
- Wafer Shape Control
  - Total thickness variation (TTV) <2.0 um (adder)
  - Local thickness variation (LTV) <0.5 um (adder)
- CMP Surface Improvement
  - Roughness (Ra) <0.2 nm
  - Total scratch length <20 mm (150mm SiC)
- Wafers Supported
  - RF Application = 350um thickness
  - Power Application = 500um thickness
  - No change in system setup
- Productivity Improvement
  - Fully automated S-face + C-face polishes
  - Membrane polishing head to reduce wafer breakage
- Production Proven
  - >20,000 wafers polished
Bio
Sean Yu was graduated from Virginia Commonwealth University (Richmond, VA, USA) with Master of Science degree in Mechanical Engineering at year of 2009, he joined Applied Materials as a process engineer in 2010.

He has 10 years’ experience in a board range of process development in CMP, CVD and wafer defect inspection process.

Currently, Sean and his colleagues are focusing on CMP process development and optimization on 6” SiC wafers, to improve the removal rate, reduce the surface defect and roughness with minimal wafer deformation.